

LSI Logic Data Book

1986

Bipolar and CMOS LSI/VLSI



TEXAS
INSTRUMENTS

General Information

1

LSI Devices

2

Application Reports

3

Mechanical Data

4

LSI Logic Data Book



**TEXAS
INSTRUMENTS**

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INTRODUCTION

The LSI Logic Data Book presents pertinent technical information on Texas Instruments complex bipolar, and CMOS LSI logic integrated circuits. The bipolar LSI products described in this volume include:

- The fastest TTL-compatible 8-bit processor slice chip set available. The chip set includes an 8-bit registered ALU, a 14-bit microsequencer, a 16- and 32-bit expandable barrel shifter, and a 16-word by 4-bit register file.
- The fastest stand-alone 32-bit error detection and correction circuit (EDAC)
- High-performance 16×4 and 16×5 "zero-fall-through" FIFOs (first in, first out) memory devices with 24-nanosecond fall-through times
- A high-speed "flash" 32-bit barrel shifter (SN74AS8838). The SN74AS8838 is the first member of the Texas Instruments 32-bit processor chip set.

Specifications on CMOS LSI products included in this volume describe the following:

- The THCT1010, which is the lowest power 16×16 -bit multiplier and accumulator (MAC) available.
- Two 64K and 256K DRAM controllers with inputs that are TTL- and CMOS-voltage compatible.
- Two high-speed CMOS multilevel pipeline registers, which offer a reduction in power over previously available devices.

To assist you in the selection of complex MSI logic components to complement a system design, the LSI Logic Data Book contains specifications on high-performance bus transceivers, readback latches, comparators, and controllers.

Many Texas Instruments leadership bipolar LSI functions use our new advanced bipolar technology, IMPACT™ (IMPlanted Advanced Composed Technology). This unique innovation offers performance advantages in speed, power, and circuit density over preceding bipolar technologies. The process offers such features as:

- 2- μ m feature size
- 7- μ m metal pitch
- Walled emitters
- Ion implantation
- Oxide isolation
- Composed masks

This data book provides a functional index to all bipolar digital device types available or under development. Packaging dimensions given in the Mechanical Data section of this book are in metric measurement (and parenthetically in inches), which should simplify board layout for designers involved in metric conversion and new designs. The general information section includes an explanation of the function tables, parameter measurement information, and typical characteristics related to the products listed in this volume.

Complete technical data for any Texas Instruments semiconductor/component product is available from your nearest TI field sales office, local authorized TI distributor, or by writing direct to:

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We sincerely believe that you will find the new LSI Logic Data Book a meaningful addition to your technical library.

General Information

1

Numerical Index
Glossary
Explanation of Function Tables
Parameter Measurement Information
Functional Index

LSI Devices

2

Application Reports

3

Advanced Schottky Family
Error Detection and Correction
Memory Mapping
Bit-Slice Processor 8-Bit Family
Excerpt – SN74AS888, SN74AS890
Bit-Slice Processor User's Guide

Mechanical Data

4

NUMERICAL INDEX

SN54AS181A	SN74AS181A	2-3	SN54AS852	SN74AS852	2-201
SN54LS222	SN74LS222	2-13	SN54AS856	SN74AS856	2-207
SN54LS224	SN74LS224	2-13	SN54AS867	SN74AS867	2-213
	SN74S225	2-21	SN54AS869	SN74AS869	2-213
SN54LS227	SN74LS227	2-13	SN54AS870	SN74AS870	2-219
SN54LS228	SN74LS228	2-13	SN54AS871	SN74AS871	2-219
SN54ALS229A	SN74ALS229A	2-27	SN54AS877	SN74AS877	2-225
SN54ALS232A	SN74ALS232A	2-33	SN54AS881A	SN74AS881A	2-3
SN54ALS233A	SN74ALS233A	2-37	SN54AS882A	SN74AS882A	2-231
	SN74AS250	2-43	SN54AS885	SN74AS885	2-239
SN54ALS280	SN74ALS280	2-47	SN54AS887	SN74AS887	2-245
SN54AS280	SN74AS280	2-47	SN54AS888	SN74AS888	2-293
SN54AS286	SN74AS286	2-53	SN54AS890	SN74AS890	2-343
SN54LS610	SN74LS610	2-59	SN54AS895	SN74AS895	2-361
SN54LS611	SN74LS611	2-59	SN54AS897A	SN74AS897A	2-411
SN54LS612	SN74LS612	2-59	SN54ALS963	SN74ALS963	2-429
SN54LS613	SN74LS613	2-59	SN54ALS964	SN74ALS964	2-429
SN54ALS616	SN74ALS616	2-69		SN74ALS990	2-441
SN54ALS617	SN74ALS617	2-69		SN74ALS991	2-441
SN54ALS632A	SN74ALS632A	2-81		SN74ALS992	2-449
SN54AS632	SN74AS632	2-97		SN74ALS993	2-449
SN54ALS633	SN74ALS633	2-81		SN74ALS994	2-457
SN54ALS634	SN74ALS634	2-81		SN74ALS995	2-457
SN54AS634	SN74AS634	2-97		SN74ALS996	2-465
SN54ALS635	SN74ALS635	2-81	SN54AS1181	SN74AS1181	2-471
SN54ALS646	SN74ALS646	2-111	SN54ALS2967	SN74ALS2967	2-483
SN54AS646	SN74AS646	2-111	SN54ALS2968	SN74ALS2968	2-483
SN54ALS647	SN74ALS647	2-111	SN54ALS6301	SN74ALS6301	2-503
SN54ALS648	SN74ALS648	2-111	SN54ALS6302	SN74ALS6302	2-503
SN54AS648	SN74AS648	2-111		SN74ALS8400	2-509
SN54ALS649	SN74ALS649	2-111	SN54AS8834	SN74AS8834	2-513
SN54ALS651	SN74ALS651	2-125	SN54AS8838	SN74AS8838	2-523
SN54AS651	SN74AS651	2-125	SN54ALS29818	SN74ALS29818	2-533
SN54ALS652	SN74ALS652	2-125	SN54ALS29819	SN74ALS29819	2-533
SN54AS652	SN74AS652	2-125	SN54ALS29821	SN74ALS29821	2-545
SN54ALS653	SN74ALS653	2-125	SN54ALS29822	SN74ALS29822	2-545
SN54ALS654	SN74ALS654	2-125	SN54ALS29823	SN74ALS29823	2-551
SN54ALS666	SN74ALS666	2-137	SN54ALS29824	SN74ALS29824	2-551
SN54ALS667	SN74ALS667	2-137	SN54ALS29825	SN74ALS29825	2-559
SN54AS821	SN74AS821	2-145	SN54ALS29826	SN74ALS29826	2-559
SN54AS822	SN74AS822	2-145	SN54ALS29827	SN74ALS29827	2-565
SN54AS823	SN74AS823	2-151	SN54ALS29828	SN74ALS29828	2-565
SN54AS824	SN74AS824	2-151	SN54ALS29861	SN74ALS29861	2-571
SN54AS825	SN74AS825	2-157	SN54ALS29862	SN74ALS29862	2-571
SN54AS826	SN74AS826	2-157	SN54ALS29863	SN74ALS29863	2-577
SN54ALS841	SN74ALS841	2-163	SN54ALS29864	SN74ALS29864	2-577
SN54AS841	SN74AS841	2-163	THCT1010-160M		2-583
SN54ALS842	SN74ALS842	2-163		THCT1010-100	2-583
SN54AS842	SN74AS842	2-163		THCT1010-140E	2-583
SN54ALS843	SN74ALS843	2-173	THCT2000M		2-593
SN54AS843	SN74AS843	2-173		THCT4502	2-597
SN54ALS844	SN74ALS844	2-173		THCT29520E	2-613
SN54AS844	SN74AS844	2-173		THCT29520	2-613
SN54ALS845	SN74ALS845	2-181		THCT29521E	2-613
SN54AS845	SN74AS845	2-181		THCT29521	2-613
SN54ALS846	SN74ALS846	2-181		TMS2150	2-619
SN54AS846	SN74AS846	2-181		TMS4500A	2-627
	SN74AS850	2-191			
	SN74AS851	2-191			

1
General Information

INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

PART I — OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

- | | |
|------------------------|---|
| f_{max} | Maximum clock frequency
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification. |
| I_{CC} | Supply current
The current into* the V _{CC} supply terminal of an integrated circuit. |
| I_{CCH} | Supply current, outputs high
The current into* the V _{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the high level. |
| I_{CCL} | Supply current, outputs low
The current into* the V _{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the low level. |
| I_{IH} | High-level input current
The current into* an input when a high-level voltage is applied to that input. |
| I_{IL} | Low-level input current
The current into* an input when a low-level voltage is applied to that input. |
| I_{OH} | High-level output current
The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output. |
| I_{OL} | Low-level output current
The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output. |
| I_{OS} | Short-circuit output current
The current into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential). |
| I_{OZH} | Off-state (high-impedance-state) output current (of a three-state output) with high-level voltage applied
The current flowing into* an output having three-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output and with a high-level voltage applied to the output.
NOTE: This parameter is measured with other input conditions established that would cause the output to be at a low level if it were enabled. |

*Current out of a terminal is given as a negative value.



GLOSSARY

TTL SYMBOLS, TERMS, AND DEFINITIONS

IOZL	Off-state (high-impedance-state) output current (of a three-state output) with low-level voltage applied The current flowing into* an output having three-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output and with a low-level voltage applied to the output. NOTE: This parameter is measured with other input conditions established that would cause the output to be at a high level if it were enabled.
VIH	High-level input voltage An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables. NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.
VIK	Input clamp voltage An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.
VIL	Low-level input voltage An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables. NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.
VOH	High-level output voltage The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a high level at the output.
VOL	Low-level output voltage The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a low level at the output.
t_a	Access time The time interval between the application of a specified input pulse and the availability of valid signals at an output.
t_{dis}	Disable time (of a three-state or open-collector output) The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state. NOTE: For 3-state outputs, $t_{dis} = t_{PHZ}$ or t_{PLZ} . Open-collector outputs will change only if they are low at the time of disabling so $t_{dis} = t_{PLH}$.
t_{en}	Enable time (of a three-state or open-collector output) The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low). NOTE: In the case of memories, this is the access time from an enable input (e.g., \overline{G}). For 3-state outputs, $t_{en} = t_{PZH}$ or t_{PZL} . Open-collector outputs will change only if they are responding to data that would cause the output to go low so $t_{en} = t_{PHL}$.

*Current out of a terminal is given as a negative value.

t_h	<p>Hold time The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.</p> <p>NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.</p> <p style="padding-left: 2em;">2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.</p>
t_{pd}	<p>Propagation delay time The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. ($t_{pd} = t_{PHL}$ or t_{PLH}).</p>
t_{PHL}	<p>Propagation delay time, high-to-low-level output The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.</p>
t_{PHZ}	<p>Disable time (of a three-state output) from high level The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.</p>
t_{PLH}	<p>Propagation delay time, low-to-high-level output The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.</p>
t_{PLZ}	<p>Disable time (of a three-state output) from low level The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.</p>
t_{PZH}	<p>Enable time (of a three-state output) to high level The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.</p>
t_{PZL}	<p>Enable time (of a three-state output) to low level The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.</p>
t_{sr}	<p>Sense recovery time The time interval needed to switch a memory from a write mode to a read mode and to obtain valid data signals at the output.</p>
t_{su}	<p>Setup time The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.</p> <p>NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.</p> <p style="padding-left: 2em;">2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.</p>
t_w	<p>Pulse duration (width) The time interval between specified reference points on the leading and trailing edges of the pulse waveform.</p>

GLOSSARY

TTL SYMBOLS, TERMS, AND DEFINITIONS

PART II — CLASSIFICATION OF CIRCUIT COMPLEXITY

Gate Equivalent Circuit

A basic unit-of-measure of relative digital-circuit complexity. The number of gate equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

Large-Scale Integration, LSI

A concept whereby a complete major subsystem or system function is fabricated as a single microcircuit. In this context a major subsystem or system, whether digital or linear, is considered to be one that contains 100 or more equivalent gates or circuitry of similar complexity.

Medium-Scale Integration, MSI

A concept whereby a complete subsystem or system function is fabricated as a single microcircuit. The subsystem or system is smaller than for LSI, but whether digital or linear, is considered to be one that contains 12 or more equivalent gates or circuitry of similar complexity.

Small-Scale Integration, SSI



Integrated circuits of less complexity than medium-scale integration (MSI).

Very-Large-Scale Integration, VLSI



The description of any IC technology that is much more complex than large-scale integration (LSI), and involves a much higher equivalent gate count. At this time an exact definition including a minimum gate count has not been standardized by JEDEC or the IEEE.



The following symbols are used in function tables on TI data sheets:

- H = high level (steady state)
- L = low level (steady state)
- ↑ = transition from low to high level
- ↓ = transition from high to low level
- = value/level or resulting value/level is routed to indicated destination
- ↻ = value/level is re-entered
- X = irrelevant (any input, including transitions)
- Z = off (high-impedance) state of a 3-state-output
- a . . h = the level of steady-state inputs at inputs A through H respectively
- Q_0 = level of Q before the indicated steady-state input conditions were established
- \bar{Q}_0 = complement of Q_0 or level of \bar{Q} before the indicated steady-state input conditions were established
- Q_n = level of Q before the most recent active transition indicated by ↓ or ↑
-  = one high-level pulse
-  = one low-level pulse
- TOGGLE = each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑.

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0 , or \bar{Q}_0), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse,  or , the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

EXPLANATION OF FUNCTION TABLES

Among the most complex function tables in this book are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

CLEAR	MODE		CLOCK	INPUTS				OUTPUTS					
				SERIAL		PARALLEL		Q _A	Q _B	Q _C	Q _D		
				LEFT	RIGHT	A	B					C	D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q _{An}	Q _{Bn}	Q _{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q _{An}	Q _{Bn}	Q _{Cn}
H	H	L	↑	H	X	X	X	X	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output Q_A, data entered at B will be at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

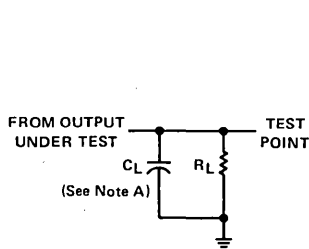
The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both mode inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

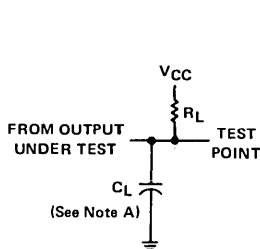
1

General Information

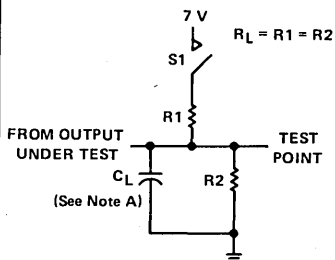
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

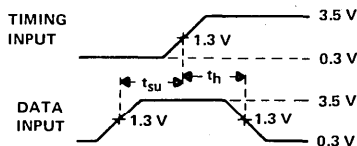


LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

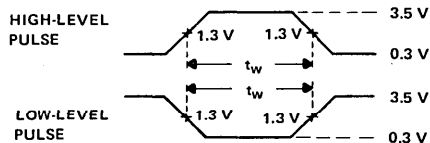


LOAD CIRCUIT FOR THREE-STATE OUTPUTS

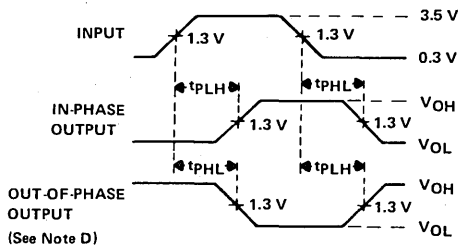
NOTE A: C_L includes probe and jig capacitance.



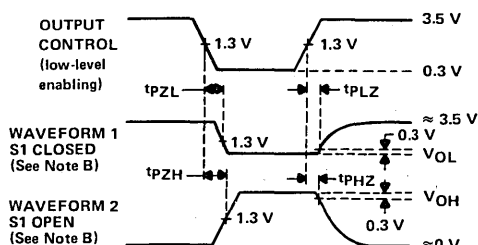
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

1
General Information

GATES AND INVERTERS

POSITIVE-NAND GATES AND INVERTERS

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	H	L	LS	
Hex 2-Input Gates	'804	●	A	B				3
Hex Inverters	'04	●	A	●	●	●	●	2
	'1004	●	A	●				3
Quadruple 2-Input Gates	'00	●	A	●	●	●	●	2
	'1000	●	A	A				3
Triple 3-Input Gates	'10	●	A	●	●	●	●	2
	'1010	●	A					3
Dual 4-Input Gates	'20	●	A	●	●	●	●	2
	'1020	●	A					3
8-Input Gates	'30	●	A	●	●	●	●	2
		●	A	●				3
13-Input Gates	'133	●	●					2
Dual 2-Input Gates	'8003	●	●					3

POSITIVE-NAND GATES AND INVERTERS WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	H	L	LS	
Hex Inverters	'05	●			●	●	●	2
	'1005	●	A					3
Quadruple 2-Input Gates	'01	●	●		●	●	●	2
	'03	●	●			●	●	3
	'1003	●	B					2
Triple 3-Input Gates	'12	●	A			●	●	3
	'22	●	A					2
Dual 4-Input Gates	'22	●	B					3

POSITIVE-AND GATES

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	H	LS	S	
Hex 2-Input Gates	'808	●	A	B				3
	'08	●	●	●	●	●	●	2
Quadruple 2-Input Gates	'1008	●	A					3
	'11	●			●	●	●	2
Triple 3-Input Gates	'11	●	A	●				3
	'1011	●	A					3
Dual 4-Input Gates	'21	●	●		●	●		2
Triple 4-Input AND/NAND	'800	●	▲					3

POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	H	LS	S	
Quadruple 2-Input Gates	'09	●				●	●	2
		●	●					3
Triple 3-Input Gates	'15	●	A		●	●	●	2
		●	A					3

POSITIVE-OR GATES

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	L	LS	S	
Hex 2-Input Gates	'832	●	A	B				3
	'32	●	●	●	●	●	●	2
Quadruple 2-Input Gates	'1032	●	●	●				3
	'1032	●	A	●				3
Triple 4-Input OR/NOR	'802	●	▲					3

POSITIVE-NOR GATES

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	L	LS	S	
Hex 2-Input Gates	'805	●	A	B				3
	'02	●	●	●	●	●	●	2
Quadruple 2-Input Gates	'1002	●	A					3
	'27	●	●	●	●	●	●	2
Dual 4-Input Gates with Strobe	'25	●	●	●	●	●	●	3
Dual 5-Input Gates	'260	●					●	2

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	L	LS	S	
Hex Inverters	'14	●				●	●	2
	'19	●				●	●	
Octal Inverters	'619	●				●	●	
Dual 4-Input Positive-NAND	'13	●				●	●	
Triple 4-Input Positive-NAND	'18	●				●	●	
Quadruple 2-Input Positive-NAND	'618	●				●	●	
	'24	●				●	●	
	'132	●				●	●	

CURRENT-SENSING GATES.

DESCRIPTION	TYPE	TECHNOLOGY			VOLUME
		ALS	AS	LS	
Hex	'63			●	2

DELAY ELEMENTS

DESCRIPTION	TYP	TECHNOLOGY			VOLUME
		ALS	AS	LS	
Inverting and Noninverting Elements, 2-Input NAND Buffers	'31			●	2

- Denotes available technology.
- ▲ Denotes planned new products.
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General Information

FUNCTIONAL INDEX

GATES, EXPANDERS, BUFFERS, DRIVERS, AND TRANSCEIVERS

AND-OR-INVERT GATES

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	H	L	LS	
2-Wide 4-Input	'55				●	●	●	2
4-Wide 4-2-3-2 Input	'64						●	
4-Wide 2-2-3-2 Input	'54				●			
4-Wide 2-Input	'54	●						
4-Wide 2-3-3-2 Input	'54					●	●	
Dual 2-Wide 2-Input	'51	●			●	●	●	

AND-OR-INVERT GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY				VOLUME
		STD TTL	ALS	AS	S	
4-Wide 4-2-3-2 Input	'65				●	2

EXPANDABLE GATES

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	H	L	LS	
Dual 4-Input Positive-NOR with Strobe	'23	●						2
4-Wide AND-OR	'52				●			
4-Wide AND-OR-INVERT	'53	●			●			
2-Wide AND-OR-INVERT	'55				●	●	●	
Dual 2-Wide AND-OR-INVERT	'50	●			●	●	●	

EXPANDERS

DESCRIPTION	TYPE	TECHNOLOGY				VOLUME
		STD TTL	ALS	AS	H	
Dual 4-Input	'60	●			●	2
Triple 3-Input	'61				●	
3-2-2-3 Input AND-OR	'62				●	

BUFFER AND INTERFACE GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	LS	S		
Hex	'07	●					2	
	'17	●						
	'35		●					
Hex Inverter	*1035		●				3	
	'06	●						
	'16	●						
Quad 2-Input Positive-NAND	*1005		●				3	
	'26	●			●			
	'38				●	●		
	'39	●	A					
	*1003		A					
Quad 2-Input Positive-NOR	'33	●			●		2	
			A					3

BUFFERS, DRIVERS, AND BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	LS	S		
Noninverting Octal Buffers/Drivers	'743		▲				3	
	'757		●	●				
	'760			●				
Inverting Octal Buffers/Drivers	'742		▲					
	'756			●				
	'763		●	●				
Inverting and Noninverting Octal Buffers/Drivers	'762		●	●				
Noninverting Quad Transceivers	'759			●				
Inverting Quad Transceivers	'758			●				

● Denotes available technology.

▲ Denotes planned new products.

A Denotes "A" suffix version available in the technology indicated.

GATES, EXPANDERS, BUFFERS, DRIVERS, AND TRANSCEIVERS

GATES, BUFFERS, DRIVERS, AND BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Noninverting 10-Bit Buffers/Drivers	'29827	▲					LSI
Inverting 10-Bit Buffers/Drivers	'29828	▲					
Noninverting 10-Bit Transceivers	'29861	▲					
Inverting 10-Bit Transceivers	'29862	▲					
Noninverting 9-Bit Transceivers	'29863	▲					
Inverting 9-Bit Transceivers	'29864	▲					
Noninverting Octal Buffers/Drivers	'241		●	●	●	●	2
	'241	A	●	●	●	●	3
	'244		●	●	●	●	2
	'244	A	●	●	●	●	3
	'465		●				2
	'465	A	●				3
	'467		●		●		2
	'467	A	●		●		3
	'541	●			●		2
	'1241 ^f	▲					3
'1244 ^f	A						
Inverting Octal Buffers/Drivers	'231	●	●	●	●	●	2
	'240	A	●	●	●	●	3
	'466		●				2
	'466	A	●				3
	'468		●				2
	'468	A	●				3
	'540	●			●		2
'1240 ^f	●					3	
Inverting and Noninverting Octal Buffers/Drivers	'230		●				3
Octal Transceivers	'245		●	●			2
	'1245	A	●	●			3
Noninverting Hex Buffers/Drivers	'365	A	●		A		2
	'365		●				3
	'367	A	●		A		2
Inverting Hex Buffers/Drivers	'366		●				3
	'366	A	▲		A		2
	'368	A	▲		A		3
Quad Buffers/Drivers with Independent Output Controls	'125	●			A		2
	'126	●			A		
	'425	●					
	'426	●					
Noninverting Quad Transceivers	'243		●				3
	'1243 ^f	▲	●				
Inverting Quad Transceivers	'242		●				3
	'1242 ^f	●	●				
Quad Transceivers with Storage	'226				●		2
12-Input NAND Gate	'134				●		

50-OHM/75-OHM LINE DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY				VOLUME
		STD TTL	ALS	AS	S	
Hex 2-Input Positive-NAND	'804		A	B		3
Hex 2-Input Positive-NOR	'805		A	B		
Hex 2-Input Positive-AND	'808		A	B		
Hex 2-Input Positive-OR	'832		A	B		
Quad 2-Input Positive-NOR	'128	●				2
Dual 4-Input Positive-NAND	'140				●	

1
General Information

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- ▲ Denotes planned new products.
- ^f Denotes very low power.
- A Denotes "A" suffix version available in the technology indicated.
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BUFFERS, DRIVERS, TRANSCEIVERS, AND CLOCK GENERATORS

BUFFERS, CLOCK/MEMORY DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	H	LS	S	
Hex 2-Input Positive-NAND	'804		A	B				3
Hex 2-Input Positive-NOR	'805		A	B				
Hex 2-Input Positive-AND	'808		A	B				
Hex 2-Input Positive-OR	'832		A	B				
Hex Inverter	'1004		●					
Hex Buffer	'34		●					
	'1034		●	A				
Quad 2-Input Positive-NAND	'37	●				●	●	2
	'1000		A					3
	'1002	●	A	●				2
Quad 2-Input Positive-NOR	'28		A					3
	'1006		A					
	'1036			A				
Quad 2-Input Positive-AND	'1008		A	●				3
Quad 2-Input Positive-OR	'1032		A	●				
Triple 3-Input Positive-NAND	'1010		A					
Triple 3-Input Positive-AND	'1011		A					
Triple 4-Input AND-NAND	'800			▲				
Triple 4-Input OR-NOR	'802			▲				
Dual 4-Input Positive-NAND	'40	●			▲	●	●	2
	'1020		A					3
Line Driver/Memory Driver with Series Damping Resistor	'436						●	2
Line Driver/Memory Driver	'437						●	

OCTAL BI-/TRI-DIRECTIONAL BUS TRANSCEIVERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY			VOLUME
			ALS	AS	LS	
12 mA/24 mA/48 mA/64 mA Sink, True Outputs	Low Power	3 State	'245	A	●	3
		OC	'621	A	●	3
		3 State	'623	A	●	2
		OC, 3 State	'639	A	●	3
		3 State	'652	●	●	3 & LSI
		OC, 3 State	'654	▲		2
	Very Low Power	OC	'1621	▲		2
		3 State	'1623	▲		3
		OC, 3 State	'1639	▲		3
		OC	'622	A	●	2
12 mA/24 mA/48 mA/64 mA Sink, Inverting Outputs	Low Power	3 State	'620	A	●	3
		OC	'622	A	●	3
		3 State	'638	A	●	3
		OC, 3 State	'638	●	●	3 & LSI
		3 State	'651	●	●	2
		OC, 3 State	'653	▲		3
	Very Low Power	3 State	'1620	▲		3
		OC	'1622	▲		3
		OC, 3 State	'1638	▲		3
		OC	'641	A	●	2
12 mA/24 mA/48 mA/64 mA Sink, True Outputs	Low Power	3 State	'645	A	●	3
		3 State	'645	A	●	2
		OC	'1641	▲		3
	Very Low Power	3 State	'1645	A	●	3
		OC	'640	A	●	2
		OC	'642	A	●	3
12 mA/24 mA/48 mA/64 mA Sink, Inverting Outputs	Low Power	3 State	'640	A	●	2
		OC	'642	A	●	3
		OC	'642	A	●	2
	Very Low Power	3 State	'1640	A	●	3
		OC	'1642	▲		3
		OC	'643	A	●	2
12 mA/24 mA/48 mA/64 mA Sink, True and Inverting Outputs	Low Power	3 State	'644	A	●	3
		OC	'644	A	●	2
		3 State	'1644	▲		3
	Very Low Power	3 State	'1643	▲		3
		OC	'1644	▲		3
		OC	'643	A	●	2
Registered with Multiplexed 12 mA/24 mA/48 mA/64 mA True Outputs	3 State	'646	●	●	3 & LSI	
	OC	'647	●	●	3	
Registered with Multiplexed 12 mA/24 mA/48 mA/64 mA Inverting Outputs	3 State	'648	●	●	3 & LSI	
	OC	'649	●	●	2	
Universal Transceiver/Port Controllers	3 State	'877	●	●	3 & LSI	
		'852	●	●	3 & LSI	
		'856	●	●	2	
		'856	●	●	2	

BI-/TRI-DIRECTIONAL BUS TRANSCEIVERS AND DRIVERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY				VOLUME
			ALS	AS	LS	S	
Quad with Bit Direction	3-State	'446			●		2
Controls	3-State	'449			●		
	OC	'440			●		
Quad Tridirection	OC	'441			●		
	3-State	'442			●		
	3-State	'443			●		
	3-State	'444			●		
	OC	'448			●		
	3-State	'226			●	●	
4-Bit with Storage	3-State	'226			●	●	

OCTAL BUS TRANSCEIVERS/MOS DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Inverting Outputs, 3-State	'2620		●				3
True Outputs, 3-State	'2640		●				
	'2623		●				
	'2645		●				

OCTAL BUFFERS AND LINE DRIVERS WITH INPUT/OUTPUT RESISTORS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Input Resistors	Inverting Outputs	'746	●				3
	Noninverting Outputs	'747	●				
Output Resistors	Inverting Outputs	'2540	●				
	Noninverting Outputs	'2541	●				

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1 General Information

FLIP-FLOPS

DUAL AND SINGLE FLIP-FLOPS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME	
		STD TTL	ALS	AS	H	L LS S		
Dual J-K Edge-Triggered	'73	●			● ●	A	2	
	'76					A		
	'78				● ●	A		
	'103				●			
	'106				●			
	'107	●				A		
	'108				●			
	'109	●				A		
	'112		A	●				3
	'113		A	▲		A ●		2
	'114		A	▲		A ●		3
	'114		A	▲		A ●		2
	'114		A	▲		A ●		3
	'114		A	▲		A ●		3
Single J-K Edge-Triggered	'70	●					2	
	'101				●			
	'102				●			
Dual Pulse-Triggered	'73	●			● ●		2	
	'76	●			●			
	'78	●			● ●			
	'107	●			● ●			
Single Pulse-Triggered	'71	●			● ●		2	
	'72	●			● ●			
	'104	●			● ●			
Dual J-K with Data Lockout	'111	●					2	
Single J-K with Data Lockout	'110	●						
Dual D-Type	'74	●			● ●	A ●		
			A	●			3	

QUAD AND HEX FLIP-FLOPS

DESCRIPTION	NO. OF FFs	OUTPUTS	TYPE	TECHNOLOGY					VOLUME
				STD TTL	ALS	AS	LS	S	
D Type	6	Q	'174	●			● ●		2
				'378		● ●			3
				'171				● ●	2
	4	Q, \bar{Q}	'175	●			● ●		3
				'379		● ●		●	
				'276	●				
J-K	4	Q	'376	●					
				'376	●				

OCTAL, 9-BIT, AND 10-BIT D-TYPE FLIP-FLOPS

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY					VOLUME
				STD TTL	ALS	AS	LS	S	
True Data	Octal	3-State	'374	●	●			● ●	3
				'574		B	●		2
True Data with Clear	Octal	2-State	'273	●			●		3
				'575		● ●			2
				'874	●	●			3
				'878	●	●			
True with Enable	Octal	2-State	377				●		2
				'534	●	●			
Inverting	Octal	3-State	'564	A	●				3
				'576	A	●			
				'577	A	●			
Inverting with Clear	Octal	3-State	'879	A	●				3
				'879	A	●			
Inverting with Preset	Octal	3-State	'876	A	●				3 & LSI
True	Octal	3-State	'825		●				
Inverting	Octal	3-State	'826		●				
True	9-Bit	3-State	'823		●				
Inverting	9-Bit	3-State	'824		●				
True	10-Bit	3-State	'821		●				
Inverting	10-Bit	3-State	'822		●				
True	Octal	3-State	'29825	▲					
Inverting	Octal	3-State	'29826	▲					
True	9-Bit	3-State	'29823	▲					
Inverting	9-Bit	3-State	'29824	▲					
True	10-Bit	3-State	'29821	▲					
Inverting	10-Bit	3-State	'29822	▲					

1
General Information

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FUNCTIONAL INDEX

LATCHES AND MULTIVIBRATORS

QUAD LATCHES

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY					VOLUME
			STD TTL	ALS	AS	L	LS	
Dual 2-Bit Transparent	2-State	'75	●			●	●	2
			'77	●			●	
			'375	●			●	
S R	2-State	'279	●			A		

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME	
		STD TTL	ALS	AS	LS	L		
Single		'122	●			●	●	2
		'130	●					
		'422				●		
Dual		'123	●			●	●	2
		'423				●		

D-TYPE OCTAL, 9-BIT, AND 10-BIT READ-BACK LATCHES

DESCRIPTION	NO. OF BITS	TYPE	TECHNOLOGY					VOLUME	
			STD TTL	ALS	AS	LS	S		
Edge-Triggered Inverting and Noninverting	Octal	'996		▲				3 & LSI	
				●					
Transparent True	Octal	'990		●				3 & LSI	
			9-Bit	'992		●			
					10-Bit	'994			●
Transparent Noninverting	Octal	'991		●				3 & LSI	
			9-Bit	'992		●			
					10-Bit	'994			●
Transparent with Clear True Outputs	Octal	'666		●					
Transparent with Clear Inverting Outputs	Octal	'667		●					

OCTAL, 9-BIT, AND 10-BIT LATCHES

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY					VOLUME	
				STD TTL	ALS	AS	LS	S		
Transparent	Octal	3-State	'268					●	2	
				'373				●		●
					'573		●	●		
Dual 4-Bit Transparent	Octal	2-State	'100	●					2	
				'116	●					
					'873		B	●		
Inverting Transparent	Octal	3-State	'533		●	●			3	
				'563	A					
					'580	A	●			
Dual 4-Bit Inverting Transparent	Octal	3-State	'880		A	●			2	
				2-Input Multiplexed	Octal	3-State	'604			
OC	'605								●	
OC	'606								●	
Addressable	Octal	2-State	'259		●			●	3	
						●				
Multi-Mode Buffered	Octal	3-State	'412					●	2	
True	Octal	3-State	'845		●	●			3 & LSI	
Inverting	Octal	3-State	'846		▲	●				
True	9-Bit	3-State	'843		●	●				
Inverting	9-Bit	3-State	'844		●	●				
True	10-Bit	3-State	'841		●	●				
Inverting	10-Bit	3-State	'842		●	●				

MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	LS	S	L	
Single		'121	●				●	2
Dual		'221	●			●		2

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1 General Information

REGISTERS

SHIFT REGISTERS

DESCRIPTION	NO. OF BITS	MODES				TYPE	TECHNOLOGY					VOLUME		
		SR	SR	LOAD	HOLD		STD TTL	ALS	AS	L	LS		S	
Sign-Protected		X	X	X	X	'322					A		2	
Parallel-In, Parallel-Out, Bidirectional	8	X	X	X	X	'198	●					●	●	3
		X	X	X	X	'299		●	▲					2
		X	X	X	X	'323						●		3
Parallel-In, Parallel-Out, Registered Outputs	4	X	X	X	X	'194	●				A	●	3	
		X	X	X	X	'671						●		2
Parallel-In, Parallel-Out	4	X	X	X	X	'672						●		2
		X	X	X	X	'199	●							2
		X	X	X	X	'96	●					●	●	3
		X	X			'95	A					●	B	2
		X	X			'99						●		3
		X	X	X	X	'178	●							2
		X	X	X	X	'179	●							2
Serial-In, Parallel-Out	8	X	X			'195	●				A	●	2	
		X	X			'295						B	3	
		X	X			'395					A		2	
		X	X			'673							3	
		X	X			'164	●					●	●	3
Parallel-In, Serial-Out	8	X	X	X	X	'674						●	2	
		X	X	X	X	'165	●					A	3	
		X	X	X	X	'166	●					A	2	
Serial-In, Serial-Out	4	X	X	X	X	'91	A				●	●	3	
	4	X	X	X	X	'94	●						2	

SHIFT REGISTERS WITH LATCHES

DESCRIPTION	NO. OF BITS	OUTPUTS	TYPE	TECHNOLOGY			VOLUME
				ALS	AS	LS	
Parallel-In, Parallel-Out with Output Latches	4	3 State	'671			●	2
		3 State	'672			●	
Serial-In, Parallel-Out with Output Latches	8	2-State	'673			●	2
		Buffered	'594			●	
		3-State	'595			●	
		OC	'596			●	
Parallel-In, Serial-Out, with Input Latches	8	2-State	'597			●	2
		3-State	'589			●	
Parallel I/O Ports with Input Latches, Multiplexed Serial Inputs	8	3-State	'598			●	3

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SIGN-PROTECTED REGISTERS

DESCRIPTION	NO. OF BITS	MODES			TYPE	TECHNOLOGY			VOLUME	
		SR	SR	LOAD		ALS	AS	LS		
Sign-Protected Register	8	X	X	X	'322				A	2

REGISTER FILES

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY					VOLUME		
			STD TTL	ALS	AS	L	LS		S	
8 Words x 2 Bits	3-State	'172	●							2
	OC	'170	●							
4 Words x 4 Bits	3-State	'670							●	3 & LSI
	3-State	'870							●	
Dual 16 Words x 4 Bits	3-State	'871							●	LSI
	3-State	'871							●	
64 Words x 40 Bits	3-State	'8834						▲		LSI

OTHER REGISTERS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME	
		STD TTL	ALS	AS	L	LS		S
Quadruple Multiplexers with Storage	'98					●	●	2
	'298	●					●	3
	'398					●		2
	'399					●		2
8-Bit Universal Shift Registers	'299					●	▲	3
Quadruple Bus-Buffer Registers	'173	●					A	2
Octal Storage Register	'396						●	2
Dual-Rank 8-Bit Shift Registers	'963					▲		3 & LSI
	'964					▲		
8-Bit Diagnostics/Pipeline Registers	'29818					▲		3
	'29819					▲		3

FUNCTIONAL INDEX

COUNTERS

SYNCHRONOUS COUNTERS – POSITIVE-EDGE TRIGGERED

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY						VOLUME	
			STD TTL	ALS	AS	L	LS	S		
Decade	Sync	'160	•				A		2	
				B	•				3	
	Sync	'162	•				A	•	2	
				B	•				3	
				A					3	
									2	
Decade Up/Down	Sync	'168		B	•			B	•	3
			•				•		2	
	Async	'190		•				•	3	
			•			•	•		2	
	Sync	'568			A				3	
			•					•	2	
Decade Rate Multiplier, $\frac{1}{N10}$	Async Set-to-9	'167	•						2	
			•				A		3	
4 Bit Binary	Sync	'161	•	B	•				3	
			•				A	•	2	
	Sync	'163	•	B	•				3	
				A					2	
	Sync	'561						•	2	
			•					•	2	
4 Bit Binary Up/Down	Sync	'169		B	•			B	•	3
			•				•		2	
	Async	'191		•				•	3	
			•			•	•		2	
	Sync	'569			A				3	
			•					•	2	
6-Bit Binary Rate Multiplier, $\frac{1}{N2}$	Async CLR	'97	•						2	
			•						2	
8-Bit Up/Down	Sync CLR	'867			•				3 & LSI	
			•						3 & LSI	

ASYNCHRONOUS COUNTERS (RIPPLE CLOCK) – NEGATIVE-EDGE TRIGGERED

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY						VOLUME		
			STD TTL	ALS	AS	L	LS	S			
Decade	Set-to-9	'90	A				•	•		2	
								•			
	Yes	'176	•					•	•		
			•						•		•
			•								•
4-Bit Binary	Set-to-9	'290	•						•	2	
			None	'93	A			•	•		
	Yes	'177	•						•		
			•	'197	•						•
			•	'293	•						•
Divide-by-12	None	'92	A					•			
			•	'390	•					•	
Dual Decade	Set to 9	'490	•						•		
			•	'393	•					•	

8-BIT BINARY COUNTERS WITH REGISTERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY			VOLUME
			ALS	AS	LS	
Parallel Register	3-State	'590			•	2
Outputs	OC	'591			•	
Parallel Register Inputs	2-State	'592			•	
Parallel I/O	3-State	'593			•	

FREQUENCY DIVIDERS, RATE MULTIPLIERS

DESCRIPTION	TYPE	TECHNOLOGY				VOLUME
		STD TTL	ALS	AS	LS	
50 to-1 Frequency Divider	'56				•	2
60 to-1 Frequency Divider	'57				•	
60-Bit Binary Rate Multiplier	'97	•				
Decade Rate Multiplier	'167	•				

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DECODERS, ENCODERS, DATA SELECTORS/MULTIPLEXERS AND SHIFTERS

DATA SELECTORS/MULTIPLEXERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY					VOLUME
			STD TTL	ALS	AS	L	LS	
16-to-1	2 State	'150	●					2
	3 State	'250		●				3 & LSI
	3 State	'850		●				
Dual 8-to-1	3 State	'351	●					2
	2 State	'151	A	●	●		●	3
8-to-1	2 State	'152	A			●		2
	3 State	'251	●			●	●	3
	3 State	'354				●		2
	2 State	'355		●	▲			
	3 State	'356				●		2
	OC	'357				●		
Dual 4-to-1	2 State	'153		●	●	●	●	3
	3 State	'253		●	●	●	●	2
	2 State	'352		●	●	●		3
	3 State	'353		●	●	●		2
Octal 2-to-1 with Storage	3 State	'604				●		2
	OC	'605				●		
	3 State	'606				●		2
	OC	'607				●		
Quad 2-to-1 with Storage	2 State	'98	●			●		2
	2 State	'298			●	●		3
	2 State	'398				●		2
2 State	'399				●			
Quad 2-to-1	2 State	'157		●	●	●	●	3
	2 State	'158		●	●	●	●	2
	3 State	'257		●	●		●	3
	3 State	'258		A	●		●	2
6-to-1 Universal Multiplexer	3 State	'857		●	●			3

DECODERS/DEMULTIPLEXERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY					VOLUME
			STD TTL	ALS	AS	L	LS	
4-to-16	3 State	'154	●			●		2
	OC	'159	●					
4-to-10 BCD-to-Decimal	2 State	'42	A			●	●	2
4-to-10 Excess 3-to-Decimal	2 State	'43	A			●		
4-to-10 Excess 3-Gray-to-Decimal	2 State	'44	A			●		3
3-to-8 with Address Latches	2 State	'131		●	▲			
	2 State	'137		●	▲			2
3-to-8	2 State	'138		●	▲			3
	3 State	'538		▲			●	3
Dual 2-to-4	2 State	'139		▲	●		A	●
	2 State	'155	●				A	●
Dual 1-to-4 Decoders	OC	'156	●				A	●
Dual 1-to-4 Decoders	3 State	'539		▲			●	3

CODE CONVERTERS

DESCRIPTION	TYPE	TECHNOLOGY		VOLUME
		STD TTL	S	
6-Line BCD to 6-Line Binary, or 4-Line to 4-Line BCD 9's/BCD 10's Converters	'184	●		~ 2
6-Bit Binary to 6-Bit BCD Converters	'185	A		4
BCD-to-Binary Converters	'484		A	
Binary-to-BCD Converters	'485		A	

PRIORITY ENCODERS/REGISTERS

DESCRIPTION	TYPE	TECHNOLOGY			VOLUME
		STD TTL	ALS	LS	
Full BCD	'147	●		●	2
Cascadable Octal	'148	●		●	
Cascadable Octal with 3-State Outputs	'348			●	
4-Bit Cascadable with Registers	'278	●			

SHIFTERS

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY					VOLUME
			STD TTL	ALS	AS	L	LS	
4-Bit Shifter	3 State	'350					●	2
Parallel 16-Bit Multi-Mode Barrel Shifter	3 State	'897			●			LSI
32-Bit Barrel Shifter	3 State	8838			▲			

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General Information

DISPLAY DECODERS/DRIVERS, MEMORY/MICROPROCESSOR CONTROLLERS, AND VOLTAGE-CONTROLLED OSCILLATORS

OPEN-COLLECTOR DISPLAY DECODERS/DRIVERS

DESCRIPTION	OFF-STATE OUTPUT VOLTAGE	TYPE	TECHNOLOGY					VOLUME
			STD TTL	ALS	AS	L	LS	
BCD-to-Decimal	30 V	'45	•					2
	60 V	'141	•					
	15 V	'145	•				•	
	7 V	'445	•				•	
BCD-to-Seven-Segment	30 V	'46	A				•	2
	15 V	'47	A				•	
	5.5 V	'48	•				•	
	5.5 V	'49	•				•	
	30 V	'246	•				•	
	15 V	'247	•				•	
	7 V	'347	•				•	
	7 V	'447	•				•	
	5.5 V	'248	•				•	
5.5 V	'249	•				•		

MEMORY/MICROPROCESSOR CONTROLLERS

DESCRIPTION	TYPE		TECHNOLOGY				VOLUME
			ALS	AS	LS	S	
System Controllers (Universal or for '888)		'890	•				LSI
Memory Refresh Controllers	Transparent, Burst Modes	4K, 16K	'600			A	2
		64K	'601			A	
	Cycle Steal, Burst Modes	4K, 16K	'602			A	
		64K	'603			A	
Memory Cycle Controller		'608			•		
Memory Mappers	3-State	'612			•	LSI	
	OC	'613			•		
Memory Mappers with Output Latches	3-State	'610			•	LSI	
	OC	'611			•		
Multi-Mode Latches (8080A Applications)		'412				•	2
		16K, 64K, 256K	'2967	▲			
Dynamic Memory Controllers		'2968	▲				LSI
		16K, 64K	'6301	▲			
		256K, 1 MEG	'6302	▲			

OPEN COLLECTOR DISPLAY DECODERS/DRIVERS WITH COUNTERS/LATCH

DESCRIPTION	TYPE	TECHNOLOGY			VOLUME
		STD TTL	ALS	AS	
BCD Counter/4-Bit Latch/BCD-to-Decimal Decoder/Driver	'142	•			2
BCD Counter/4-Bit Latch/BCD-to-Seven-Segment Decoder/LED Driver	'143	•			
BCD Counter/4-Bit Latch/BCD-to-Seven-Segment Decoder/Lamp Driver	'144	•			

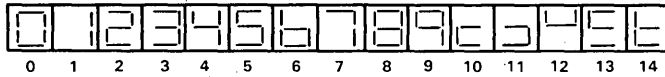
CLOCK GENERATOR CIRCUITS

DESCRIPTION	TYPE		TECHNOLOGY					VOLUME
			STD TTL	ALS	AS	LS	S	
Quadruple Complementary-Output Logic Elements		'265	•					2
Dual Pulse Synchronizers/Drivers		'120	•					
Crystal-Controlled Oscillators		'320				•	2	
		'321				•		
Digital Phase-Lock Loop		'297				•	3	
Programmable Frequency Dividers/Digital Timers		'292				•		
		'294				•		
Triple 4-Input AND/NAND Drivers		'800				▲	3	
Triple 4-Input OR/NOR Drivers		'802				▲		
Dual VCO		'124					•	2

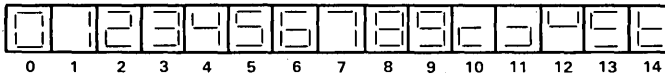
VOLTAGE-CONTROLLED OSCILLATORS

DESCRIPTION							TECHNOLOGY			VOLUME
No. VCOs	COMPL ZOUT	ENABLE	RANGE INPUT	R _{ext}	f _{max} MHz	TYPE	LS	S		
Single	Yes	Yes	No	Yes	20	'624	•		2	
Single	Yes	Yes	Yes	Yes	20	'628	•			
Dual	No	Yes	Yes	No	60	'124		•		
Dual	Yes	Yes	No	No	20	'626	•			
Dual	No	No	No	No	20	'627	•			
Dual	No	Yes	Yes	No	20	'629	•			

RESULTANT DISPLAYS USING '46A, '47A, '48, '49, 'L46, 'L47, 'LS47, 'LS48, 'LS49, 'LS347



RESULTANT DISPLAYS USING '246, '247, '248, '249, 'LS247, 'LS248, 'LS249, 'LS447



RESULTANT DISPLAYS USING '143, '144



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COMPARATORS AND ERROR DETECTION CIRCUITS

4-BIT COMPARATORS

DESCRIPTION					TECHNOLOGY					VOLUME	
P=Q	P>Q	P<Q	OUTPUT ENABLE	TYPE	STD TTL	ALS	AS	L	LS		S
Yes	Yes	No	2-State	No	'85	●		●	●	●	2

8-BIT COMPARATORS

INPUTS		DESCRIPTION				TECHNOLOGY					VOLUME	
		P=Q	P=Q	P>Q	P<Q	OUTPUT ENABLE	TYPE	ALS	AS	LS		
20 kΩ Pull-Up	Yes	No	No	No	No	OC	Yes	'518	●			3
	No	Yes	No	No	No	2-S	Yes	'520	●			
	No	Yes	No	No	No	OC	Yes	'522	●			
	No	Yes	No	Yes	No	2-S	No	'682			●	2
	No	Yes	No	Yes	No	OC	No	'683			●	
	Yes	No	No	No	No	OC	Yes	'519	●			
No	Yes	No	No	No	2-S	Yes	'521	●				
No	Yes	No	Yes	No	2-S	No	'684			●		
Standard	No	Yes	No	Yes	No	OC	No	'685			●	2
	No	Yes	No	Yes	No	2-S	Yes	'686			●	
	No	Yes	No	Yes	No	OC	Yes	'687			●	
	No	Yes	No	No	No	2-S	Yes	'688	●			3
	No	Yes	No	No	No	2-S	Yes	'689	●			
	No	Yes	No	No	No	OC	Yes	'689	●			
Latched P Logic & Arith	No	No	Yes	No	Yes	2-S	Yes	'885		●	3 & LSI	
Latched P&Q Logic & Arith	Yes	No	Yes	No	Yes	Latched	Yes	'886		●	3	

ADDRESS COMPARATORS

DESCRIPTION	OUTPUT ENABLE	LATCHED OUTPUT	TYPE	TECHNOLOGY		VOLUME
				ALS	AS	
16-Bit to 4-Bit	Yes			'677	●	3
		Yes		'678	●	
12-Bit to 4-Bit	Yes			'679	●	
		Yes		'680	●	

PARITY GENERATORS/CHECKERS, ERROR DETECTION AND CORRECTION CIRCUITS

DESCRIPTION	NO. OF BITS	TYPE	TECHNOLOGY					VOLUME
			STD TTL	ALS	AS	LS	S	
Odd/Even Parity Generators/Checkers	8	'180	●					2
	9	'280		●	●	●	●	3 & LSI
	9	'286			●			
Parallel Error Detection/Correction Circuits	3-State	8	'636				●	2
	OC	8	'637				●	
	3-State	16	'616		●			3 & LSI
	OC	16	'617		▲			
	3-State	16	'630				●	2
	OC	16	'631				●	
	3-State	16	'8400		▲			LSI
	3-State	32	'632		▲	▲		3 & LSI
	OC	32	'633		▲	▲		
	3-State	32	'634		▲	▲		
OC	32	'635		▲	▲			

FUSE PROGRAMMABLE COMPARATORS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
16 Bit Identity Comparator	'526		●				3
12-Bit Identity Comparator	'528		●				
8-Bit Identity Comparator			●				
and 4-Bit Comparator	'527		●				

General Information

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- ▲ Denotes planned new products.
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ARITHMETIC CIRCUITS AND PROCESSOR ELEMENTS

PARALLEL BINARY ADDERS

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	H	LS	S	
1-Bit Gated	'80	●						2
2 Bit	'82	●						
4 Bit	'83	A				A		
	'283	●				●	●	
Dual 1-Bit Carry-Save	'183					●	●	

OTHER ARITHMETIC OPERATORS

DESCRIPTION	TYPE	TECHNOLOGY								VOLUME
		STD TTL	ALS	AS	H	L	LS	S		
Quad 2-Input Exclusive-OR Gates with Totem-Pole Outputs	'86	●				●	A	●		2
	'386		●				A			3
Quad 2-Input Exclusive-OR Gates with Open Collector Outputs	'136	●						●		2
			●							3
Quad 2-Input Exclusive-NOR Gates	'266							●		2
	'810		●	▲						3
Quad 2-Input Exclusive-NOR Gates with Open Collector Outputs	'811		●	▲						3
Quad Exclusive-OR/NOR Gates	'135							●		2
4 Bit True/Complement Element	'87					●				

ACCUMULATORS, ARITHMETIC LOGIC UNITS, LOOK-AHEAD CARRY GENERATORS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
4-Bit Parallel Binary Accumulators	'281					●	2
	'681					●	
	'181	●				●	
4 Bit Arithmetic Logic Units Function Generators	'1181			A			3 & LSI
	'381				A		2
	'881			A			3 & LSI
4 Bit Arithmetic Logic Unit with Ripple Carry	'382					●	2
			●			●	2
Look Ahead Carry Generators	16 Bit	'182			▲		3
		'282			▲		
	32 Bit	'882			A		3 & LSI
Quad Serial Adder/Subtractor	'385					●	2

BIPOLAR BIT-SLICE PROCESSOR ELEMENTS

DESCRIPTION	CASCADABLE TO N-BITS	TYPE	TECHNOLOGY				VOLUME
			ALS	AS	LS	S	
8-Bit Slice	No	'887		●			LSI
	Yes	'888		●			
	Yes	'895		▲			

MULTIPLIERS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
2-Bit-by-4-Bit Parallel Binary Multipliers	'261					●	2
4 Bit-by-4 Bit Parallel Binary Multipliers	'284	●					
	'285	●					
25-MHz 6-Bit Binary Rate Multipliers	'97	●					
25-MHz Decade Rate Multipliers	'167	●					
8-Bit x 1-Bit 2's Complement Multipliers	'384					●	

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1 General Information

MEMORIES

USER-PROGRAMMABLE READ-ONLY MEMORIES (PROMs)
STANDARD PROMs

DESCRIPTION	TYPE	ORGANIZATION	TYPE OUTPUT	S	VOLUME
16K-Bit Arrays	TBP28S166	2048W x 8B	3-State	●	4
	TBP38S165	2048W x 8B	3-State	●	
	TBP38S166	2048W x 8B	3-State	●	
	TBP38SA165	2048W x 8B	OC	●	
	TBP38SA166	2048W x 8B	OC	●	
	TBP34S162	4096W x 4B	3-State	●	
8K-Bit Arrays	TBP24S81	2048W x 4B	3-State	●	4
	TBP24SA81	2048W x 4B	OC	●	
	TBP28S85A	1024W x 8B	3-State	▲	
	TBP28S86A	1024W x 8B	3-State	●	
	TBP28SA85A	1024W x 8B	OC	●	
	TBP38S85	1024W x 8B	3-State	▲	
4K-Bit Arrays	TBP38S86	1024W x 8B	3-State	▲	4
	TBP38SA85	1024W x 8B	OC	▲	
	TBP38SA86	1024W x 8B	OC	▲	
	TBP24S41	1024W x 4B	3-State	●	
	TBP24SA41	1024W x 4B	OC	●	
	TBP28S42	512W x 8B	3-State	●	
2K-Bit Arrays	TBP28SA42	512W x 8B	OC	●	4
	TBP28S46	512W x 8B	3-State	●	
	TBP28SA46	512W x 8B	OC	●	
	TBP38S22	256W x 8B	3-State	●	
	TBP38SA22	256W x 8B	OC	●	
	1K-Bit Arrays	TBP24S10	256W x 4B	3-State	
TBP24SA10		256W x 4B	OC	●	
TBP34S10		256W x 4B	3-State	●	
TBP34SA10		256W x 4B	OC	●	
256-Bit Arrays	TBP18S030	32W x 8B	3-State	●	4
	TBP18SA030	32W x 8B	OC	●	
	TBP38S030	32W x 8B	3-State	●	
	TBP38SA030	32W x 8B	OC	●	

LOW-POWER PROMs

DESCRIPTION	TYPE	ORGANIZATION	TYPE OUTPUT	S	VOLUME
16K-Bit Arrays	TBP28L166	2048W x 8B	3-State	●	4
	TBP38L165	2048W x 8B	3-State	●	
	TBP38L166	2048W x 8B	3-State	●	
	TBP34L162	4096W x 4B	3-State	▲	
8K-Bit Arrays	TBP28L85A	1024W x 8B	3-State	▲	4
	TBP28L86A	1024W x 8B	3-State	●	
	TBP38L85	1024W x 8B	3-State	▲	
	TBP38L86	1024W x 8B	3-State	▲	
4K-Bit Arrays	TBP28L42	512W x 8B	3-State	●	4
	TBP28L46	512W x 8B	3-State	●	
2K-Bit Arrays	TBP28L22	256W x 8B	3-State	●	4
	TBP28LA22	256W x 8B	OC	●	
1K-Bit Arrays	TBP38L22	256W x 8B	3-State	▲	4
1K-Bit Arrays	TBP34L10	256W x 4B	3-State	●	4
256-Bit Arrays	TBP38L030	32W x 8B	3-State	▲	4

REGISTERED PROMs

DESCRIPTION	TYPE	ORGANIZATION	TYPE OUTPUT	S	VOLUME
16K-Bit Arrays	TBP34R162	4096W x 4B	3-State	●	4
	TBP34SR165	4096W x 4B	3-State	▲	
	TBP38R165	2048W x 8B	3-State	●	

RANDOM-ACCESS READ-WRITE MEMORIES (RAMs)

DESCRIPTION	ORGANIZATION	TYPE OF OUTPUT	TYPE	TECHNOLOGY					VOLUME	
				STD TTL	ALS	AS	LS	S		
256-Bit Arrays	256 x 1	3-State	'201						●	4
		OC	'301						●	
64-Bit Arrays	16 x 4	OC	'89	●						4
		3-State	'189				A	B		
		3-State	'219					A		
		OC	'289					A	B	
		OC	'319						A	
16-Bit Multiple-Port Register File	8 x 2	3-State	'172	●						2
16-Bit Register File	4 x 4	OC	'170	●						2
		3-State	'670						●	
Dual 64-Bit Register Files	16 x 4	3-State	'871						●	3

FIRST-IN FIRST-OUT MEMORIES (FIFOs)

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY					VOLUME
			ALS	AS	LS	S		
16 x 4	3-State	222				●	LSI	
		224				●		
		227				●		
		228				●		
		228				●		
16 x 5	3-State	232	A				3 & LSI	
		225				●	LSI	
		229	A				3 & LSI	
		233	A				3 & LSI	

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General Information

PROGRAMMABLE LOGIC ARRAYS

PROGRAMMABLE LOGIC ARRAYS

DESCRIPTION	INPUTS	OUTPUTS		TYPE NO	ALS	NO. OF PINS	VOLUME
		NO.	TYPE				
Impact PAL*	16	8	Active-Low	*TIBPAL16L8-15	●	20	
		4		*TIBPAL16R4-15	●		
		6	Registered	*TIBPAL16R6-15	●		
		8		*TIBPAL16R8-15	●		
High-Performance PAL*	16	8	Active-Low	*TIBPAL16L8A	●	20	
		4		*TIBPAL16R4A	●		
		6	Registered	*TIBPAL16R6A	●		
		8		*TIBPAL16R8A	●		
Half-Power PAL*	16	8	Active-Low	*TIBPAL16L8A-2	●	20	
		4		*TIBPAL16R4A-2	●		
		6	Registered	*TIBPAL16R6A-2	●		
		8		*TIBPAL16R8A-2	●		
High-Performance PAL*	20	8	Active-Low	*PAL20L8A	▲	24	
		4		*PAL20R4A	▲		
		6	Registered	*PAL20R6A	▲		
		8		*PAL20R8A	▲		
Half-Power PAL*	20	8	Active-Low	*PAL20L8A-2	▲	24	
		4		*PAL20R4A-2	▲		
		6	Registered	*PAL20R6A-2	▲		
		8		*PAL20R8A-2	▲		
Exclusive-OR PAL*	20	10	Active-Low	*TIBPAL20L10-20	●	24	4
		4		*TIBPAL20X4-20	●		
		8	Registered	*TIBPAL20X8-20	●		
		10		*TIBPAL20X10-20	●		
Exclusive-OR PAL*	20	8	Active-Low	*TIBPAL20L10-35	●	24	
		4		*TIBPAL20X4-35	●		
		8	Registered	*TIBPAL20X8-35	●		
		10		*TIBPAL20X10-35	●		
Registered-input PAL*	19	8	Active-Low	*TIBPALR19L8-25	●	24	
		4		*TIBPALR19R4-25	●		
		6	Registered	*TIBPALR19R6-25	●		
		8		*TIBPALR19R8-25	●		
Registered-input PAL*	19	8	Active-Low	*TIBPALR19L8-40	●	24	
		4		*TIBPALR19R4-40	●		
		6	Registered	*TIBPALR19R6-40	●		
		8		*TIBPALR19R8-40	●		
Latched-input PAL*	19	8	Active-Low	*TIBPALT19L8-25	●	24	
		4		*TIBPALT19R4-25	●		
		6	Registered	*TIBPALT19R6-25	●		
		8		*TIBPALT19R8-25	●		
Latched-input PAL*	19	8	Active-Low	*TIBPALT19L8-40	●	24	
		4		*TIBPALT19R4-40	●		
		6	Registered	*TIBPALT19R6-40	●		
		8		*TIBPALT19R8-40	●		
Field-Programmable 14 x 32 x 6 Logic Arrays	14	6	3-State	*TIFPLA839	●	24	
			OC	*TIFPLA840	●		

* PAL is a registered trademark of Monolithic Memories Incorporated.

- Denotes available technology.
- ▲ Denotes planned new products.

General Information

1

Numerical Index

Glossary

Explanation of Function Tables

Parameter Measurement Information

Functional Index

LSI Devices

2

Application Reports

3

Advanced Schottky Family

Error Detection and Correction

Memory Mapping

Bit-Slice Processor 8-Bit Family

Excerpt — SN74AS888, SN74AS890

Bit-Slice Processor User's Guide

Mechanical Data

4

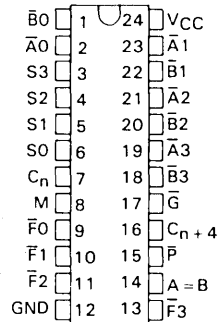
SN54AS181A, SN54AS881A, SN74AS181A, SN74AS881A ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

D2661, DECEMBER 1982—REVISED AUGUST 1985

- Package Options Include the 'AS181A in Compact 300-mil or Standard 600-mil DIPs. The 'AS881A is Offered in 300-mil DIPs. Both Devices are Available in Both Plastic and Ceramic Chip Carriers
- Full Look-Ahead for High-Speed Operations on Long Words
- Arithmetic Operating Modes:
 - Addition
 - Subtraction
 - Shift Operand A One Position
 - Magnitude Comparison
 - Plus Twelve Other Arithmetic Operations
- Logic Function Modes
 - Exclusive-OR
 - Comparator
 - AND, NAND, OR, NOR
 - 'AS881A Provides Status Register Checks
 - Plus Ten Other Logic Operations
- Dependable Texas Instruments Quality and Reliability

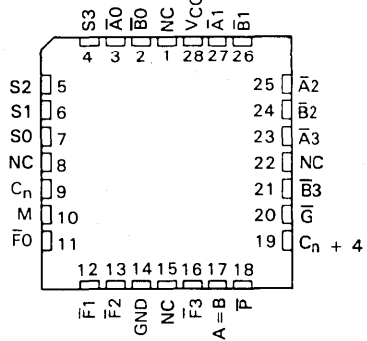
SN54AS181A . . . JT OR JW PACKAGE
SN54AS881A . . . JT PACKAGE
SN74AS181A . . . NT OR NW PACKAGE
SN74AS881A . . . NT PACKAGE

(TOP VIEW)



SN54AS181A, SN54AS881A . . . FK PACKAGE
SN74AS181A, SN74AS881A . . . FN PACKAGE

(TOP VIEW)

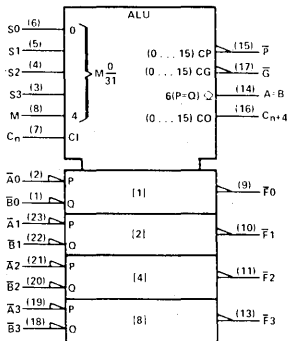


NC—No internal connection

2

LSI Devices

logic symbol



Pin numbers shown are JT, JW, NT, and NW packages.

TYPICAL ADDITION TIMES ($C_L = 15 \text{ pF}$, $R_L = 280 \Omega$, $T_A = 25^\circ\text{C}$)

NUMBER OF BITS	ADDITION TIMES			PACKAGE COUNT		CARRY METHOD BETWEEN ALUS
	USING 'AS881A AND 'AS882	USING 'AS181A AND 'AS882	USING 'S181 AND 'S182	ARITHMETIC LOGIC UNITS	LOOK-AHEAD CARRY GENERATORS	
1 to 4	5 ns	5 ns	11 ns	1		NONE
5 to 8	10 ns	10 ns	18 ns	2		RIPPLE
9 to 16	14 ns	14 ns	19 ns	3 or 4	1	FULL LOOK-AHEAD
17 to 64	19 ns	19 ns	28 ns	5 to 16	2 to 5	FULL LOOK-AHEAD

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SN54AS181A, SN54AS881A, SN74AS181A, SN74AS881A ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

description

The 'AS181A and 'AS881A are arithmetic logic units (ALU)/function generators that have a complexity of 75 and 77 equivalent gates, respectively, on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the SN54AS882 or SN74AS882 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown previously illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading 'AS882 circuits with these ALUs to provide multilevel full carry look-ahead is illustrated under signal designations.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The 'AS181A and 'AS881A will accommodate active-high or active-low data if the pin designations are interpreted as follows:

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-low data (Table 1)	$\bar{A}0$	$\bar{B}0$	$\bar{A}1$	$\bar{B}1$	$\bar{A}2$	$\bar{B}2$	$\bar{A}3$	$\bar{B}3$	F0	F1	F2	F3	C_n	C_{n+4}	\bar{P}	\bar{G}
Active-high data (Table 2)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	C_n	C_{n+4}	X	Y

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is $A-B-1$, which requires an end-around or forced carry to provide $A-B$.

The 'AS181A and 'AS881A can also be utilized as a comparator. The $A=B$ output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality ($A=B$). The ALU must be in the subtract mode with $C_n=H$ when performing this comparison. The $A=B$ output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select input S3, S2, S1, S0 at L, H, H, L, respectively.

INPUT C_n	OUTPUT C_{n+4}	ACTIVE-LOW DATA (FIGURE 1)	ACTIVE-HIGH DATA (FIGURE 2)
H	H	$A \geq B$	$A \leq B$
H	L	$A < B$	$A > B$
L	H	$A > B$	$A < B$
L	L	$A \leq B$	$A \geq B$

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

SN54AS181A, SN54AS881A, SN74AS181A, SN74AS881A

ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

description (continued)

The 'AS881A has the same pinout and same functionality as the 'AS181A except for the \bar{P} , \bar{G} , and C_{n+4} outputs when the device is in the logic mode ($M=H$).

In the logic mode the 'AS881A provides the user with a status check on the input words A and B, and the output word F. While in the logic mode the \bar{P} , \bar{G} , and C_{n+4} outputs supply status information based upon the following logical combinations:

$$\begin{aligned}\bar{P} &= F_0 + F_1 + F_2 + F_3 \\ \bar{G} &= H \\ C_{n+4} &= PC_n\end{aligned}$$

FUNCTION TABLE FOR INPUT BITS EQUAL/NOT EQUAL

S0=S3=H, S1=S2=L, and M=H

C _n	DATA INPUTS				OUTPUTS		
	$\bar{A}_0=\bar{B}_0$	$\bar{A}_1=\bar{B}_1$	$\bar{A}_2=\bar{B}_2$	$\bar{A}_3=\bar{B}_3$	\bar{G}	\bar{P}	C _{n+4}
H	$\bar{A}_0=\bar{B}_0$	$\bar{A}_1=\bar{B}_1$	$\bar{A}_2=\bar{B}_2$	$\bar{A}_3=\bar{B}_3$	H	L	H
L	$\bar{A}_0=\bar{B}_0$	$\bar{A}_1=\bar{B}_1$	$\bar{A}_2=\bar{B}_2$	$\bar{A}_3=\bar{B}_3$	H	L	L
X	$\bar{A}_0 \neq \bar{B}_0$	X	X	X	H	H	L
X	X	$\bar{A}_1 \neq \bar{B}_1$	X	X	H	H	L
X	X	X	$\bar{A}_2 \neq \bar{B}_2$	X	H	H	L
X	X	X	X	$\bar{A}_3 \neq \bar{B}_3$	H	H	L

FUNCTION TABLE FOR INPUT PAIRS HIGH/NOT HIGH

S0=S1=S3=L, S2=H, and M=H

C _n	DATA INPUTS				OUTPUTS		
	\bar{A}_0 or $\bar{B}_0 = L$	\bar{A}_1 or $\bar{B}_1 = L$	\bar{A}_2 or $\bar{B}_2 = L$	\bar{A}_3 or $\bar{B}_3 = L$	\bar{G}	\bar{P}	C _{n+4}
H	\bar{A}_0 or $\bar{B}_0 = L$	\bar{A}_1 or $\bar{B}_1 = L$	\bar{A}_2 or $\bar{B}_2 = L$	\bar{A}_3 or $\bar{B}_3 = L$	H	L	H
L	\bar{A}_0 or $\bar{B}_0 = L$	\bar{A}_1 or $\bar{B}_1 = L$	\bar{A}_2 or $\bar{B}_2 = L$	\bar{A}_3 or $\bar{B}_3 = L$	H	L	L
X	$\bar{A}_0 = \bar{B}_0 = H$	X	X	X	H	H	L
X	X	$\bar{A}_1 = \bar{B}_1 = H$	X	X	H	H	L
X	X	X	$\bar{A}_2 = \bar{B}_2 = H$	X	H	H	L
X	X	X	X	$\bar{A}_3 = \bar{B}_3 = H$	H	H	L

The combination of signals on the S3 through S0 control lines determine the operation performed on the data words to generate the output bits \bar{F}_i . By monitoring the \bar{P} and C_{n+4} outputs, the user can determine if all pairs of input bits are equal (see table above) or if any pair of inputs are both high (see table above). The 'AS881A has the unique feature of providing an $A = B$ status while the exclusive-OR(\oplus) function is being utilized. When the control inputs (S3, S2, S1, S0) equal H, L, L, H; a status check is generated to determine whether all pairs (\bar{A}_i, \bar{B}_i) are equal in the following manner: $\bar{P} = (\bar{A}_0 \oplus \bar{B}_0) + (\bar{A}_1 \oplus \bar{B}_1) + (\bar{A}_2 \oplus \bar{B}_2) + (\bar{A}_3 \oplus \bar{B}_3)$. This unique bit-by-bit comparison of the data words, which is available on the totem-pole \bar{P} output, is particularly useful when cascading 'AS881s. As the $A = B$ condition is sensed in the first stage, the signal is propagated through the same ports used for carry generation in the arithmetic mode (\bar{P} and \bar{G}). Thus the $A = B$ status is transmitted to the second stage more quickly without the need for external multiplexing logic. The $A = B$ open-collector output allows the user to check the validity of the bit-by-bit result by comparing the two signals for parity.

If the user wishes to check for any pair of data inputs (\bar{A}_i, \bar{B}_i) being high, it is necessary to set the control lines (S3,S2,S1,S0) to L, H, L, L. The data pairs will then be ANDed together and the results ORed in the following manner: $\bar{P} = \bar{A}_0\bar{B}_0 + \bar{A}_1\bar{B}_1 + \bar{A}_2\bar{B}_2 + \bar{A}_3\bar{B}_3$.

S3	S2	S1	S0	M	$\bar{P} = F_0 + F_1 + F_2 + F_3$
L	H	L	L	H	$\bar{A}_0\bar{B}_0 + \bar{A}_1\bar{B}_1 + \bar{A}_2\bar{B}_2 + \bar{A}_3\bar{B}_3$
H	L	L	H	H	$(\bar{A}_0 \oplus \bar{B}_0) + (\bar{A}_1 \oplus \bar{B}_1) + (\bar{A}_2 \oplus \bar{B}_2) + (\bar{A}_3 \oplus \bar{B}_3)$

signal designations

In both Figures 1 and 2, the polarity indicators (∇) indicate that the associated input or output is active-low with respect to the function shown inside the symbol and the symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data, and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accommodate the logic functions and arithmetic operations for the active-high data given in Table 2. The 'AS181A and 'AS881A together with 'AS882 and 'S182 can be used with the signal designation of either Figure 1 or Figure 2.

2
LSI Devices

SN54AS181A, SN54AS881A, SN74AS181A, SN74AS881A ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

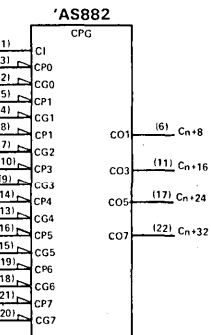
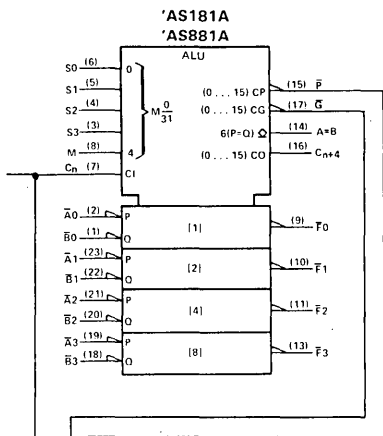


FIGURE 1
(USE WITH TABLE 1)

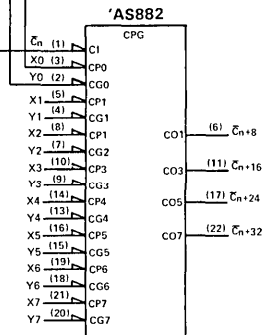
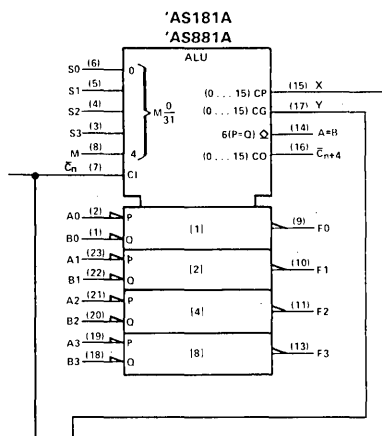


FIGURE 2
(USE WITH TABLE 2)

TABLE 1

SELECTION S3 S2 S1 S0	ACTIVE-LOW DATA			
	M = H LOGIC FUNCTIONS	M = L; ARITHMETIC OPERATIONS		F = A
		C _n = L (no carry)	C _n = H (with carry)	
L L L L	F = \bar{A}	F = A MINUS 1	F = A	
L L L H	F = $\bar{A}\bar{B}$	F = AB MINUS 1	F = AB	
L L H L	F = $\bar{A} + \bar{B}$	F = \bar{A} MINUS 1	F = $\bar{A}\bar{B}$	
L L H H	F = 1	F = MINUS 1 (2's COMPL)	F = ZERO	
L H L L	F = $\bar{A} + \bar{B}$	F = A PLUS (A + \bar{B}) PLUS 1	F = A PLUS (A + \bar{B}) PLUS 1	
L H L H	F = \bar{B}	F = AB PLUS (A + \bar{B})	F = AB PLUS (A + \bar{B}) PLUS 1	
L H H L	F = A \odot B	F = A MINUS B MINUS 1	F = A MINUS B	
L H H H	F = A + \bar{B}	F = A + \bar{B}	F = (A + \bar{B}) PLUS 1	
H L L L	F = $\bar{A}\bar{B}$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1	
H L L H	F = A \odot B	F = A PLUS B	F = A PLUS B PLUS 1	
H L H L	F = B	F = $\bar{A}\bar{B}$ PLUS (A + B)	F = $\bar{A}\bar{B}$ PLUS (A + B) PLUS 1	
H L H H	F = A + B	F = (A + B)	F = (A + B) PLUS 1	
H H L L	F = 0	F = A PLUS A [†]	F = A PLUS A PLUS 1	
H H L H	F = $\bar{A}\bar{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1	
H H H L	F = AB	F = $\bar{A}\bar{B}$ PLUS A	F = $\bar{A}\bar{B}$ PLUS A PLUS 1	
H H H H	F = A	F = A	F = A PLUS 1	

TABLE 2

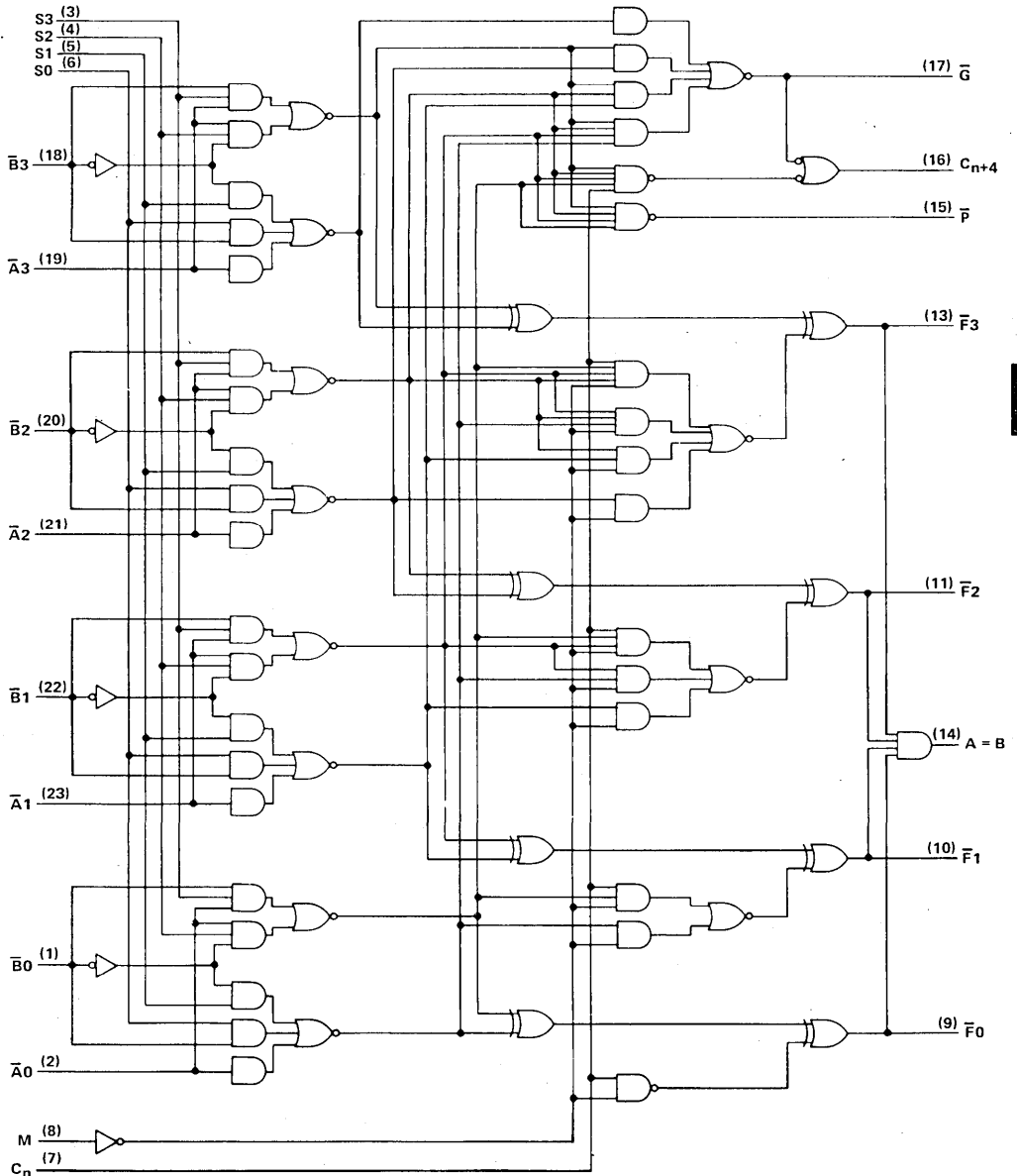
SELECTION S3 S2 S1 S0	ACTIVE-HIGH DATA			
	M = H LOGIC FUNCTIONS	M = L; ARITHMETIC OPERATIONS		F = A PLUS 1
		C _n = H (no carry)	C _n = L (with carry)	
L L L L	F = A	F = A	F = A PLUS 1	
L L L H	F = $\bar{A} + \bar{B}$	F = A + B	F = (A + B) PLUS 1	
L L H L	F = $\bar{A}\bar{B}$	F = A + \bar{B}	F = (A + \bar{B}) PLUS 1	
L L H H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO	
L H L L	F = $\bar{A}\bar{B}$	F = A PLUS $\bar{A}\bar{B}$	F = A PLUS $\bar{A}\bar{B}$ PLUS 1	
L H L H	F = \bar{B}	F = (A + B) PLUS $\bar{A}\bar{B}$	F = (A + B) PLUS $\bar{A}\bar{B}$ PLUS 1	
L H H L	F = A \odot B	F = A MINUS B MINUS 1	F = A MINUS B	
L H H H	F = $\bar{A}\bar{B}$	F = $\bar{A}\bar{B}$ MINUS 1	F = $\bar{A}\bar{B}$	
H L L L	F = $\bar{A} + \bar{B}$	F = A PLUS AB	F = A PLUS AB PLUS 1	
H L L H	F = A \odot B	F = A PLUS B	F = A PLUS B PLUS 1	
H L H L	F = B	F = (A + \bar{B}) PLUS AB	F = (A + \bar{B}) PLUS AB PLUS 1	
H L H H	F = AB	F = AB MINUS 1	F = AB	
H H L L	F = 1	F = A PLUS A [†]	F = A PLUS A PLUS 1	
H H L H	F = A + \bar{B}	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1	
H H H L	F = A + B	F = (A + \bar{B}) PLUS A	F = (A + \bar{B}) PLUS A PLUS 1	
H H H H	F = A	F = A MINUS 1	F = A	

[†]Each bit is shifted to the next more significant position.

SN54AS181A, SN74AS181A
 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

logic diagram (positive logic)

'AS181A

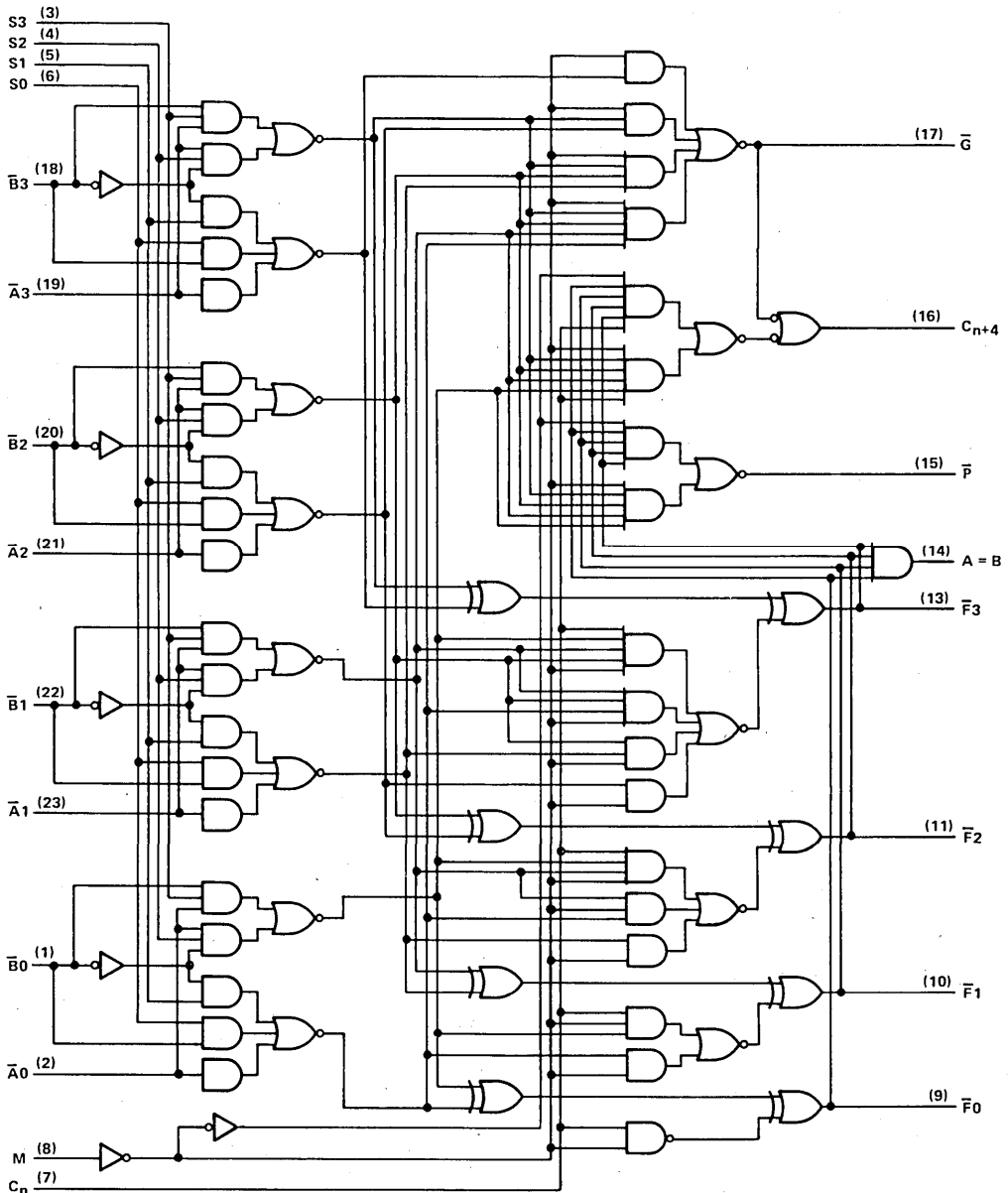


2
 LSI Devices

SN54AS881A, SN74AS881A
 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

logic diagram (positive logic)

'AS881A



2

LSI Devices

SN54AS181A, SN54AS881A, SN74AS181A, SN74AS881A ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Off-state output voltage (A = B output only)	7 V
Operating free-air temperature range: SN54AS181A, SN54AS881A	- 55°C to 125°C
SN74AS181A, SN74AS881A	0°C to 70°C
Storage temperature range	- 65°C to 150°C

recommended operating conditions

			SN54AS'			SN74AS'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage					0.8			V
V_{OH}	High-level output voltage	A = B output only				5.5			V
I_{OH}	High-level output current	All outputs except A = B and \overline{G}				- 2			mA
		\overline{G}				- 3			mA
I_{OL}	Low-level output current	All outputs except \overline{G}				20			mA
		\overline{G}				48			mA
T_A	Operating free-air temperature		- 55	125		0	70		°C

2

LSI Devices

SN54AS181A, SN54AS881A, SN74AS181A, SN74AS881A

ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS'			SN74AS'			UNIT	
		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX		
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2			-1.2	V	
V _{OH}	Any output except A = B	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -2 mA			V _{CC} -2			V	
	\bar{G}	V _{CC} = 4.5 V, I _{OH} = -3 mA	2.4	3.4	2.4	3.4		V	
I _{OH}	A = B	V _{CC} = 4.5 V, V _{OH} = 5.5 V	0.1			0.1		mA	
V _{OL}	Any output except \bar{G}	V _{CC} = 4.5 V, I _{OL} = 20 mA	0.3	0.5	0.3	0.5		V	
	\bar{G}	V _{CC} = 4.5 V, I _{OL} = 48 mA	0.4	0.5	0.4	0.5		V	
I _I	M input	V _{CC} = 5.5 V, V _I = 7 V	0.1			0.1		mA	
	Any A or B input		0.3			0.3			
	Any S input		0.4			0.4			
	Carry input		0.6			0.6			
I _{IH}	M input	V _{CC} = 5.5 V, V _I = 2.7 V	20			20		μA	
	Any A or B input		60			60			
	Any S input		80			80			
	Carry input		120			120			
I _{IL}	M input	V _{CC} = 5.5 V, V _I = 0.4 V	-2			-2		mA	
	Any A or B input		-6			-6			
	Any S input		-8			-8			
	Carry input		-12			-12			
I _O [‡]	All outputs except A = B and \bar{G}	V _{CC} = 5.5 V, V _O = 2.25 V	-30	-45	-112	-30	-45	-112	mA
	\bar{G}		-165			-165			
I _{CC}	V _{CC} = 5.5 V	'AS181A	135	200	135	200	mA		
		'AS881A	135	210	135	210			

[†]All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡]The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

SN54AS181A, SN54AS881A, SN74AS181A, SN74AS881A ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V _{CC} = 5 V, C _L = 15 pF, R _L = 500 Ω (280 Ω for A=B), T _A = 25°C		V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF (15 pF for A=B), R _L = 500 Ω (280 Ω for A=B), T _A = MIN to MAX				UNIT		
				'AS181A 'AS881A		SN54AS181A SN54AS881A		SN74AS181A SN74AS881A				
				MIN	TYP [†] MAX	MIN	TYP [†] MAX	MIN	TYP [†] MAX			
t _{pd}	C _n	C _{n+4}		5		2	7	11	2	7	9	ns
t _{pd}	Any A or B	C _{n+4}	M=0 V, S1=S2=0 V, S0=S3=4.5 V (SUM mode)	6		2	8	14	2	8	12	ns
t _{pd}	Any A or B	C _{n+4}	M=0 V, S0=S3=0 V, S1=S2=4.5 V (DIFF mode)	7		2	8	20	2	8	16	ns
t _{pd}	C _n	Any F	M=0 V (SUM or DIFF mode)	5		3	6	11	3	6	9	ns
t _{pd}	Any A or B	G	M=0 V, S1=S2=0 V, S0=S3=4.5 V (SUM mode)	4		2	5	9	2	5	7	ns
t _{pd}	Any A or B	G	M=0 V, S0=S3=0 V, S1=S2=4.5 V (DIFF mode)	5		2	6	12	2	6	9	ns
t _{pd}	Any A or B	P	M=0 V, S1=S2=0 V, S0=S3=4.5 V (SUM mode)	5		2	6	11	2	6	8	ns
t _{pd}	Any A or B	P	M=0 V, S0=S3=0 V, S1=S2=4.5 V (DIFF mode)	5		2	6	13	2	6	10	ns
t _{pd}	A _i or B _i	F _i	M=0 V, S1=S2=0 V, S0=S3=4.5 V (SUM mode)	5		2	5	11	2	5	8	ns
t _{pd}	A _i or B _i	F _i	M=0 V, S0=S1=0 V, S1=S2=4.5 V (DIFF mode)	5		2	6	12	2	6	10	ns
t _{pd}	A _i or B _i	F _i	M=4.5 V (LOGIC mode)	6		2	6	16	2	6	11	ns
t _{pd}	Any A or B	A=B	M=0 V, S0=S3=0 V, S1=S2=4.5 V (DIFF mode)	12		4	14	26	4	14	21	ns

additional 'AS881A switching characteristics involving status checks (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V _{CC} = 5 V, C _L = 15 pF, R _L = 500 Ω, T _A = 25°C		V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX				UNIT		
				'AS881A		SN54AS881A		SN74AS881A				
				MIN	TYP [†] MAX	MIN	TYP [†] MAX	MIN	TYP [†] MAX			
t _{pd}	Any A or B	P	C _n =4.5V, M=4.5 V, S0=S3=4.5 V, S1=S2=0 V, Equality (A _i =B _i or A _i ≠B _i)	8		2	10	19	2	10	15	ns
t _{pd}	Any A or B	C _{n+4}	C _n =4.5 V, M=4.5 V, S0=S3=4.5 V, S1=S2=0 V, Equality (A _i =B _i or A _i ≠B _i)	10		2	12	24	2	12	18	ns
t _{pd}	Any A or B	P	C _n =4.5 V, M=4.5 V, S2=4.5 V, S0=S1=S3=0 V, (A _i =B _i =H or A _i or B _i =L)	8		2	10	19	2	10	15	ns
t _{pd}	Any A or B	C _{n+4}	C _n =4.5 V, M=4.5 V, S2=4.5 V, S0=S1=S3=0 V, (A _i =B _i =H or A _i or B _i =L)	11		2	13	25	2	13	19	ns

t_{pd} = t_{PHL} or t_{PLH}

[†]All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

2

LSI Devices

SN54AS181A, SN54AS881A, SN74AS181A, SN74AS881A
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

PARAMETER MEASUREMENT INFORMATION

SUM MODE TEST TABLE

FUNCTION INPUTS: $S_0 - S_3 = 4.5\text{ V}$, $S_1 - S_2 = M = 0\text{ V}$

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH}	\bar{A}_i	\bar{B}_i	None	Remaining \bar{A} and \bar{B}	C_n	\bar{F}_i	In-Phase
t_{PHL}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A} and \bar{B}	C_n	\bar{F}_i	In-Phase
t_{PLH}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{P}	In-Phase
t_{PHL}	\bar{B}_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{P}	In-Phase
t_{PLH}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{B}	Remaining \bar{A} , C_n	\bar{G}	In-Phase
t_{PHL}	\bar{B}_i	None	\bar{A}_i	Remaining \bar{B}	Remaining \bar{A} , C_n	\bar{G}	In-Phase
t_{PLH}	C_n	None	None	All \bar{A}	All \bar{B}	Any \bar{F} or C_{n+4}	In-Phase
t_{PHL}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{B}	Remaining \bar{A} , C_n	C_{n+4}	Out-of-Phase
t_{PHL}	\bar{B}_i	None	\bar{A}_i	Remaining \bar{B}	Remaining \bar{A} , C_n	C_{n+4}	Out-of-Phase

DIFF MODE TEST TABLE

FUNCTION INPUTS: $S_1 - S_2 = 4.5\text{ V}$, $S_0 - S_3 = M = 0\text{ V}$

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{A}	Remaining \bar{B} , C_n	\bar{F}_i	In-Phase
t_{PHL}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A}	Remaining \bar{B} , C_n	\bar{F}_i	Out-of-Phase
t_{PLH}	\bar{A}_i	None	\bar{B}_i	None	Remaining \bar{A} and \bar{B} , C_n	\bar{P}	In-Phase
t_{PHL}	\bar{B}_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{P}	Out-of-Phase
t_{PLH}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{G}	In-Phase
t_{PHL}	\bar{B}_i	None	\bar{A}_i	None	Remaining \bar{A} and \bar{B} , C_n	\bar{G}	Out-of-Phase
t_{PLH}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{A}	remaining \bar{B} , C_n	$A = B$	In-Phase
t_{PHL}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A}	Remaining \bar{B} , C_n	$A = B$	Out-of-Phase
t_{PLH}	C_n	None	None	All \bar{A} and \bar{B}	None	C_{n+4} or any \bar{F}	In-Phase
t_{PHL}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} , \bar{B} , C_n	C_{n+4}	Out-of-Phase
t_{PHL}	\bar{B}_i	None	\bar{A}_i	None	Remaining \bar{A} , \bar{B} , C_n	C_{n+4}	In-Phase

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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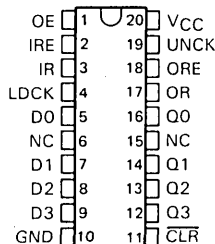
LSI Devices

SN54LS222, SN54LS224, SN54LS227, SN54LS228 SN74LS222, SN74LS224, SN74LS227, SN74LS228 16 X 4 SYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES

JANUARY 1981—REVISED MARCH 1985

- Independent Synchronous Inputs and Outputs
- 16 Words of 4 Bits Each
- 3-State Outputs Drive Bus Lines Directly
- Data Rates from 0 to 10 MHz
- Fall-Through Time . . . 50 ns Typ
- Data Terminals Arranged for Optimum PC Board Layout
- Expandable Using External Gating

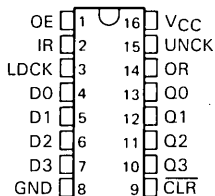
SN54LS222, SN54LS227 . . . J PACKAGE
SN74LS222, SN74LS227 . . . J OR N PACKAGE
(TOP VIEW)



description

These 64-bit memories are Low-Power Schottky memory arrays organized as 16 words of 4 bits each. They can be expanded in multiples of $15m + 1$ words or $4n$ bits, or both, (where n is the number of packages in the vertical array and m is the number of packages in the horizontal array) however some external gating is required (see Figure 1). For longer words using the 'LS224 or 'LS228, the IR signals of the first-rank packages and OR signals of the last-rank packages must be ANDed for proper synchronization.

SN54LS224, SN54LS228 . . . J PACKAGE
SN74LS224, SN74LS228 . . . J OR N PACKAGE
(TOP VIEW)



TYPE	INPUT-READY ENABLE AND OUTPUT-READY ENABLE	OUTPUT
'LS222	Yes	3-State
'LS224	No	3-State
'LS227	Yes	Open-collector
'LS228	No	Open-collector

NC—No internal connection

For chip carrier information contact the factory.

operation

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. These FIFOs are designed to process data at rates from 0 to 10 MHz in a bit-parallel format, word by word. Data is written into the memory on a high-to-low transition at the load clock input (LDCK) and read out on a low-to-high transition at the unload clock input (UNCK).

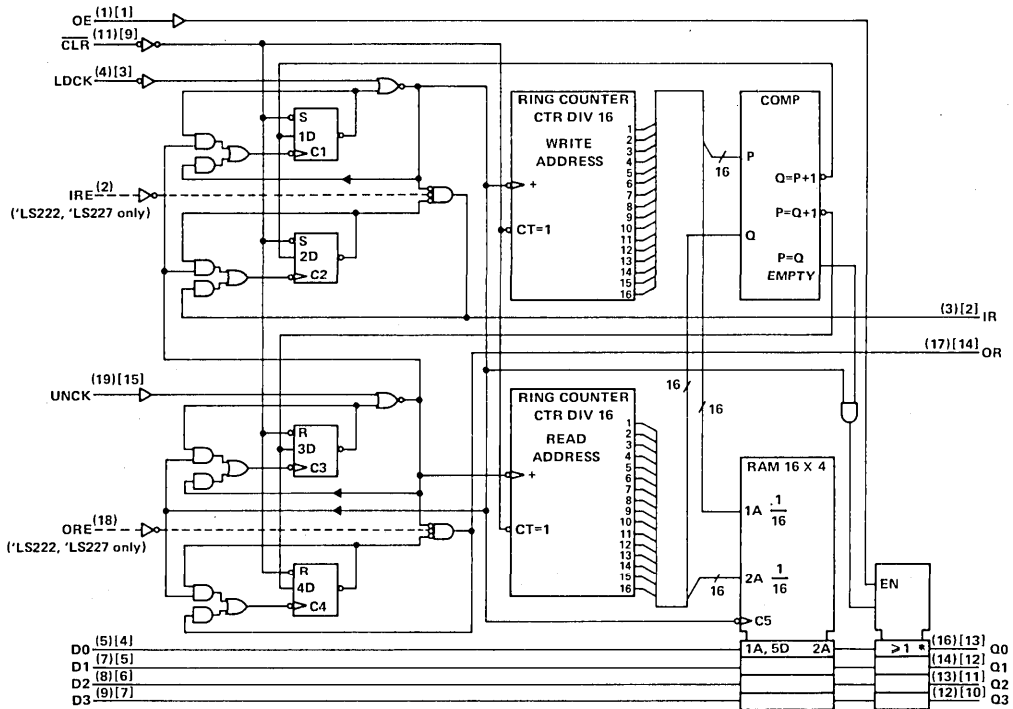
The memory is full when the number of words clocked in exceeds the number of words clocked out by 16. When the memory is full, LDCK signals have no effect. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory (see timing diagram) is monitored by the input ready (IR) and output ready (OR) flags that indicate "not full" and "not empty" conditions. The IR output will be high only when the memory is not full and the LDCK input is low. The OR output will be high only when the memory is not empty and UNCK is high.

A low level at the clear ($\overline{\text{CLR}}$) input resets the internal stack control counters and also sets IR high and OR low to indicate that old data remaining at the data outputs is invalid. Data outputs are noninverting with respect to the data inputs and are at high impedance when output enable (OE) is low. OE does not affect the IR and OR outputs.

**SN54LS222, SN54LS224, SN54LS227, SN54LS228
SN74LS222, SN74LS224, SN74LS227, SN74LS228
16 X 4 SYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES**

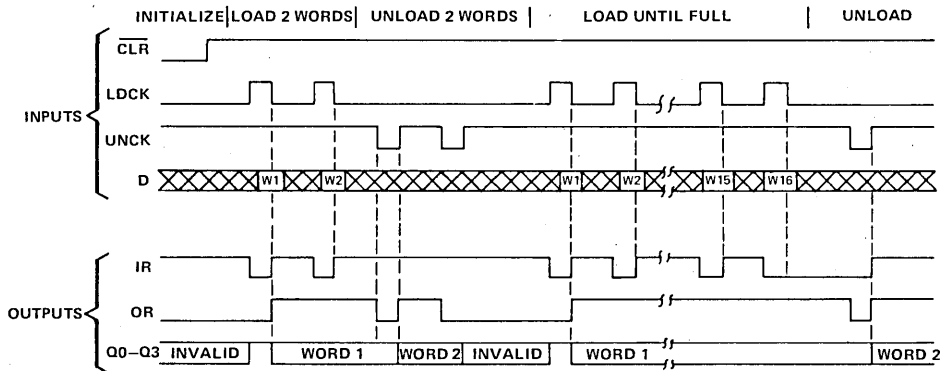
functional block diagram (positive logic)



*LS222 and 'LS224 have 3-state (∇) outputs.
'LS227 and 'LS228 have open-collector (\square) outputs.

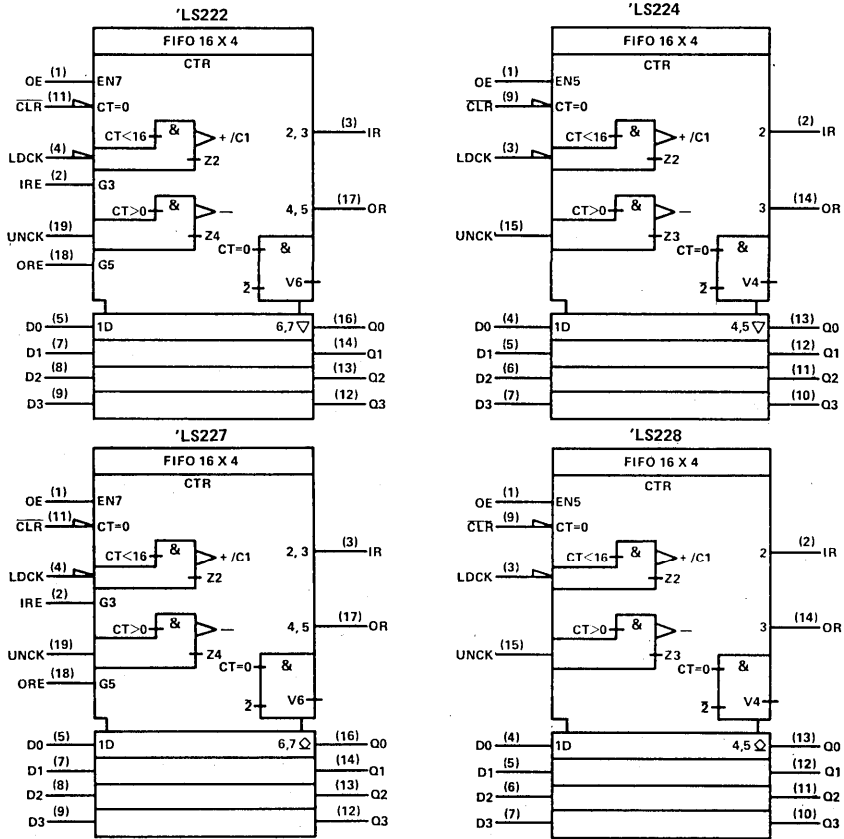
(*LS222 and 'LS227 pin numbers)
'LS224 and 'LS228 pin numbers)

timing diagram



SN54LS222, SN54LS224, SN54LS227, SN54LS228 SN74LS222, SN74LS224, SN74LS227, SN74LS228 16 X 4 SYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. These symbols are functionally accurate but do not show the details of implementation; for these, see the functional block diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at that time. Output data is invalid when the counter content is 0.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (See Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range:	
SN54LS222, SN54LS224, SN54LS227, SN54LS228	-55°C to 125°C
SN74LS222, SN74LS224, SN74LS227, SN74LS228	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

2
LSI Devices

SN54LS222, SN54LS224, SN74LS222, SN74LS224

16 X 4 SYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES WITH 3-STATE OUTPUTS

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage	0.7			0.8			V
I _{OH}	High-level output current	Q		-1	-2.6		mA	
		IR, OR		-0.4	-0.4			
I _{OL}	Low-level output current	Q		12	24		mA	
		IR, OR		4	8			
t _w	Pulse duration	LDCK high		60	60		ns	
		LDCK low		15	15			
		UNCK low		30	30			
		UNCK high		30	30			
		CLR low		20	20			
t _{su}	Setup time	D to LDCK↓		50	50		ns	
		LDCK↓ before UNCK↓		50	50			
		UNCK↑ before LDCK↑		50	50			
t _h	Hold time	D from LDCK↓		0	0		ns	
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS'		SN74LS'		UNIT		
			MIN	TYP‡	MAX	MIN		TYP‡	MAX
V _{IK}		V _{CC} = MIN, I _I = -18 mA	-1.5		-1.5		V		
V _{OH}	Q	V _{CC} = MIN, I _{OH} = MAX	2.4	3.3	2.4	3.4	V		
	IR, OR	V _{CC} = MIN, I _{OH} = -0.4 mA	2.5	3.4	2.7	3.4			
V _{OL}	Q	V _{CC} = MIN, I _{OL} = 12 mA	0.25		0.4		V		
		V _{CC} = MIN, I _{OL} = 24 mA			0.35				
	IR, OR	V _{CC} = MIN, I _{OL} = 4 mA	0.25		0.4				
		V _{CC} = MIN, I _{OL} = 8 mA			0.35				
I _{OZH}	Q	V _{CC} = MAX, V _O = 2.7 V	20		20		μA		
I _{OZL}	Q	V _{CC} = MAX, V _O = 0.4 V	-20		-20		μA		
I _I		V _{CC} = MAX, V _I = 7 V	0.1		0.1		mA		
I _{IH}		V _{CC} = MAX, V _I = 2.7 V	20		20		μA		
I _{IL}		V _{CC} = MAX, V _I = 0.4 V	-0.4		-0.4		mA		
I _{OS} §	Q	V _{CC} = MAX,	-30	-130	-30	-130	mA		
	IR, OR		-20	-100	-20	-100			
I _{CC}	V _{CC} = MAX,		Outputs high		84	135	84	135	mA
			Outputs low		87	155	87	155	
			Outputs disabled		89	155	89	155	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

SN54LS222, SN54LS224, SN74LS222, SN74LS224

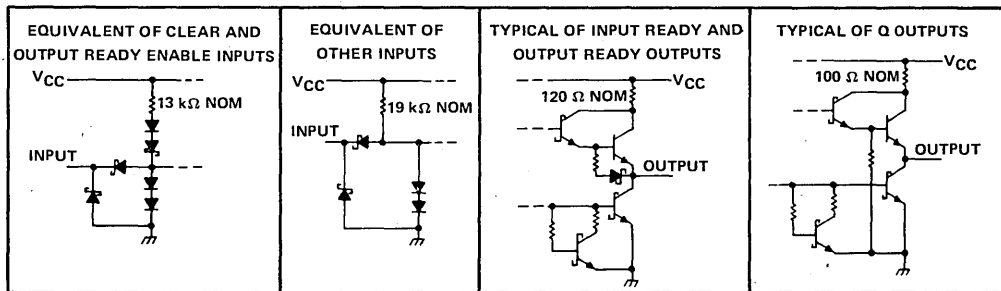
16 X 4 SYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES WITH 3-STATE OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM	TO	TEST CONDITIONS	'LS222			'LS224			UNIT	
				MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	IRE \uparrow	IR	$R_L = 2\text{ k}\Omega$, $C_L = 15\text{ pF}$, See Note 2		23	35				ns	
t_{PHL}	IRE \downarrow	IR			9	15				ns	
t_{PLH}	ORE \uparrow	OR			22	35				ns	
t_{PHL}	ORE \downarrow	OR			9	15				ns	
t_{PLH}	LDCK \uparrow	IR			25	40		25	40	ns	
t_{PHL}	LDCK \downarrow	IR			36	50		36	50	ns	
t_{PLH}	LDCK \downarrow	OR			48	70		48	70	ns	
t_{PLH}	UNCK \uparrow	OR			29	45		29	45	ns	
t_{PHL}	UNCK \downarrow	OR			28	45		28	45	ns	
t_{PLH}	UNCK \downarrow	IR			49	70		49	70	ns	
t_{PLH}	CLR \downarrow	IR			36	55		36	55	ns	
t_{PHL}	CLR \downarrow	OR			25	40		25	40	ns	
t_{PHL}	LDCK \downarrow	Q		$R_L = 667\ \Omega$, $C_L = 45\text{ pF}$, See Note 2		34	50		34	50	ns
t_{PLH}	UNCK \uparrow	Q				54	80		54	80	ns
t_{PHL}	UNCK \downarrow	Q			45	70		45	70	ns	
t_{PZL}	OE \uparrow	Q			22	35		22	35	ns	
t_{PZH}	OE \downarrow	Q			21	35		21	35	ns	
t_{PLZ}	OE \downarrow	Q	$R_L = 667\ \Omega$, $C_L = 5\text{ pF}$, See Note 2			16	30		16	30	ns
t_{PHZ}	OE \downarrow	Q			18	30		18	30	ns	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs



2

LSI Devices

SN54LS227, SN54LS228, SN74LS227, SN74LS228

16 X 4 SYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES

WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage	0.7			0.8			V
V _{OH}	High-level output voltage	Q			5.5			V
I _{OH}	High-level output current	IR, OR			-0.4			mA
I _{OL}	Low-level output current	Q			12			mA
		IR, OR			8			
t _w	Pulse duration	LDCK high			60			ns
		LDCK low			15			
		UNCK low			30			
		UNCK high			30			
		CLR low			20			
t _{su}	Setup time	D to LDCK↓			50			ns
		LDCK↓ before UNCK↓			50			
		UNCK↑ before LDCK↑			50			
t _h	Hold time	D from LDCK↓			0			ns
T _A	Operating free-air temperature	-55			125			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}		V _{CC} = MIN, I _I = -18 mA		-1.5			-1.5			V
I _{OH}	Q	V _{CC} = MIN, V _{OH} = 5.5 V		0.1			0.1			mA
V _{OH}	IR, OR	V _{CC} = MIN, I _{OH} = -0.4 mA		2.5	3.4		2.7	3.4		V
V _{OL}	Q	V _{CC} = MIN, I _{OL} = 12 mA		0.25	0.4		0.25	0.4		V
		V _{CC} = MIN, I _{OL} = 24 mA					0.35	0.5		
	IR, OR	V _{CC} = MIN, I _{OL} = 4 mA		0.25	0.4		0.25	0.4		
		V _{CC} = MIN, I _{OL} = 8 mA					0.35	0.5		
I _{OZH}	Q	V _{CC} = MAX, V _O = 2.7 V		20			20			μA
I _{OZL}	Q	V _{CC} = MAX, V _O = 0.4 V		-20			-20			μA
I _I		V _{CC} = MAX, V _I = 7 V		0.1			0.1			mA
I _{IH}		V _{CC} = MAX, V _I = 2.7 V		20			20			μA
I _{IL}		V _{CC} = MAX, V _I = 0.4 V		-0.4			-0.4			mA
I _{OS} §	IR, OR	V _{CC} = MAX		-20	-100		-20	-100		mA
I _{CC}	V _{CC} = MAX		Outputs high		84	135		84	135	mA
			Outputs low		87	155		87	155	
			Outputs disabled		89	155		89	155	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

SN54LS227, SN54LS228, SN74LS227, SN74LS228

16 X 4 SYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES

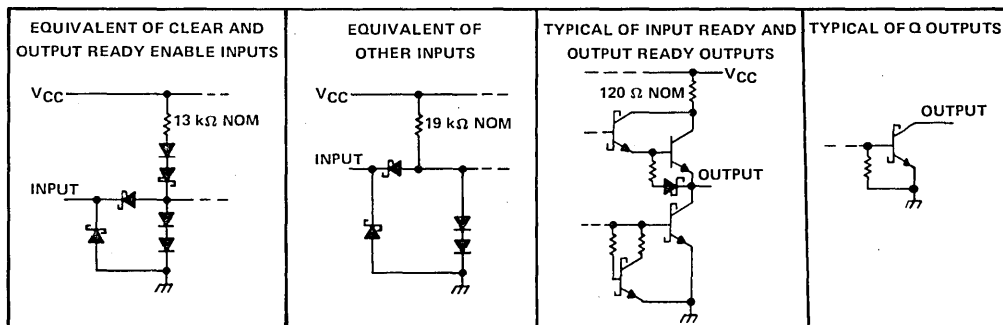
WITH OPEN-COLLECTOR OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM	TO	TEST CONDITIONS	'LS227			'LS228			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	IRE \dagger	IR	$R_L = 2\text{ k}\Omega$, $C_L = 15\text{ pF}$, See Note 2		23	35				ns
t_{PHL}	IRE \dagger	IR			9	15				ns
t_{PLH}	ORE \dagger	OR			22	35				ns
t_{PHL}	ORE \dagger	OR			9	15				ns
t_{PLH}	LDCK \dagger	IR			25	40	25	40		ns
t_{PHL}	LDCK \dagger	IR			36	50	36	50		ns
t_{PLH}	LDCK \dagger	OR			48	70	48	70		ns
t_{PLH}	UNCK \dagger	OR			29	45	29	45		ns
t_{PHL}	UNCK \dagger	OR			28	45	28	45		ns
t_{PLH}	UNCK \dagger	IR			49	70	49	70		ns
t_{PLH}	CLR \dagger	IR			36	55	36	55		ns
t_{PHL}	CLR \dagger	OR			25	40	25	40		ns
t_{PHL}	LDCK \dagger	Q	$R_L = 667\ \Omega$, $C_L = 45\text{ pF}$, See Note 2	34	50	34	50		ns	
t_{PLH}	UNCK \dagger	Q		54	80	54	80		ns	
t_{PHL}	UNCK \dagger	Q		45	70	45	70		ns	
t_{PLH}	OE \dagger	Q		21	30	21	30		ns	
t_{PHL}	OE \dagger	Q		20	35	20	35		ns	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs



2
LSI Devices

SN54LS222, SN54LS224, SN54LS227, SN54LS228
SN74LS222, SN74LS224, SN74LS227, SN74LS228
16 X 4 SYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES

TYPICAL APPLICATIONS INFORMATION

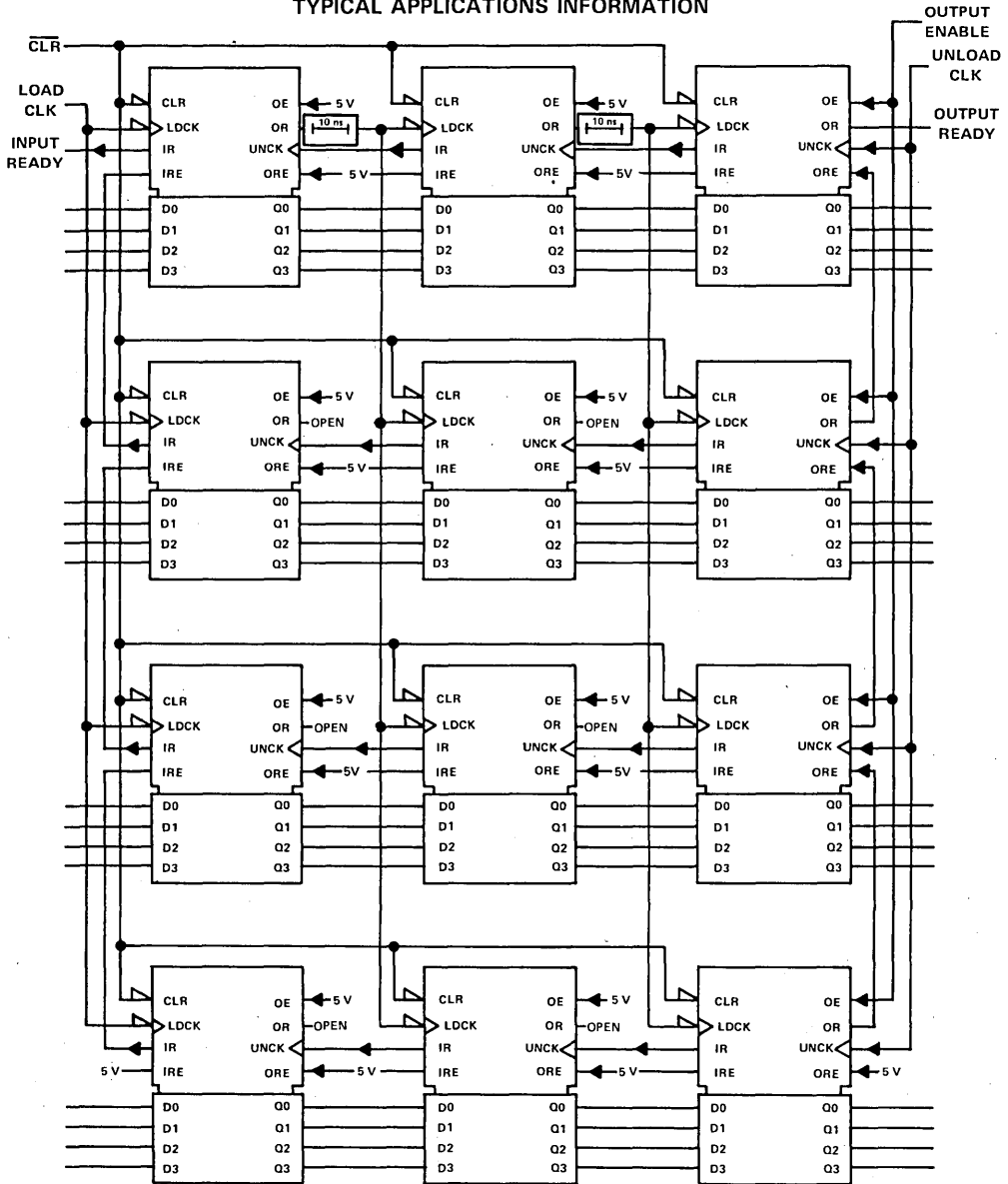



FIGURE 1. 46-WORD BY 16-BIT EXPANSION USING 'LS222

 = Noninverting delay ≥ 10 ns (e.g., 2 stages of 'LS04), 2 places.

- Independent Asynchronous Inputs and Outputs
- Organized as 16-Words of 5 Bits
- DC to 10-MHz Data Rate
- 3-State Data Outputs
- 20-Pin, 300-mil, High-Density Package

description

This 80-bit active-element memory is a monolithic Schottky-clamped transistor-transistor logic (STTL) array organized as 16 words of five-bits each. A memory system using the SN74S225 can easily be expanded in multiples of 16 words or of 5 bits as shown in Figure 2. The three-state outputs controlled by a single enable, \overline{OE} , makes bus connection and multiplexing easy.

operation

A FIFO is a memory storage device that allows data to be written into and/or read from its array at independent data rates. The 'S225 FIFO will process data at any desired clock rate from DC to 10 MHz. The data is processed in a parallel format, word by word.

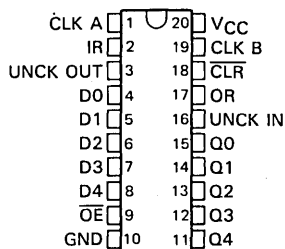
Reading or writing is done independently utilizing separate asynchronous data clocks. Data may be written into the array on the low-to-high transition of either load clock input. Data may be read out of the array on the low-to-high transition of the unload clock input (normally high). Writing data into the FIFO may be accomplished in one of two manners: 1) In applications not requiring a gated clock control, best results will be achieved by applying the clock input to one of the clocks while tying the other clock input high. 2) In applications needing a gated clock, the load clock (gate control) must be high in order for the FIFO to load on the next clock pulse. The clock A and B inputs can be used interchangeably for either clock gate control or clock input.

Status of the 'S225 is provided by three outputs. Input ready monitors the status of the last word location and signifies when the memory is full. This output is high whenever the memory is available to accept any data. The unload clock output also monitors the last word location. This output generates a low-logic-level pulse (synchronized to the internal clock pulse) when the location is vacant. The third status output, output ready, is high when the first word location contains valid data and unload clock input is high. When unload clock input goes low, output ready will go low and stay low until new valid data is in the first word position. The first word location is defined as the location from which data is provided to the outputs.

The data outputs are noninverted with respect to the data inputs and are three-state with a common control input, output enable. When output enable is low, the data outputs are enabled to function as totem-pole outputs. A high-logic-level forces each data output to a high-impedance state while all other inputs and outputs remain active.

The clear input invalidates all data stored in the memory array by clearing the control logic and setting output ready to a low-logic-level on the high-to-low transition of a low-active pulse.

SN74S225 . . . J OR N PACKAGE
(TOP VIEW)



SN74S225

16 × 5 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORY

FUNCTION TABLES

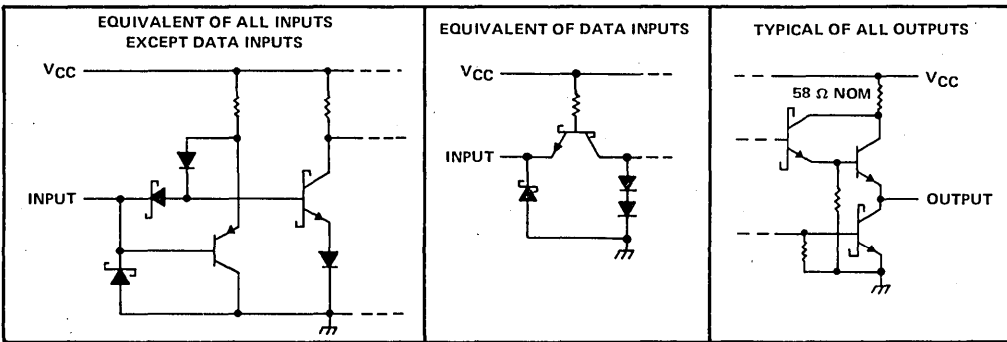
TABLE 1 INPUT FUNCTIONS

Input	Pin	Description
CLK A	1	Load Clock A
D0-D4	4-8	Data Inputs
\overline{OE}	9	Output Enable
UNCK IN	16	Unload Clock
\overline{CLR}	18	Clear
CLK B	19	Load Clock B
GND	10	Ground pin
VCC	20	Supply Voltage

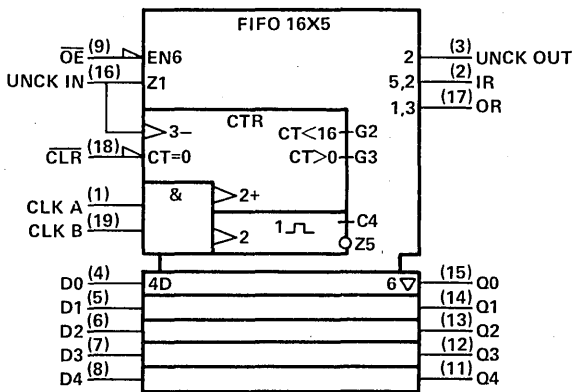
TABLE 2 OUTPUT FUNCTIONS

Output	Pin	Description
IR	2	Input Ready
UNCK OUT	3	Unload Clock
Q4-D0	11-15	Data Outputs
OR	17	Output Ready

schematics of inputs and outputs



logic symbol†

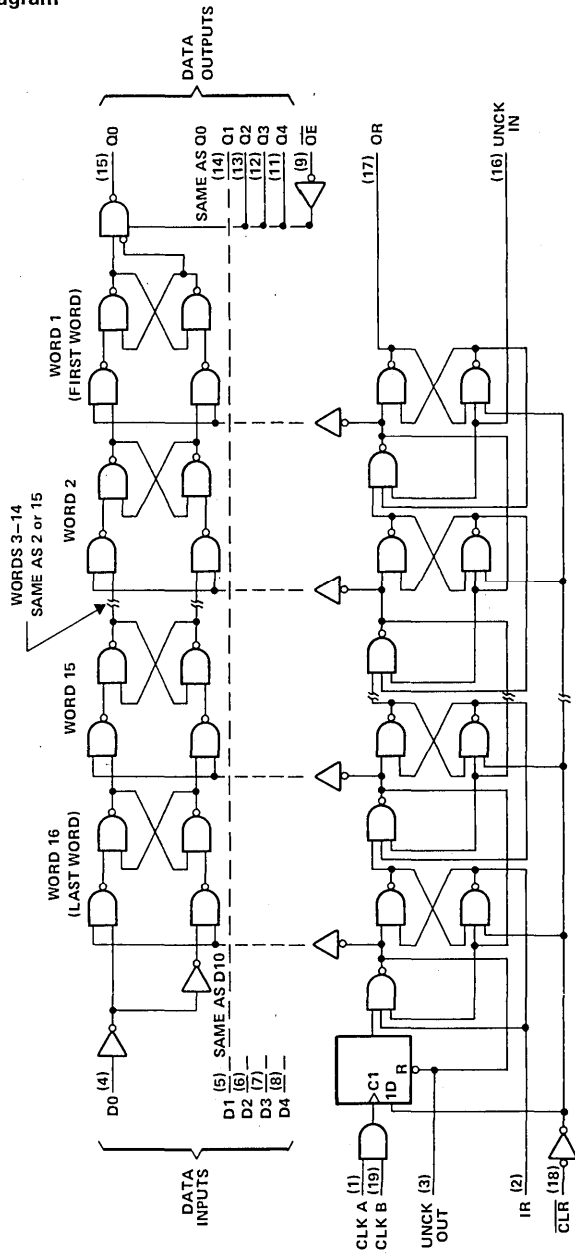


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

2 LSI Devices

SN74S225
 16 × 5 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORY

functional block diagram



SN74S225

16 × 5 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORY

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT	
V_{CC}	Supply voltage	4.75	5	5.25	V	
V_{IH}	High-level input voltage	2			V	
V_{IL}	Low-level input voltage			0.8	V	
I_{OH}	High-level output current	Q outputs		-6.5	mA	
		All other outputs		-3.2		
I_{OL}	Low-level output current	Q outputs		16	mA	
		All other outputs		8		
t_w	Pulse duration	CLK A or CLK B (high)		25	ns	
		UNCK IN (low)		7		
		CLR (low)		40		
t_{su}	Setup time before CLK A† or CLK B†	Data (See Note 2)		-20	ns	
		CLR inactive		25		
t_h	Hold time after CLK A† or CLK B†			70	ns	
T_A	Operating free-air temperature			0	70	°C

NOTE 2: Data must be setup within 20 ns after the load clock positive transition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 4.75 \text{ V}, I_I = -18 \text{ mA}$			-1.2	V
V_{OH}	Q	$V_{CC} = 4.75 \text{ V}, I_{OH} = -6.5 \text{ mA}$	2.4	2.9		V
	All others	$V_{CC} = 4.75 \text{ V}, I_{OH} = -3.2 \text{ mA}$	2.4	2.9		
V_{OL}	Q	$V_{CC} = 4.75 \text{ V}, I_{OL} = 16 \text{ mA}$		0.35	0.5	V
	All others	$V_{CC} = 4.75 \text{ V}, I_{OL} = 8 \text{ mA}$		0.35	0.5	
I_{OZH}		$V_{CC} = 5.25 \text{ V}, V_O = 2.4 \text{ V}$			50	μA
I_{OZL}		$V_{CC} = 5.25 \text{ V}, V_O = 0.5 \text{ V}$			-50	μA
I_I		$V_{CC} = 5.25 \text{ V}, V_I = 5.5 \text{ V}$			1	mA
I_{IH}	Data	$V_{CC} = 5.25 \text{ V}, V_I = 2.7 \text{ V}$		40		μA
	All others			25		
I_{IL}	Data	$V_{CC} = 5.25 \text{ V}, V_I = 0.5 \text{ V}$		-1		mA
	All others			-0.25		
I_{OS}^\ddagger		$V_{CC} = 5.25 \text{ V}, V_O = 0 \text{ V}$	-30		-100	mA
I_{CC}		$V_{CC} = 5.25 \text{ V},$ (See Note 3)		80	120	mA

†All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

‡Duration of the short circuit should not exceed one second.

NOTE 3: I_{CC} is measured with all inputs grounded and the output open.

SN74S225
16 × 5 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORY

switching characteristics over recommended operating ranges of T_A and V_{CC}
(unless otherwise noted)

PARAMETERS†	FROM	TO	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
f_{max}	CLK A		$C_L = 30$ pF, See Note 4	10	20		MHZ
f_{max}	CLK B			10	20		MHz
f_{max}	UNCK IN			10	20		MHz
t_w	UNCK OUT			7	14		ns
t_{dis}	\overline{OE}	Any Q	$C_L = 5$ pF	10	25		ns
t_{en}				25	40		
t_{PLH}	UNCK IN	Any Q	$C_L = 30$ pF, See Note 4	50	75		ns
t_{PHL}				50	75		
t_{PLH}	CLK A or CLK B	OR		190	300		ns
t_{PLH}	UNCK IN	OR		40	60		ns
t_{PHL}				30	45		
t_{PHL}	\overline{CLR}	OR		35	60		ns
t_{PHL}	CLK A or CLK B	UNCK OUT		25	45		ns
t_{PHL}	UNCK IN	UNCK OUT		270	400		ns
t_{PHL}	CLK A or CLK B	IR		55	75		ns
t_{PLH}	UNCK IN	IR		255	400		ns
t_{PLH}	\overline{CLR}	IR		16	35		ns
t_{PLH}	OR†	Any Q		10	20		ns

† f_{max} = maximum clock frequency

t_w = pulse width (output)

†† The arrow indicates that the low-to-high (↑) or high-to-low (↓) transition of the output ready (OR) output is used for reference.

t_{PLH} = propagation delay time, low-to-high-level output.

t_{PHL} = propagation delay time, high-to-low-level output.

‡All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

NOTE 4: Load circuit and voltage waveforms are shown in Section 1.

2
LSI Devices

SN74S225
16 × 5 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORY

TYPICAL WAVEFORMS FOR A 16-WORD FIFO

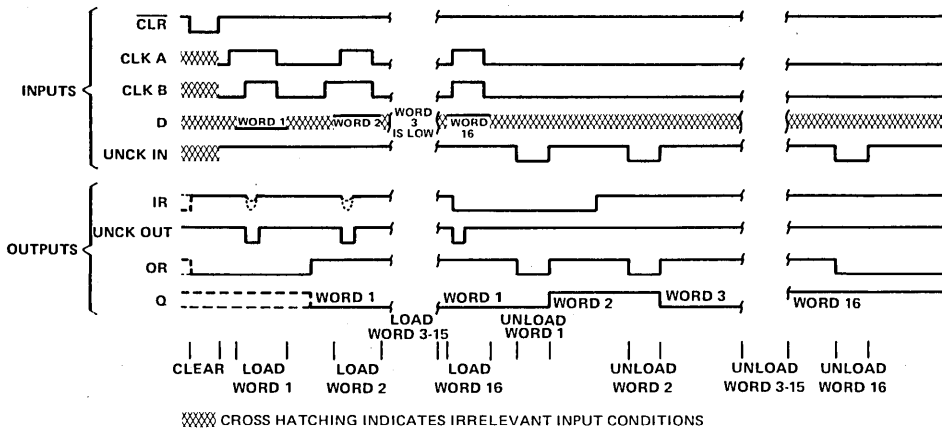


FIGURE 1. TYPICAL WAVEFORMS FOR A 16-WORD FIFO

2

LSI Devices

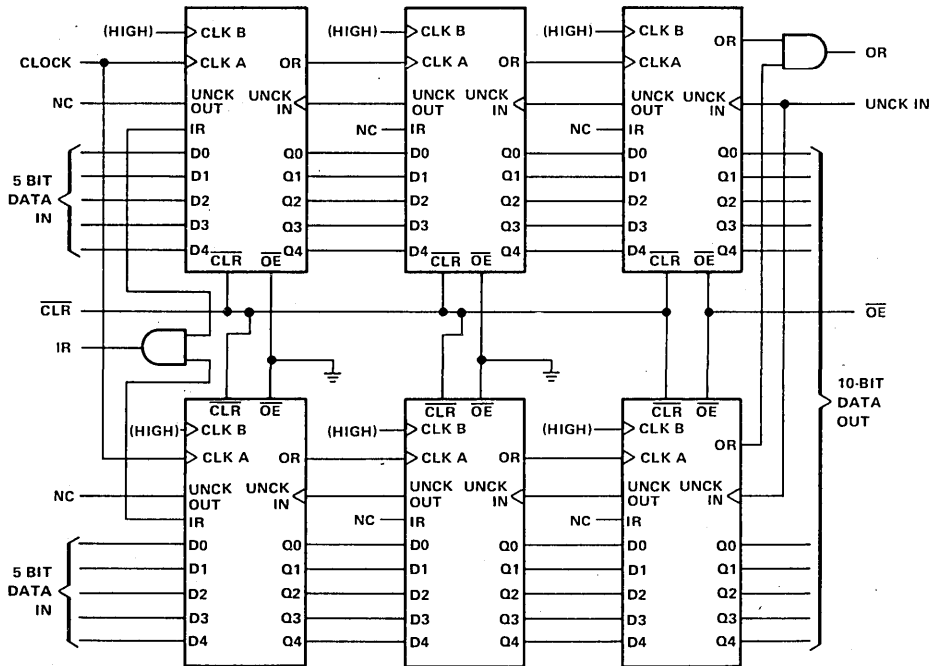


FIGURE 2. EXPANDING THE 'S225 FIFO (48 WORDS OF 10 BITS SHOWN)

SN54ALS229A, SN74ALS229A

16 × 5 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES

D2876, MARCH 1986—REVISED APRIL 1986

- Independent Asynchronous Inputs and Outputs
- 16 Words by 5 Bits Each
- Data Rates from 0 to 30 MHz
- Fall-Through Time . . . 24 ns Typ
- 3-State Outputs

description

These 80-bit memories utilize Advanced Low-Power Schottky technology and feature high speed and fast fall-through times. They are organized as 16 words by 5 bits each.

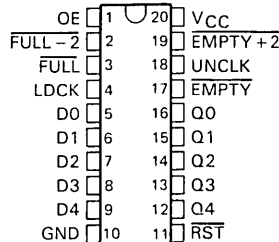
A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. These FIFOs are designed to process data at rates from 0 to 25 megahertz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition at the load clock input (LDCK) and is read out on a low-to-high transition at the unload clock input (UNCLK). The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals will have no effect. When the memory is empty, UNCLK signals have no effect.

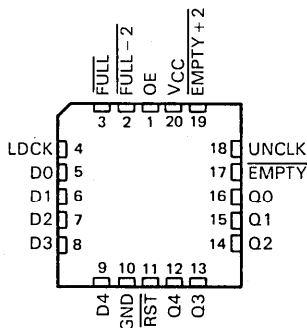
Status of the FIFO memory is monitored by the FULL, EMPTY, FULL - 2, and EMPTY + 2 output flags. The FULL output will be low whenever the memory is full, and high whenever not full. The FULL - 2 output will be low whenever the memory contains 14 data words. The EMPTY output will be low whenever the memory is empty, and high whenever it is not empty. The EMPTY + 2 output will be low whenever 2 words remain in memory.

A low level on the reset input ($\overline{\text{RST}}$) resets the internal stack control pointers and also sets $\overline{\text{EMPTY}}$ low and sets FULL, FULL - 2, and $\overline{\text{EMPTY}} + 2$ high. The Q outputs are not reset to any specific logic level. The first low-to-high transition on LDCK, after either a $\overline{\text{RST}}$ pulse or from an empty condition, will cause $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output enable input (OE) is low. OE does not affect the output flags. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

SN54ALS229A . . . J PACKAGE
SN74ALS229A . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS229A . . . FK PACKAGE
SN74ALS229A . . . FN PACKAGE
(TOP VIEW)

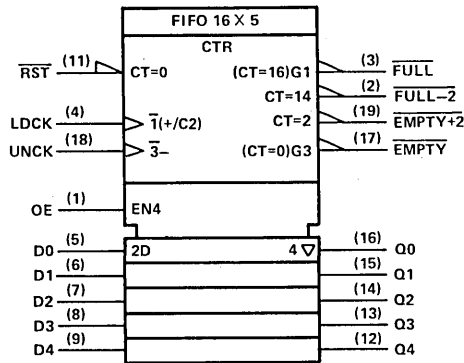


2

LSI Devices

SN54ALS229A, SN74ALS229A
16 × 5 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES

logic symbol†



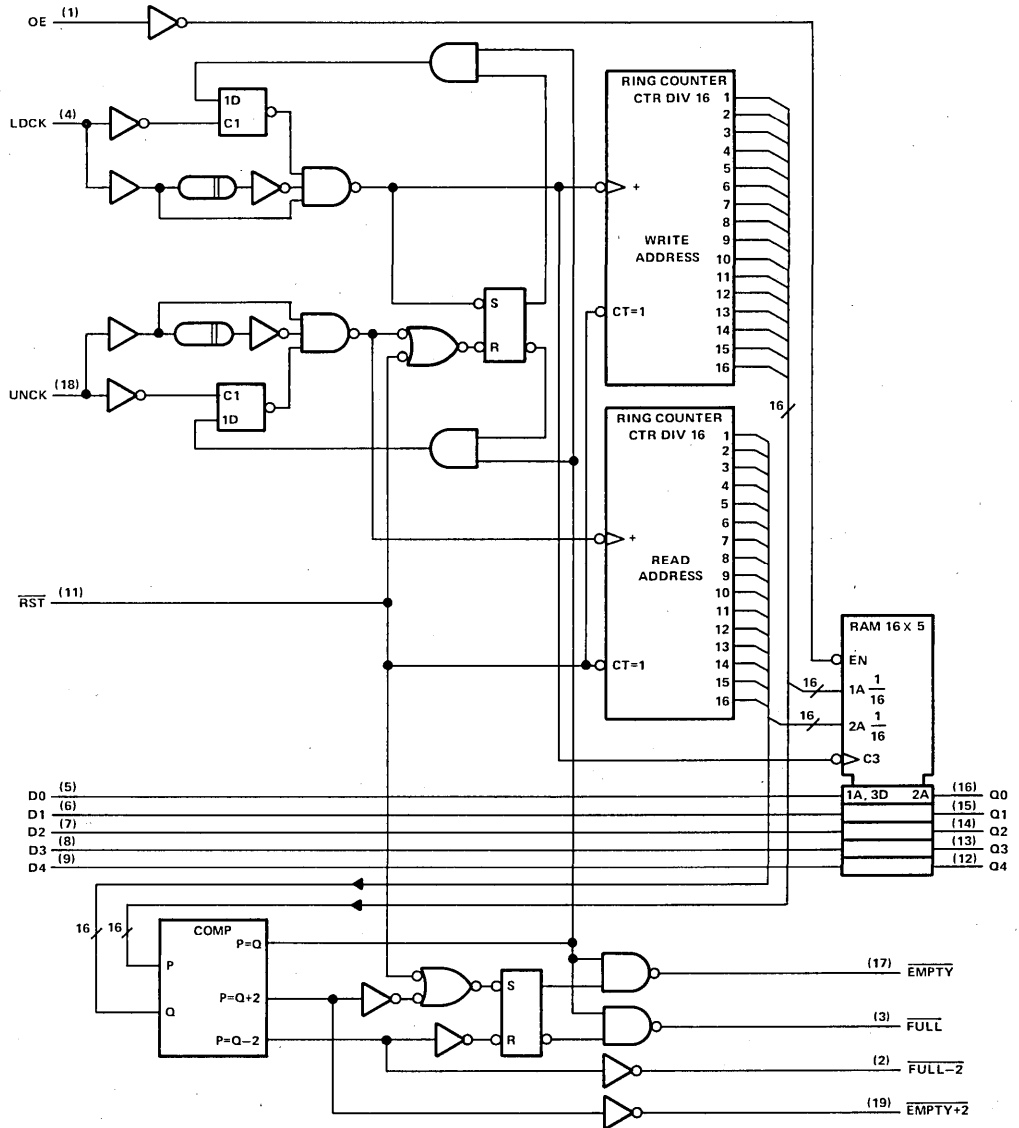
† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

2

LSI Devices

SN54ALS229A, SN74ALS229A
 16 × 5 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES

logic diagram (positive logic)

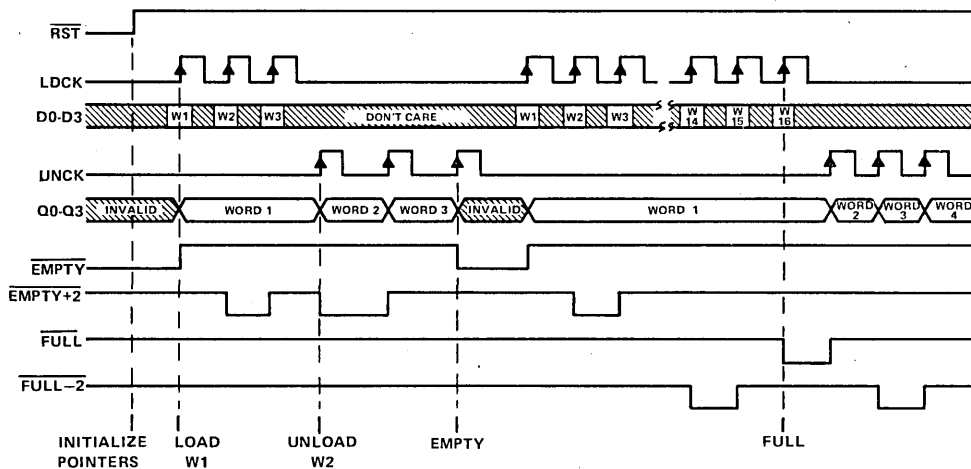


2
 LSI Devices

SN54ALS229A, SN74ALS229A

16 × 5 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES

timing diagram



2

LSI Devices

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range: SN54ALS229A	-55°C to 125°C
SN74ALS229A	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54ALS229A			SN74ALS229A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current	Q outputs		-1.0	-1.6		mA	
		Status flags		-0.4	-0.4			
I_{OL}	Low-level output current	Q outputs		12	24		mA	
		Status flags		4	8			
f_{clock}	Clock frequency	LDCK	0	25	0	30	MHz	
		UNCK	0	25	0	30		
t_w	Pulse duration	RST low	20		15		ns	
		LDCK low	15		10			
		LDCK high	25		20			
		UNCK low	15		10			
		UNCK high	25		20			
t_{su}	Setup time	Data before LDCK†	10		10		ns	
		RST (inactive) before LDCK†	5		5			
t_h	Hold time	Data after LDCK†	5		5		ns	
T_A	Operating free-air temperature	-55		125	0		70	°C

SN54ALS229A, SN74ALS229A

16 × 5 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS229A		SN74ALS229A		UNIT		
		MIN	TYP†	MAX	MIN		TYP†	MAX
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2		-1.2	V	
V _{OH}	Status flags V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA	V _{CC} -2		V _{CC} -2			V	
	Q outputs V _{CC} = 4.5 V, I _{OH} = -1 mA	2.4	3.3					
V _{OL}	Q outputs V _{CC} = 4.5 V, I _{OL} = 12 mA			0.25	0.4	0.25	0.4	
	Q outputs V _{CC} = 4.5 V, I _{OL} = 24 mA					0.35	0.5	
	Status flags V _{CC} = 4.5 V, I _{OL} = 4 mA			0.25	0.4	0.25	0.4	
	Status flags V _{CC} = 4.5 V, I _{OL} = 8 mA					0.35	0.5	
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V			20		20	μA	
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.4 V			-20		-20	μA	
I _I	V _{CC} = 5.5 V, V _I = 7 V			0.1		0.1	mA	
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V			20		20	μA	
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V			-0.2		-0.2	mA	
I _O ‡	V _{CC} = 5.5 V, V _O = 2.25 V	-30		-112		-30	-112	mA
I _{CC}	V _{CC} = 5.5 V			95	150	95	140	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OQ}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX			UNIT	
			'ALS229A			SN54ALS229A		SN74ALS229A		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
f _{max}	LDCK				25		30		MHz	
	UNCK				25		30			
t _{pd}	LDCK↑	Any Q	24	47	7	54	7	50	ns	
t _{pd}	UNCK↑	Any Q	19	29	9	35	9	33	ns	
t _{PLH}	LDCK↑	EMPTY	18	26	9	32	9	30	ns	
t _{PHL}	UNCK↑	EMPTY	18	25	9	32	9	29	ns	
t _{PHL}	RST↓	EMPTY	15	21	6	26	6	24	ns	
t _{pd}	LDCK↑	EMPTY+2	23	33	10	40	10	38	ns	
t _{pd}	UNCK↑	EMPTY+2	20	29	9	38	9	35	ns	
t _{PLH}	RST↓	EMPTY+2	20	28	9	35	9	33	ns	
t _{pd}	LDCK↑	FULL-2	23	33	10	40	10	38	ns	
t _{pd}	UNCK↑	FULL-2	20	29	9	38	9	35	ns	
t _{PLH}	RST↓	FULL-2	20	28	9	35	9	33	ns	
t _{PHL}	LDCK↑	FULL	21	28	10	35	10	33	ns	
t _{PLH}	UNCK↑	FULL	17	23	8	29	8	27	ns	
t _{PLH}	RST↓	FULL	18	27	8	33	8	31	ns	
t _{en}	OE↑	Q	8	13	1	16	2	15	ns	
t _{dis}	OE↓	Q	8	14	2	20	2	17	ns	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS232A, SN74ALS232A 16 × 4 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES

D2876, OCTOBER 1985—REVISED APRIL 1986

- Independent Asynchronous Inputs and Outputs
- 16 Words by 4 Bits Each
- Data Rates From 0 to 30 MHz
- Fall-Through Time . . . 24 ns Typ
- 3-State Outputs

description

These 64-bit memories use Advanced Low-Power Schottky technology and feature high speed and fast fall-through times. They are organized as 16 words by 4 bits each.

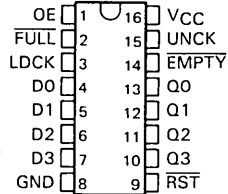
A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. These FIFOs are designed to process data at rates from 0 to 25 megahertz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition at the load clock input (LDCK) and is read out on a low-to-high transition at the unload clock input (UNCK). The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

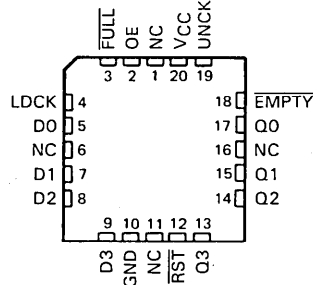
Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ output flags. The $\overline{\text{FULL}}$ output will be low when the memory is full, and high when the memory is not full. The $\overline{\text{EMPTY}}$ output will be low when the memory is empty, and high when it is not empty.

A low level on the reset input ($\overline{\text{RST}}$) resets the internal stack control pointers and also sets $\overline{\text{EMPTY}}$ low and sets $\overline{\text{FULL}}$ high. The outputs are not reset to any specific logic levels. The first low-to-high transition on LDCK, either after a $\overline{\text{RST}}$ pulse or from an empty condition, will cause $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable input (OE) is low. OE does not affect either the $\overline{\text{FULL}}$ or $\overline{\text{EMPTY}}$ output flags. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

SN54ALS232A . . . J PACKAGE
SN74ALS232A . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS232A . . . FK PACKAGE
SN74ALS232A . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection.

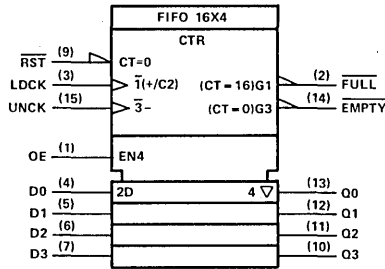


LSI Devices

SN54ALS232A, SN74ALS232A

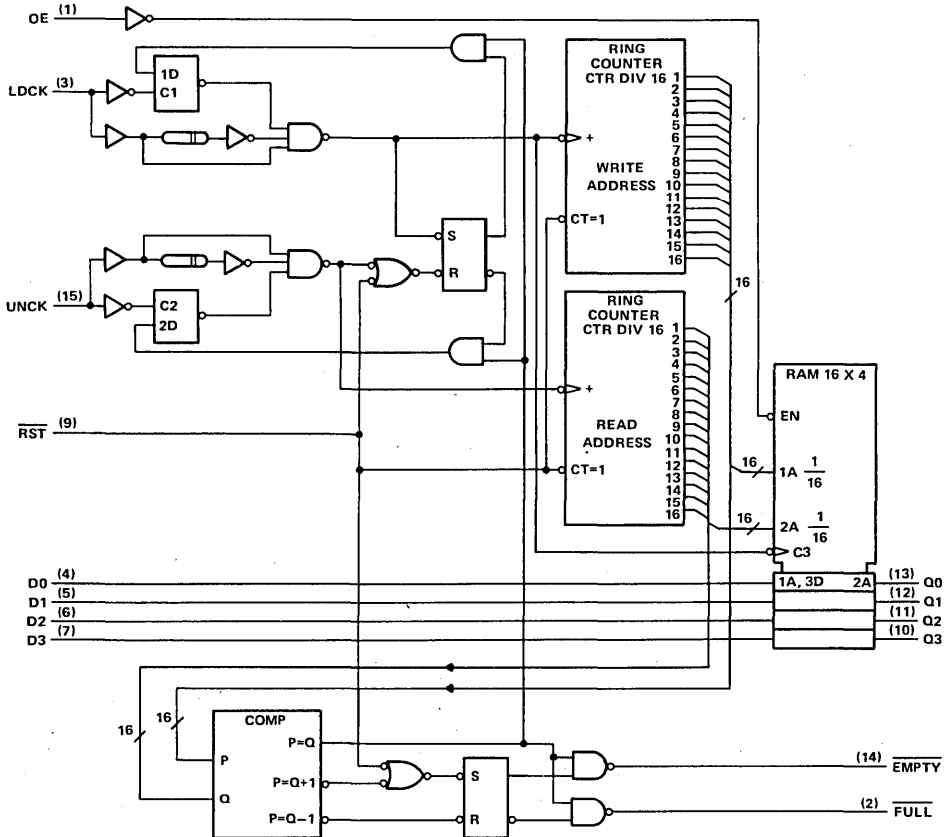
16 × 4 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES

logic symbol†



†This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

logic diagram (positive logic)

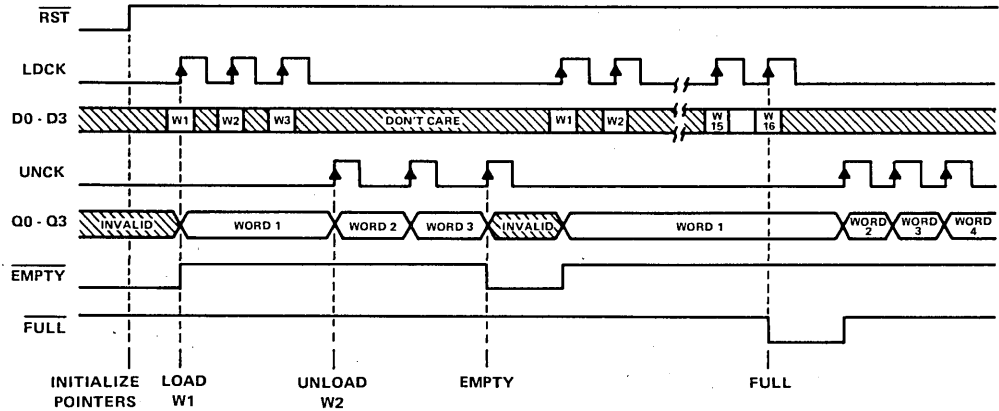


Pin numbers shown are for D, J, and N packages.

SN54ALS232A, SN74ALS232A

16 × 4 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES

timing diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range: SN54ALS232A	-55°C to 125°C
SN74ALS232A	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54ALS232A			SN74ALS232A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current	Q outputs		-1	-1.6		mA	
		FULL, EMPTY		-0.4	-0.4			
I_{OL}	Low-level output current	Q outputs		12	24		mA	
		FULL, EMPTY		4	8			
f_{clock}	Clock frequency	LDCK		0	25	0	30	MHz
		UNCK		0	25	0	30	
t_w	Pulse duration	RST low		20	15		ns	
		LDCK low		15	10			
		LDCK high		25	20			
		UNCK low		15	10			
		UNCK high		25	20			
t_{su}	Setup time	Data before LDCK↑		10	10		ns	
		RST (inactive) before LDCK↑		5	5			
t_h	Hold time	Data after LDCK↑		5	5		ns	
T_A	Operating free-air temperature	-55	125	0	70	°C		

2

LSI Devices

SN54ALS232A, SN74ALS232A

16 × 4 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS232A		SN74ALS232A		UNIT
		MIN	TYP†	MAX	MIN	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2		V
V _{OH}	FULL, EMPTY	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA		V _{CC} -2		V
	Q outputs	V _{CC} = 4.5 V, I _{OH} = -1 mA		2.4 3.3		
V _{OL}	Q outputs	V _{CC} = 4.5 V, I _{OL} = 12 mA		0.25 0.4		V
		V _{CC} = 4.5 V, I _{OL} = 24 mA		0.35 0.5		
	V _{CC} = 4.5 V, I _{OH} = 4 mA		0.25 0.4			
	FULL, EMPTY		0.35 0.5			
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V			20		μA
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.4 V			-20		μA
I _I	V _{CC} = 5.5 V, V _I = 7 V			0.1		mA
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V			20		μA
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V			-0.2		mA
I _O ‡	V _{CC} = 5.5 V, V _O = 2.25 V			-30 -112		mA
I _{CC}	V _{CC} = 5.5 V			75 125		mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX			UNIT	
			ALS232A			SN54ALS232A		SN74ALS232A		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
f _{max}	LDCK		40			25		30		MHz
	UNCK		40			25		30		
t _{pd}	LDCK↑	Any Q	30	40	4	50	4	46	ns	
t _{pd}	UNCK↑	Any Q	20	27	7	35	7	31	ns	
t _{PLH}	LDCK↑	EMPTY	17	23	8	29	8	26	ns	
t _{PHL}	UNCK↑	EMPTY	19	24	10	36	10	29	ns	
t _{PHL}	RST↓	EMPTY	13	18	5	23	5	20	ns	
t _{PHL}	LDCK↑	FULL	21	26	10	35	10	31	ns	
t _{PLH}	UNCK↑	FULL	17	23	8	28	8	25	ns	
t _{PLH}	RST↓	FULL	18	24	8	31	8	28	ns	
t _{en}	OE↑	Q	7	12	1	16	1	14	ns	
t _{dis}	OEL	Q	10	16	2	23	2	21	ns	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

2
LSI Devices

SN54ALS233A, SN74ALS233A

16 × 5 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES

D2876, JANUARY 1986—REVISED APRIL 1986

- Independent Asynchronous Inputs and Outputs
- 16 Words by 5 Bits Each
- Data Rates from 0 to 30 MHz
- Fall-Through Time . . . 24 ns Typ
- 3-State Outputs

description

These 80-bit memories utilize Advanced Low-Power Schottky technology and feature high speed and fast fall-through times. They are organized as 16 words by 5 bits each.

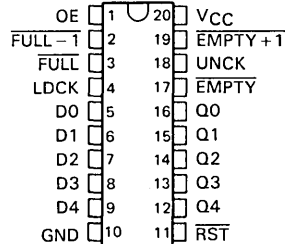
A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. These FIFOs are designed to process data at rates from 0 to 25 megahertz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition at the load clock input (LDCK) and is read out on a low-to-high transition at the unload clock input (UNCK). The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals will have no effect. When the memory is empty, UNCK signals have no effect.

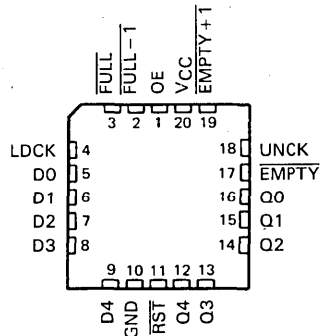
Status of the FIFO memory is monitored by the FULL, EMPTY, FULL-1, and EMPTY+1 output flags. The FULL output will be low whenever the memory is full, and high whenever not full. The FULL-1 output will be low whenever the memory contains 15 data words. The EMPTY output will be low whenever the memory is empty, and high whenever it is not empty. The EMPTY+1 output will be low whenever one word remains in memory.

A low level on the reset input (\overline{RST}) resets the internal stack control pointers and also sets \overline{EMPTY} low and sets FULL, FULL-1, and $\overline{EMPTY+1}$ high. The Q outputs are not reset to any specific logic level. The first low-to-high transition on LDCK, after either a \overline{RST} pulse or from an empty condition, will cause \overline{EMPTY} to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output enable input (OE) is low. OE does not affect the output flags. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

SN54ALS233A . . . J PACKAGE
SN74ALS233A . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS233A . . . FK PACKAGE
SN74ALS233A . . . FN PACKAGE
(TOP VIEW)

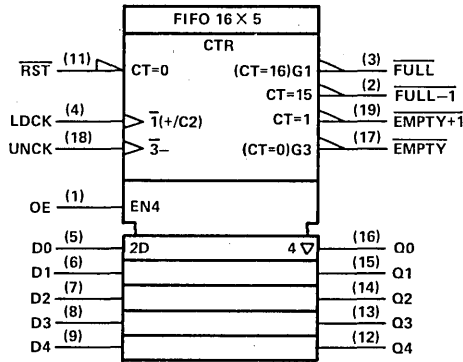


2

LSI Devices

SN54ALS233A, SN74ALS233A
16 × 5 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES

logic symbol†



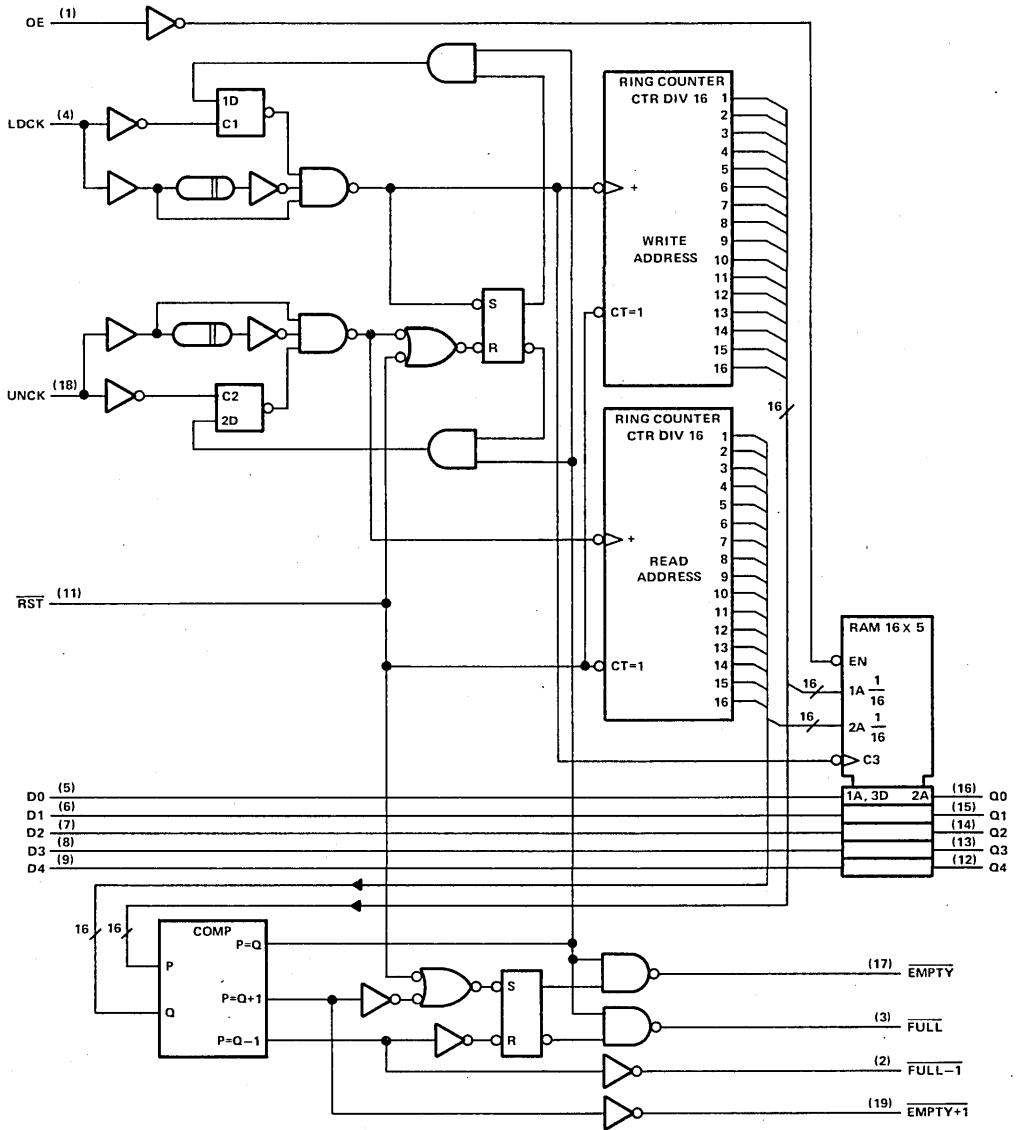
† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

2

LSI Devices

SN54ALS233A, SN74ALS233A
 16 × 5 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES

logic diagram (positive logic)

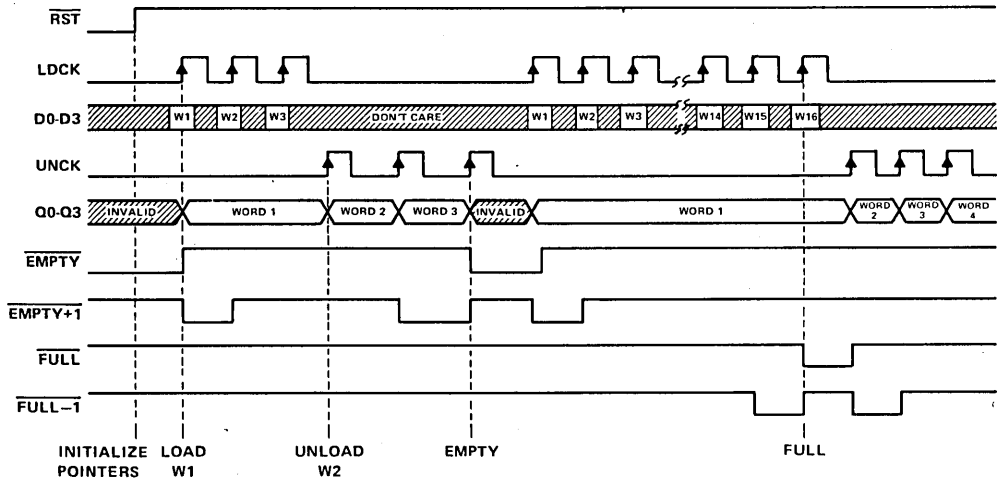


2

LSI Devices

SN54ALS233A, SN74ALS233A
16 × 5 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES

timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range: SN54ALS233A	-55°C to 125°C
SN74ALS233A	0°C to 70°C
Storage temperature range	-65°C to 150°C

2

LSI Devices

SN54ALS233A, SN74ALS233A

16 × 5 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES

recommended operating conditions

		SN54ALS233A			SN74ALS233A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage				0.8			V
I _{OH}	High-level output current	Q outputs		-1		-1.6		mA
		Status flags		-0.4		-0.4		
I _{OL}	Low-level output current	Q outputs		12		24		mA
		Status flags		4		8		
f _{clock}	Clock frequency	LDCK		0 25		0 30		MHz
		UNCK		0 25		0 30		
t _w	Pulse duration	RST low		20		15		ns
		LDCK low		15		10		
		LDCK high		25		20		
		UNCK low		15		10		
		UNCK high		25		20		
t _{su}	Setup time	Data before LDCK↑		10		10		ns
		RST inactive before LDCK↑		5		5		
t _h	Hold time	Data after LDCK↑		5		5		ns
T _A	Operating free-air temperature	-55		125		0 70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS233A		SN74ALS233A		UNIT
				MIN	TYP†	MAX	MIN	
V _{IK}	Status flags	V _{CC} = 4.5 V, I _I = -18 mA		-1.2		-1.2		V
V _{OH}	Q outputs	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA		V _{CC} -2		V _{CC} -2		V
		V _{CC} = 4.5 V, I _{OH} = -1 mA		2.4 3.3				
V _{OL}	Q outputs	V _{CC} = 4.5 V, I _{OL} = 12 mA		0.25 0.4		0.25 0.4		V
		V _{CC} = 4.5 V, I _{OL} = 24 mA				0.35 0.5		
	Status flags	V _{CC} = 4.5 V, I _{OL} = 4 mA		0.25 0.4		0.25 0.4		
		V _{CC} = 4.5 V, I _{OL} = 8 mA				0.35 0.5		
I _{OZH}		V _{CC} = 5.5 V, V _O = 2.7 V		20		20		μA
I _{OZL}		V _{CC} = 5.5 V, V _O = 0.4 V		-20		-20		μA
I _I		V _{CC} = 5.5 V, V _I = 7 V		0.1		0.1		mA
I _{IH}		V _{CC} = 5.5 V, V _I = 2.7 V		20		20		μA
I _{IL}		V _{CC} = 5.5 V, V _I = 0.4 V		-0.2		-0.2		mA
I _O ‡		V _{CC} = 5.5 V, V _O = 2.25 V		-30 -112		-30 -112		mA
I _{CC}		V _{CC} = 5.5 V		88 143		88 133		mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_OS.

2
LSI Devices

SN54ALS233A, SN74ALS233A
16 × 5 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = --MIN to MAX				UNIT
			'ALS233A			SN54ALS233A		SN74ALS233A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}	LDCK↑		40		25	30		MHz		
	UNCK↑		40		25	30				
t _{pd}	LDCK↑	Any Q	24	44	7	52	7	48	ns	
t _{pd}	UNCK↑	Any Q	19	29	9	35	9	33	ns	
t _{PLH}	LDCK↑	EMPTY	18	25	9	30	9	28	ns	
t _{PHL}	UNCK↑	EMPTY	18	25	9	33	10	30	ns	
t _{PHL}	RST↓	EMPTY	13	19	6	24	6	22	ns	
t _{pd}	LDCK↑	EMPTY+1	22	31	10	40	10	37	ns	
t _{pd}	UNCK↑	EMPTY+1	22	31	9	40	10	37	ns	
t _{PLH}	RST↓	EMPTY+1	19	27	8	32	8	31	ns	
t _{pd}	LDCK↑	FULL-1	23	32	11	38	12	36	ns	
t _{pd}	UNCK↑	FULL-1	23	32	11	39	12	36	ns	
t _{PLH}	RST↓	FULL-1	20	28	10	34	11	32	ns	
t _{PHL}	LDCK↑	FULL	21	28	10	35	12	33	ns	
t _{PLH}	UNCK↑	FULL	17	24	8	29	9	27	ns	
t _{PLH}	RST↓	FULL	18	27	8	32	9	30	ns	
t _{en}	OE↑	Q	8	13	1	16	2	15	ns	
t _{dis}	OE↓	Q	8	12	2	20	2	17	ns	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN74AS250

1-OF-16 DATA GENERATORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

D2910, DECEMBER 1983—REVISED JANUARY 1986

- 4-Line to 1-Line Multiplexer that can Select 1 and 16 Data Inputs
- Applications:
 - Boolean Function Generator
 - Parallel-to-Serial Converter
 - Data Source Selector
- Buffered 3-State Bus Driver Inputs Permit Multiplexing from N Lines to One Line
- Dependable Texas Instruments Quality and Reliability

description

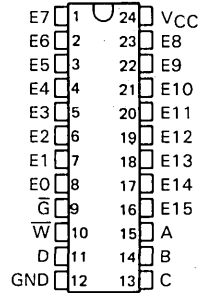
The 'AS250 provides full binary decoding to select one of sixteen data sources with an inverting \bar{W} output. The selected sources are buffered with symmetrical propagation delay times. This reduces the possibility of transients occurring at the output.

A buffered enable output (\bar{G}) may be used for n-line-to-one-line cascading. Taking the \bar{G} high will place the output in a high-impedance state. In the high-impedance state, the output neither loads nor drives the bus lines significantly.

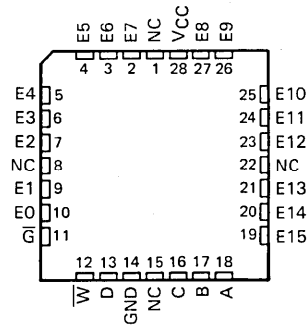
The enable (\bar{G}) does not affect the internal operations of the data selector/multiplexer. New data can be set up while the outputs are disabled.

The SN74AS250 is characterized for operation from 0°C to 70°C.

SN74AS250 . . . DW OR NT PACKAGE
(TOP VIEW)



SN74AS250 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

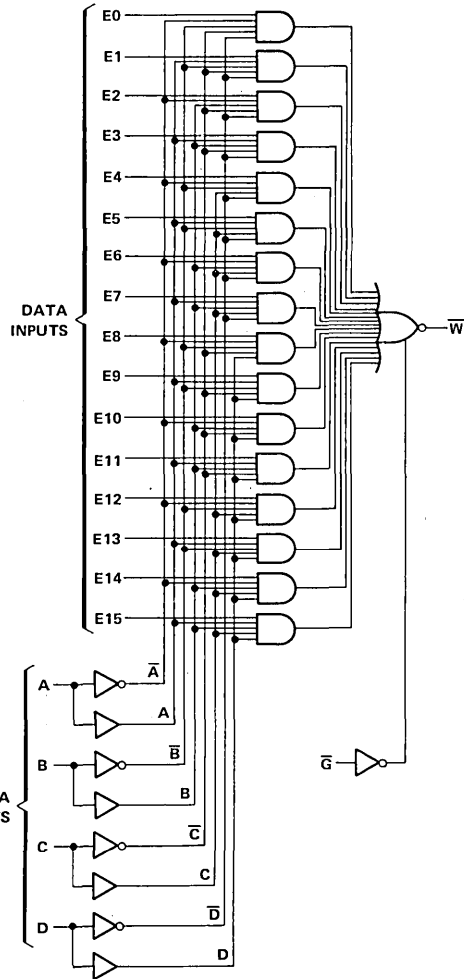
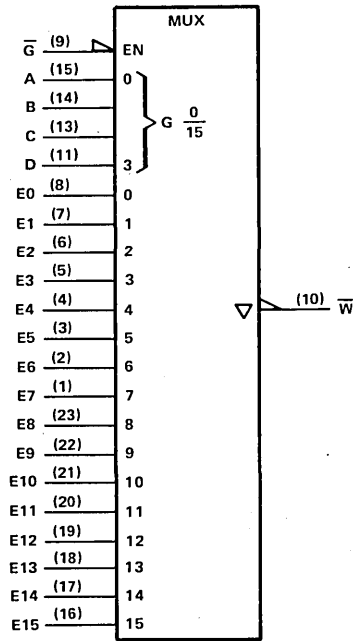
2
LSI Devices

SN74AS250

1-OF-16 DATA GENERATORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

logic symbol†

logic diagram (positive logic)



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW or NT packages.

2

LSI Devices

SN74AS250
1-OF-16 DATA GENERATORS/MULTIPLEXERS
WITH 3-STATE OUTPUTS

FUNCTION TABLE

INPUT						OUTPUT
G	A	B	C	D	Ei	W
L	L	L	L	L	E0	E0
L	H	L	L	L	E1	E1
L	L	H	L	L	E2	E2
L	H	H	L	L	E3	E3
L	L	L	H	L	E4	E4
L	H	L	H	L	E5	E5
L	L	H	H	L	E6	E6
L	H	H	H	L	E7	E7
L	L	L	L	H	E8	E8
L	H	L	L	H	E9	E9
L	L	H	L	H	E10	E10
L	H	H	L	H	E11	E11
L	L	L	H	H	E12	E12
L	H	L	H	H	E13	E13
L	L	H	H	H	E14	E14
L	H	H	H	H	E15	E15
H	X	X	X	X	X	Z

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

2
LSI Devices

SN74AS250

1-OF-16 DATA GENERATORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT	
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2	V	
V_{OH}	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $I_{OH} = -2 \text{ mA}$	$V_{CC}-2$			V	
	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -15 \text{ mA}$	2.4	3.3			
V_{OL}	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 48 \text{ mA}$		0.35	0.5	V	
I_{OZH}	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.7 \text{ V}$			50	μA	
I_{OZL}	$V_{CC} = 5.5 \text{ V}$, $V_O = 0.4 \text{ V}$			-50	μA	
I_I	$V_{CC} = 5.5 \text{ V}$, $V_I = 7 \text{ V}$			0.1	mA	
I_{IH}	$V_{CC} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$			20	μA	
I_{IL}	$V_{CC} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$			-0.5	mA	
I_O^\ddagger	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.25 \text{ V}$	-30		-112	mA	
I_{CC}	$V_{CC} = 5.5 \text{ V}$	Outputs high		26	42	mA
		Outputs low		31	50	
		Outputs disabled		30	48	

†All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

2

LSI Devices

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $R_1 = 500 \Omega$, $R_2 = 500 \Omega$, $T_A = 0^\circ\text{C to } 70^\circ\text{C}$			UNIT
			MIN	TYP†	MAX	
t_{PLH}	DATA	\bar{W}	3		8	ns
t_{PHL}			2		6	
t_{PLH}	SELECT	\bar{W}	4		13	ns
t_{PHL}			4		10	
t_{PZH}	\bar{G}	\bar{W}	2		7	ns
t_{PZL}			4		20	
t_{PHZ}	\bar{G}	\bar{W}	2		6	ns
t_{PLZ}			2		6	

†All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS280, SN54AS280, SN74ALS280, SN74AS280 9-BIT PARITY GENERATORS/CHECKERS

D2661, DECEMBER 1982—REVISED AUGUST 1985

- Generates Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bits Parity
- Can Be Used to Upgrade Existing Systems Using MSI Parity Circuits
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

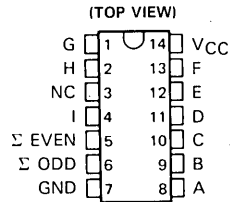
These universal, monolithic, nine-bit parity generators/checkers utilize Advanced Schottky high-performance circuitry and feature odd and even outputs to facilitate operation of either odd or even parity application. The word-length capability is easily expanded by cascading.

These devices can be used to upgrade the performance of most systems utilizing the '180 parity generator/checker. Although the 'ALS280 and 'AS280 are implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4 and the absence of any internal connection at pin 3. This permits the 'ALS280 and 'AS280 to be substituted for the '180 in existing designs to produce an identical function even if the devices are mixed with existing '180's.

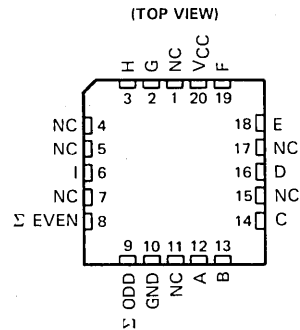
All 'AS280 inputs are buffered to lower the drive requirements.

The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

SN54ALS280, SN54AS280 . . . J PACKAGE
SN74ALS280, SN74AS280 . . . D OR N PACKAGE



SN54ALS280, SN54AS280 . . . FK PACKAGE
SN74ALS280, SN74AS280 . . . FN PACKAGE

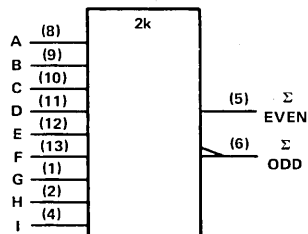


NC—No internal connection†

FUNCTION TABLE

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0,2,4,6,8	H	L
1,3,5,7,9	L	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

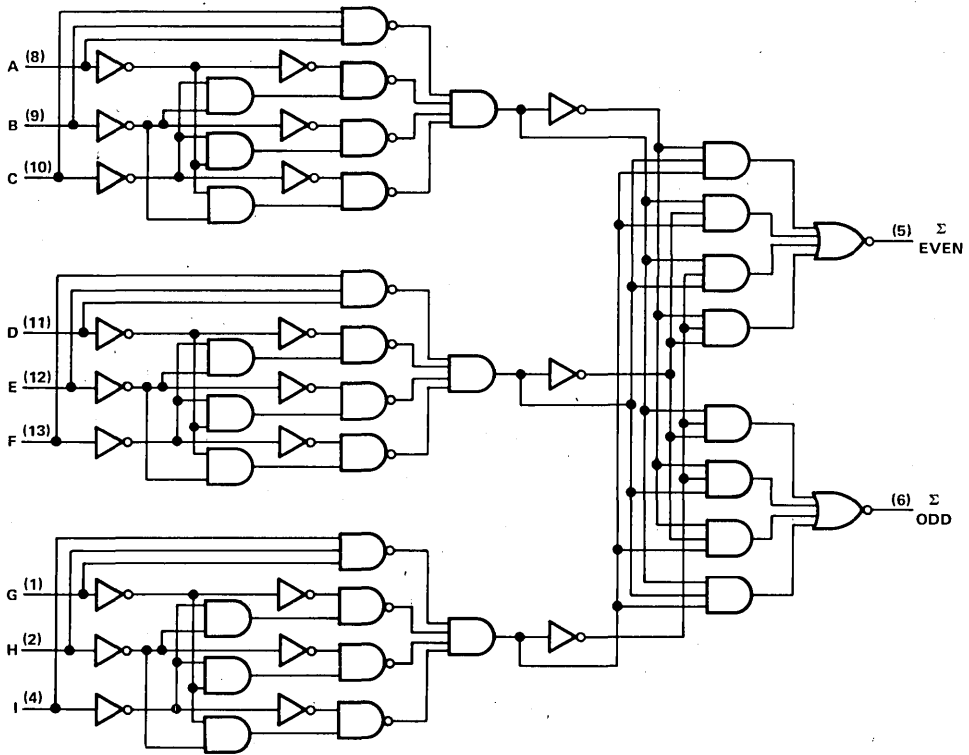
**TEXAS
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SN54ALS280, SN74ALS280
9-BIT PARITY GENERATORS/CHECKERS

logic diagram



2
LSI Devices

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Operating free-air temperature range: SN54ALS280	-55°C to 125°C
SN74ALS280	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

	SN54ALS280			SN74ALS280			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage	0.8			0.8			V
I_{OH} High-level output current	-1			-2.6			mA
I_{OL} Low-level output current	12			24			mA
T_A Operating free-air temperature	-55			0			70 °C

SN54ALS280, SN74ALS280 9-BIT PARITY GENERATORS/CHECKERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS280		SN74ALS280		UNIT		
		MIN	TYP†	MAX	MIN		TYP†	MAX
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2		-1.2	V	
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA	V _{CC} -2		V _{CC} -2			V	
	V _{CC} = 4.5 V, I _{OH} = -1 mA	2.4	3.3					
	V _{CC} = 4.5 V, I _{OH} = -2.6 mA			2.4	3.2			
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 12 mA	0.25	0.4	0.25	0.4		V	
	V _{CC} = 4.5 V, I _{OL} = 24 mA			0.35	0.5			
I _I	V _{CC} = 5.5 V, V _I = 7 V			0.1		0.1	mA	
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V			20		20	μA	
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V			-0.1		-0.1	mA	
I _O ‡	V _{CC} = 5.5 V, V _O = 2.25 V	-30		-112	-30	-112	mA	
I _{CC}	V _{CC} = 5.5 V		10	16		10	16	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R _L = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX			UNIT	
			ALS280			SN54ALS280		SN74ALS280		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
t _{PLH}	Any	Σ Even	12	16	3	24	3	20	ns	
t _{PHL}			12	17	3	24	3	20		
t _{PLH}	Any	Σ Odd	12	16	3	24	3	20	ns	
t _{PHL}			13	18	4	26	4	22		

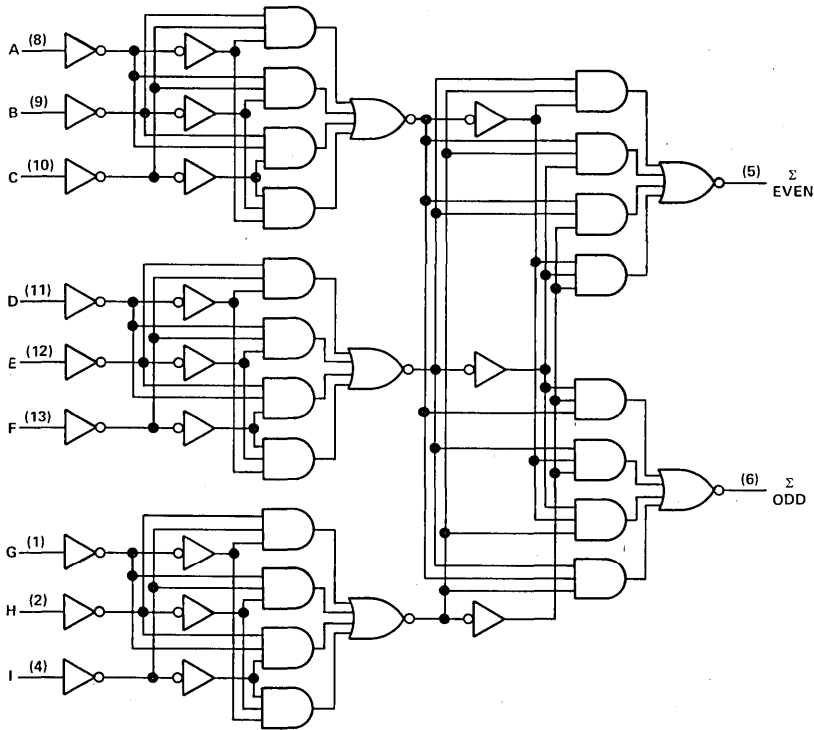
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

2

LSI Devices

SN54AS280, SN74AS280
9-BIT PARITY GENERATORS/CHECKERS

logic diagram



2
 LSI Devices

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

- Supply voltage, V_{CC} 7 V
- Input voltage 7 V
- Operating free-air temperature range: SN54AS280 -55°C to 125°C
- SN74AS280 0°C to 70°C
- Storage temperature range -65°C to 150°C

recommended operating conditions

	SN54AS280			SN74AS280			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage	0.8			0.8			V
I_{OH} High-level output current	-2			-2			mA
I_{OL} Low-level output current	20			20			mA
T_A Operating free-air temperature	-55			0			70 °C

SN54AS280, SN74AS280 9-BIT PARITY GENERATORS/CHECKERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS280		SN74AS280		UNIT
		MIN	TYP†	MAX	MIN	
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$		-1.2		-1.2	V
V_{OH}	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $I_{OH} = -2 \text{ mA}$	$V_{CC}-2$		$V_{CC}-2$		V
V_{OL}	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 20 \text{ mA}$	0.35	0.5	0.35	0.5	V
I_I	$V_{CC} = 5.5 \text{ V}$, $V_I = 7 \text{ V}$		0.1		0.1	mA
I_{IH}	$V_{CC} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$		20		20	μA
I_{IL}	$V_{CC} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$		-0.5		-0.5	mA
I_{O}^{\ddagger}	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.25 \text{ V}$	-30	-112	-30	-112	mA
I_{CC}	$V_{CC} = 5.5 \text{ V}$	25	40	25	35	mA

†All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $R_L = 500 \Omega$, $T_A = \text{MIN to MAX}$				UNIT
			SN54AS280		SN74AS280		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Σ Even	3	13	3	12	ns
t_{PHL}			3	12.5	3	11	
t_{PLH}	Any	Σ Odd	3	13	3	12	ns
t_{PHL}			3	12.5	3	11.5	

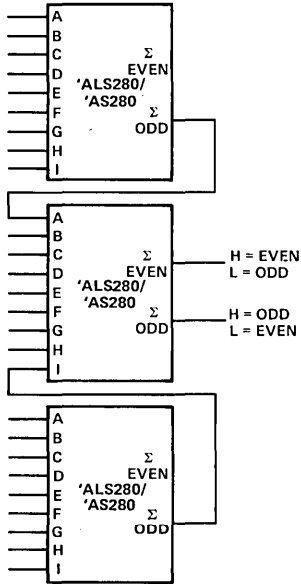
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

2
LSI Devices

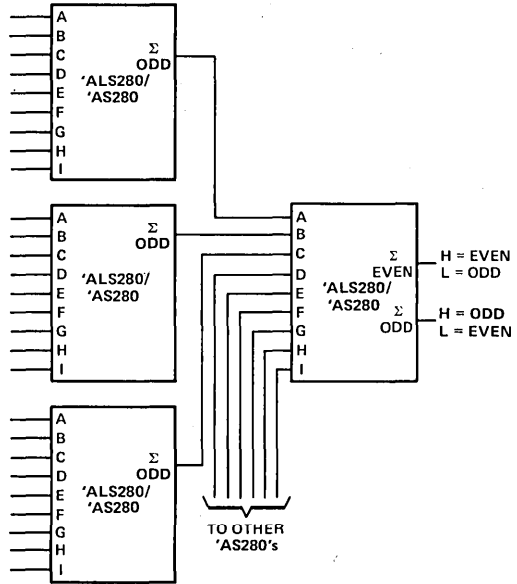
SN54ALS280, SN54AS280, SN74ALS280, SN74AS280
9-BIT PARITY GENERATORS/CHECKERS

TYPICAL APPLICATION DATA

25-LINE PARITY/GENERATOR CHECKER



81-LINE PARITY/GENERATOR CHECKER



Three 'ALS280/'AS280 can be used to implement a 25-line parity generator/checker.

As an alternative, the Σ ODD outputs of two or three parity generators/checkers can be decoded with a 2-input ('S86 or 'LS86) or 3-input ('S135) exclusive-OR gate for 18- or 27-line parity applications.

Longer word lengths can be implemented by cascading 'ALS280/'AS280. As shown here, parity can be generated for word lengths up to 81 bits.

2

LSI Devices

SN54AS286, SN74AS286 9-BIT PARITY GENERATORS/CHECKER WITH BUS DRIVER PARITY I/O PORT

D2809, DECEMBER 1983—REVISED AUGUST 1985

- Generates Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bits Parity
- Direct Bus Connection for Parity Generation or for Checking by Using the Parity I/O Port
- Glitch-Free Bus During Power Up/Down
- Package Options Include both Plastic and Ceramic Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

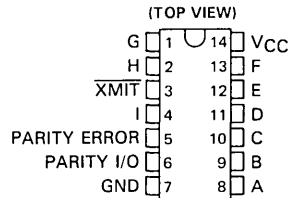
The SN54AS286 and SN74AS286 universal nine-bit parity generators/checkers feature a local output for parity checking and a 48-milliampere bus-driving parity I/O port for parity generation/checking. The word-length capability is easily expanded by cascading.

The $\overline{\text{XMIT}}$ control input is implemented specifically to accommodate cascading. When $\overline{\text{XMIT}}$ is low the parity tree is disabled and PE will remain at a high logic level regardless of the input levels. When $\overline{\text{XMIT}}$ is high the parity tree is enabled. The Parity Error output will indicate a parity error when either an even number of inputs (A through I) are high and Parity I/O is forced to a low logic level, or when an odd number of inputs are high and Parity I/O is forced to a high logic level.

The I/O control circuitry was designed so that the I/O port will remain in the high-impedance state during power-up or power-down to prevent bus glitches.

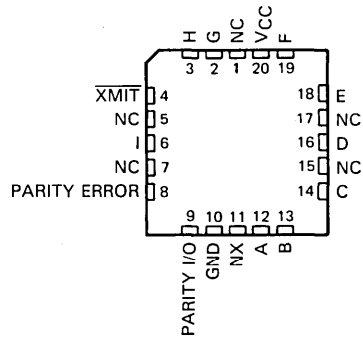
The SN54AS286 is characterized for operation over the full military range of -55°C to 125°C . The SN74AS286 is characterized for operation from 0°C to 70°C .

SN54AS286 . . . J PACKAGE
SN74AS286 . . . D OR N PACKAGE



SN54AS286 . . . FK PACKAGE
SN74AS286 . . . FN PACKAGE

(TOP VIEW)



NC—No internal connection

2

LSI Devices

SN54AS286, SN74AS286

9-BIT PARITY GENERATORS/CHECKER

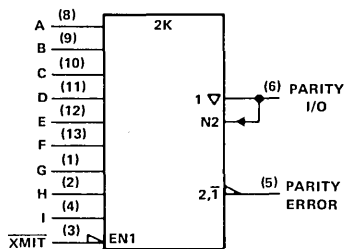
WITH BUS DRIVER PARITY I/O PORT

FUNCTION TABLE

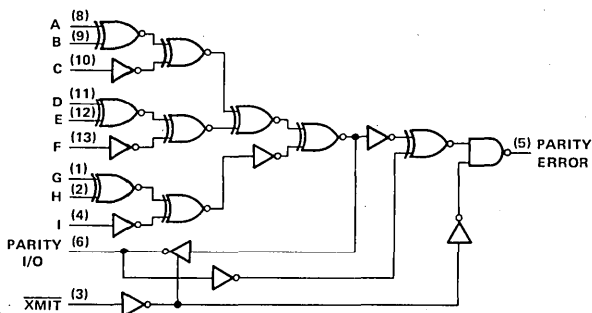
NUMBER OF INPUTS (A THRU I) THAT ARE HIGH	$\overline{\text{XMIT}}$	PARITY I/O	PARITY ERROR
0, 2, 4, 6, 8	I	H	H
1, 3, 5, 7, 9	I	L	H
0, 2, 4, 6, 8	h	h	H
	h	l	L
1, 3, 5, 7, 9	h	h	L
	h	l	H

h — high input level l — low input level
H — high output level L — low output level

logic symbol†



logic diagram (positive logic)



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range: SN54AS286	-55°C to 125°C
SN74AS286	0°C to 70°C
Storage temperature	-65°C to 140°C

recommended operating conditions

	SN54AS286			SN74AS286			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current	Parity error		-2	Parity I/O		-15	mA
	Parity I/O		-12	Parity error		-2	
I_{OL} Low-level output current	Parity error		20	Parity I/O		48	mA
	Parity I/O		32	Parity error		20	
T_A Operating free-air temperature	-55	125		0	70		°C

SN54AS286, SN74AS286
9-BIT PARITY GENERATORS/CHECKER
WITH BUS DRIVER PARITY I/O PORT

electrical characteristics over recommended free-air temperature range
(unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS286		SN74AS286		UNIT		
		MIN	TYP†	MAX	MIN		TYP†	MAX
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA	-1.2		-1.2		V		
V _{OH}	All outputs	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -2 mA		V _{CC} -2		V		
	Parity I/O	V _{CC} = 4.5 V, I _{OH} = -3 mA		2.4	2.9		2.4	3
		V _{CC} = 4.5 V, I _{OH} = -12 mA		2.4				
V _{OL}	Parity error	V _{CC} = 4.5 V, I _{OL} = 20 mA		0.35	0.5	0.35	0.5	
		V _{CC} = 4.5 V, I _{OL} = 32 mA		0.5				
	Parity I/O	V _{CC} = 4.5 V, I _{OL} = 48 mA				0.5		
I _I	Parity I/O	V _{CC} = 5.5 V, V _I = 5.5 V		0.1		0.1		
	All other inputs	V _{CC} = 5.5 V, V _I = 7 V		0.1		0.1		
I _{IH}	Parity I/O‡	V _{CC} = 5.5 V, V _I = 2.7 V		50		50		
	All other inputs			20		20		
I _{IL}	Parity I/O‡	V _{CC} = 5.5 V, V _I = 0.4 V		0.5		-0.5		
	All other inputs			0.5		-0.5		
I _O [§]	V _{CC} = 5.5 V, V _O = 2.25 V	-30	-112	-30	-112	mA		
I _{CC}	Transmit			30	43	30	43	
	Receive	V _{CC} = 5.5 V		35	50	35	50	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state current.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX				UNIT
			SN54AS286		SN74AS286		
			MIN	MAX	MIN	MAX	
t _{PLH}	Any A thru I	Parity I/O	3	17	3	15	ns
t _{PHL}			3	15	3	14	
t _{PLH}	Any A thru I	Parity error	3	20	3	16.5	ns
t _{PHL}			3	18	3	16.5	
t _{PLH}	Parity I/O	Parity error	3	10	3	9	ns
t _{PHL}			3	10	3	9	
t _{PZH}	XMIT	Parity I/O	3	14	3	13	ns
t _{PZL}			3	17	3	16	
t _{PHZ}			3	13	3	11.5	
t _{PLZ}			3	11	3	10	

NOTE 1: Load circuit and voltage waveforms as shown in Section 1.

SN54AS286, SN74AS286
9-BIT PARITY GENERATORS/CHECKER
WITH BUS DRIVER PARITY I/O PORT

TYPICAL APPLICATION DATA

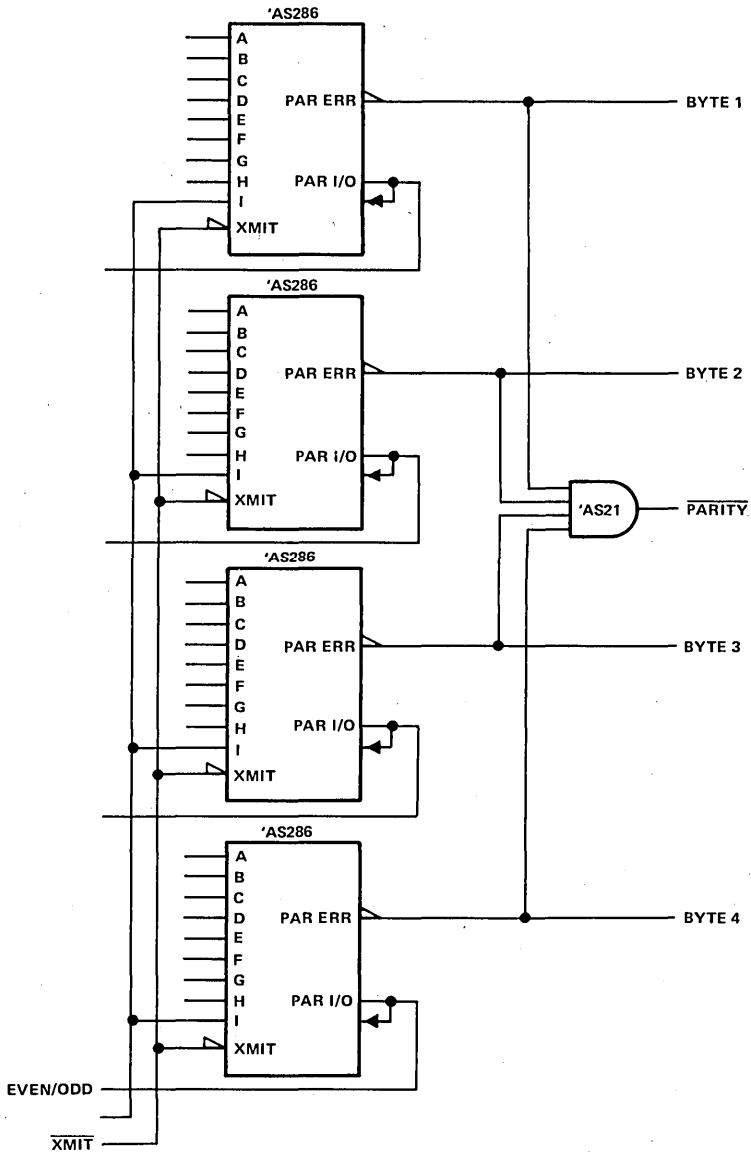


FIGURE 1. 32-BIT PARITY GENERATOR/CHECKER

Figure 1 shows a 32-bit parity generator/checker with output polarity-switching, parity error detection, and parity on every byte.

SN54AS286, SN74AS286
9-BIT PARITY GENERATORS/CHECKER
WITH BUS DRIVER PARITY I/O PORT

TYPICAL APPLICATION DATA

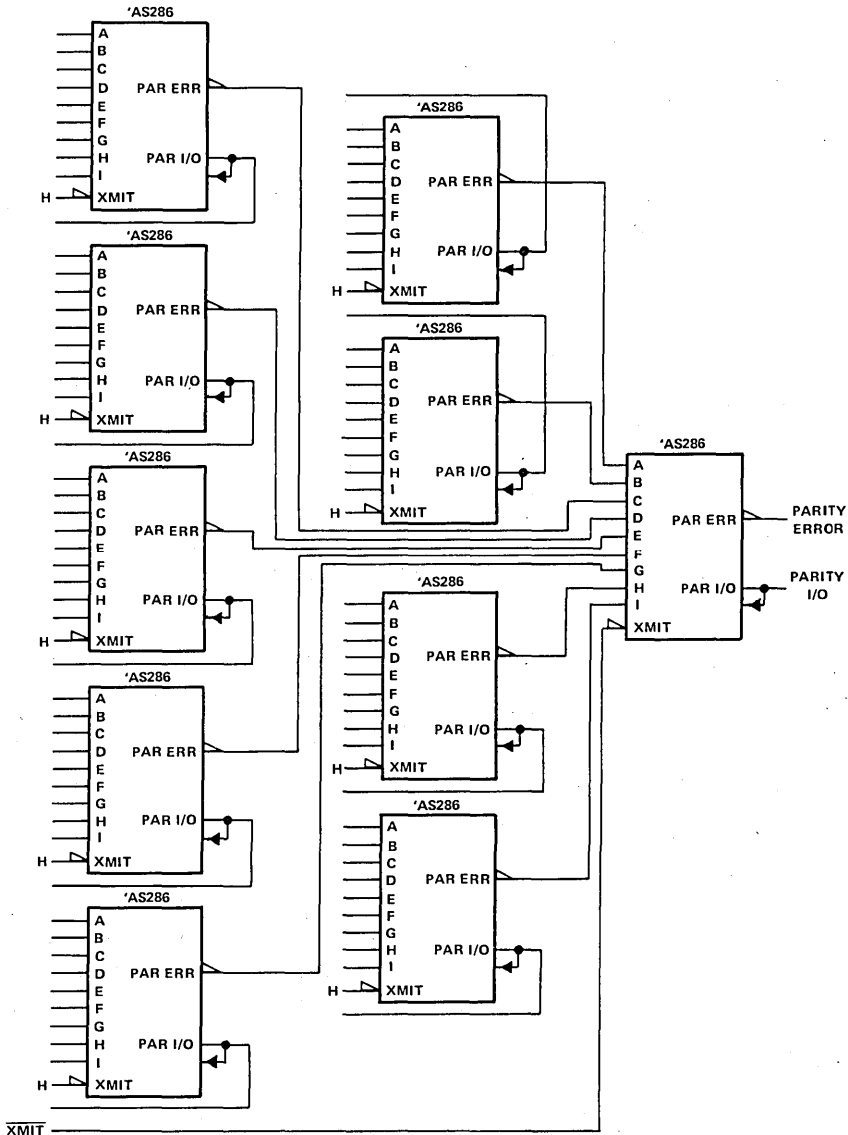


FIGURE 2. 90-BIT PARITY GENERATOR/CHECKER WITH PARITY ERROR DETECTION

In Figure 2, a 90-bit parity generator/checker with the $\overline{\text{XMIT}}$ on the last stage is available for use with parity detection.

2
LSI Devices

2

LSI Devices

SN54LS610 THRU SN54LS613, SN74LS610 THRU SN74LS613 MEMORY MAPPERS

D2549, JANUARY 1981—REVISED DECEMBER 1985

- Expands 4 Address Lines to 12 Address Lines
- Designed for Paged Memory Mapping
- Output Latches Provided on 'LS610 and 'LS611
- Choice of 3-State or Open-Collector Map Outputs
- Compatible with TMS9900 and Other Microprocessors

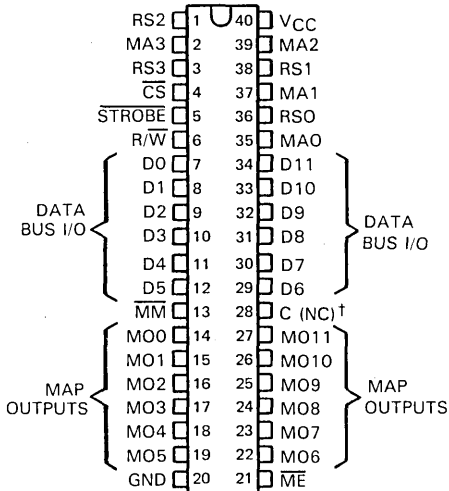
DEVICE	OUTPUTS LATCHED	MAP OUTPUT TYPE
'LS610	Yes	3-State
'LS611	Yes	Open-Collector
'LS612	No	3-State
'LS613	No	Open-Collector

description

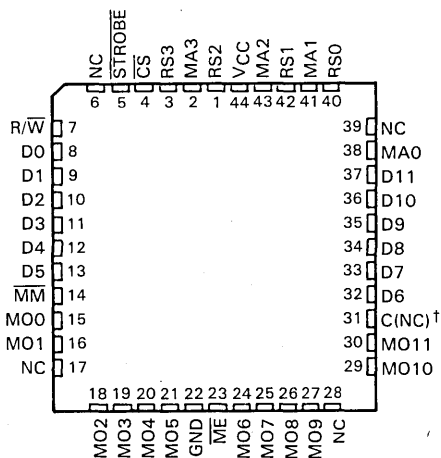
Each 'LS610 through 'LS613 memory-mapper integrated circuit contains a 4-line to 16-line decoder, a 16-word by 12-bit RAM, 16 channels of 2-line to 1-line multiplexers, and other miscellaneous circuitry on a monolithic chip. Each 'LS610 and 'LS611 also contains 12 latches with an enable control.

The memory mappers are designed to expand a microprocessor's memory address capability by eight bits. Four bits of the memory address bus (see System Block Diagram) can be used to select one of 16 map registers that contain 12 bits each. These 12 bits are presented to the system memory address bus through the map output buffers along with the unused memory address bits from the CPU. However, addressable memory space without reloading the map registers is the same as would be available with the memory mapper left out. The addressable memory space is increased only by periodically reloading the map registers from the data bus. This configuration lends itself to memory utilization of 16 pages of $2^{(n-4)}$ registers each without reloading (n = number of address bits available from CPU).

SN54LS'... JD PACKAGE
SN74LS'... JD OR N PACKAGE
(TOP VIEW)



SN54LS'... FK PACKAGE
SN74LS'... FN PACKAGE
(TOP VIEW)



† This pin has no internal connection on 'LS612 and 'LS613
NC—No internal connection

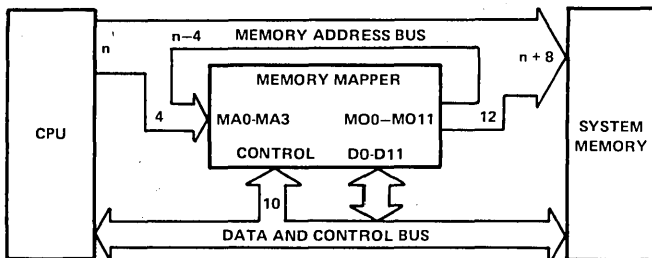
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SN54LS610 THRU SN54LS613, SN74LS610 THRU SN74LS613 MEMORY MAPPERS



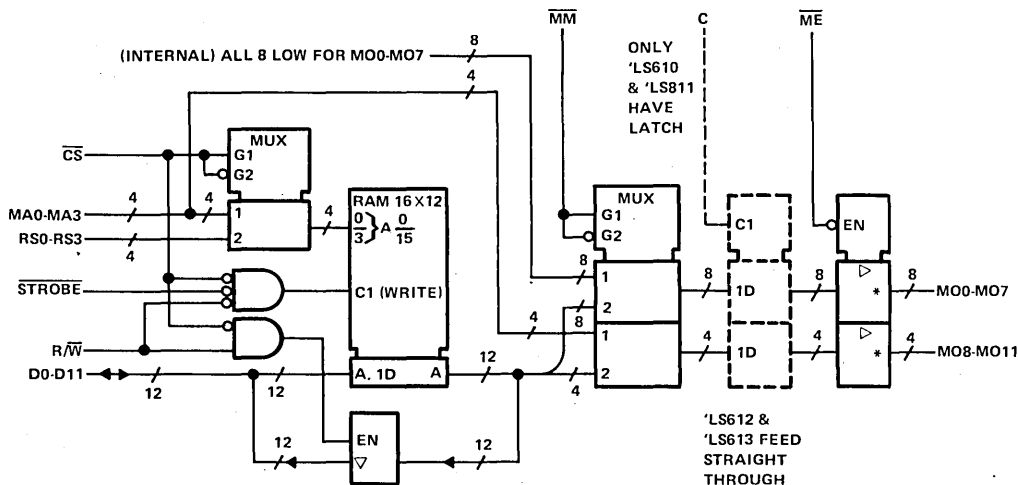
SYSTEM BLOCK DIAGRAM

These devices have four modes of operation: read, write, map, and pass. Data may be read from or loaded into the map register selected by the register select inputs (RS0 thru RS3) under control of R/W whenever chip select (\overline{CS}) is low. The data I/O takes place on the data bus D0 thru D7. The map operation will output the contents of the map register selected by the map address inputs (MA0 thru MA3) when \overline{CS} is high and \overline{MM} (map mode control) is low. The 'LS612 and 'LS613 output stages are transparent in this mode, while the 'LS610 and 'LS611 outputs may be transparent or latched. When \overline{CS} and \overline{MM} are both high (pass mode), the address bits on MA0 thru MA3 appear at MO8-MO11, respectively, (assuming appropriate latch control) with low levels in the other bit positions on the map outputs.

2

LSI Devices

logic diagram (positive logic)



*'LS610 and 'LS612 have 3-state (∇) map outputs.
'LS611 and 'LS613 have open-collector (\square) map outputs.

**SN54LS610 THRU SN54LS613, SN74LS610 THRU SN74LS613
MEMORY MAPPERS**

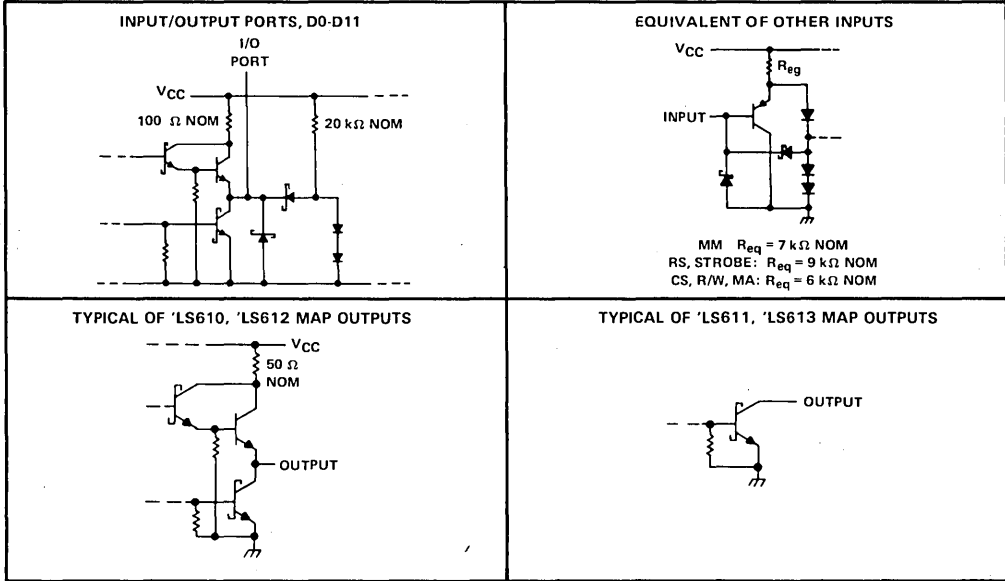
PIN		DESCRIPTION
NO.	NAME	
7-12 29-34	D0 thru D11	I/O connections to data and control bus used for reading from and writing to the map register selected by RSO-RS3 when \overline{CS} is low. Mode controlled by R/\overline{W} .
36, 38, 1, 3	RS0 thru RS3	Register select inputs for I/O operations.
6	R/\overline{W}	Read or write control used in I/O operations to select the condition of the data bus. When high, the data bus outputs are active for reading the map register. When low, the data bus is used to write into the register.
5	\overline{STROBE}	Strobe input used to enter data into the selected map register during I/O operations.
4	\overline{CS}	Chip select input. A low input level selects the memory mapper (assuming more than one used) for an I/O operation.
35, 37, 39, 2	MA0 thru MA3	Map address inputs to select one of 16 map registers when in map mode (\overline{MM} low and \overline{CS} high).
14-19, 22-27	MO0 thru MO11	Map outputs. Present the map register contents to the system memory address bus in the map mode. In the pass mode, these outputs provide the map address data on MO8-MO11 and low levels on MO0-MO7.
13	\overline{MM}	Map mode input. When low, 12 bits of data are transferred from the selected map register to the map outputs. When high (pass mode), the 4 bits present on the map address inputs MA0-MA3 are passed to the map outputs MO8-MO11, respectively, while MO0-MO7 are set low.
21	\overline{ME}	Map enable for the map outputs. A low level allows the outputs to be active while a high input level puts the outputs at high impedance.
28	C	Latch enable input for the 'LS610 and 'LS611 (no internal connection for 'LS612 and 'LS613). A high level will transparently pass data to the map outputs. A low level will latch the outputs.
40, 20	VCC, GND	5 V power supply and network ground (substrate) pins.

2

LSI Devices

SN54LS610 THRU SN54LS613, SN74LS610 THRU SN74LS613 MEMORY MAPPERS

schematics of inputs and outputs



2

LSI Devices

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: Data Bus I/O	5.5 V
All other inputs	7 V
Operating free-air temperature range: SN54LS610 through SN54LS613	-55°C to 125°C
SN74LS610 through SN74LS613	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

SN54LS610, SN54LS612, SN74LS610, SN74LS612 MEMORY MAPPERS WITH 3-STATE MAP OUTPUTS

recommended operating conditions

				SN54LS610			SN74LS610			UNIT
				SN54LS612			SN74LS612			
				MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage			2			2			V
V _{IL}	Low-level input voltage					0.7			0.8	V
I _{OH}	High-level output current		MO			-12			-15	mA
			D			-1		-2.6		
I _{OL}	Low-level output current		MO			12			24	mA
			D			4		8		
t _{AVCL}	Address setup time (AV before C low)	'LS610 only	See Figure 2	30			30			ns
t _{SLSH}	Duration of strobe input pulse		See Figure 1	75			75			ns
t _{CSSL}	\overline{CS} setup time (\overline{CS} low to strobe low)			20			20			ns
t _{WLSL}	R/ \overline{W} setup time (R/ \overline{W} low to strobe low)			20			20			ns
t _{RVSL}	RS setup time (RS valid to strobe low)			20			20			ns
t _{DVSH}	Data setup time (D0-D11 valid to strobe high)			75			75			ns
t _{SHCSH}	\overline{CS} hold time (Strobe high to \overline{CS} high)			20			20			ns
t _{SHWH}	R/ \overline{W} hold time (Strobe high to R/ \overline{W} high)			20			20			ns
t _{SHRX}	RS hold time (Strobe high to RS invalid)			20			20			ns
t _{SHDX}	Data hold time (Strobe high to D0-D11 invalid)			20			20			ns
T _A	Operating free-air temperature				-55		125	0		70

2

LSI Devices

SN54LS610, SN54LS612, SN74LS610, SN74LS612 MEMORY MAPPERS WITH 3-STATE MAP OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]	SN54LS610 SN54LS612			SN74LS610 SN74LS612			UNIT
			MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V _{IK}		V _{CC} = MIN, I _I = -18 mA	-1.5			-1.5			V
V _{OH}	MO	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OH} = -3 mA			2.4			V
	D		I _{OH} = MAX			2			
V _{OL}	MO	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OL} = 12 mA			0.25 0.4			V
	D		I _{OL} = 24 mA			0.35 0.5			
			I _{OL} = 4 mA			0.25 0.4			
			I _{OL} = 8 mA			0.35 0.5			
I _{OZH}		V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = MAX, V _O = 2.7 V	20			20			μA
I _{OZL}	MO	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = MAX, V _O = 0.4 V	-20			-20			μA
	D		-400			-400			
I _I	D	V _{CC} = MAX	V _I = 5.5 V			0.1			mA
	All others		V _I = 7 V			0.1			
I _{IH}		V _{CC} = MAX, V _I = 2.7 V	20			20			μA
I _{IL}		V _{CC} = MAX, V _I = 0.4 V	-0.4			-0.4			mA
I _{OS} [§]	MO	V _{CC} = MAX	-40			-225			mA
	D		-30			-130			
I _{CC}	V _{CC} = MAX		Outputs high			112 180			mA
			Outputs low			112 180			
			Outputs disabled			150 230			

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§]Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, C_L = 45 pF to GND

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS610		'LS612		UNIT
				MIN	TYP	MAX	MIN	
t _{CSDLV}	Access (enable) time	\overline{CS} ↓	DO-11	28 50		26 50		ns
t _{WHDV}	Access (enable) time	R/W↑	DO-11	20 35		20 35		ns
t _{TRVDV}	Access time	RS	DO-11	49 75		39 75		ns
t _{WLDDZ}	Disable time	R/W↓	DO-11	32 50		30 50		ns
t _{CSHDZ}	Disable time	\overline{CS} ↑	DO-11	42 65		38 65		ns
t _{ELQV}	Access (enable) time	\overline{ME} ↓	MO0-11	19 30		17 30		ns
t _{CSHQV}	Access time	\overline{CS} ↑	MO0-11	56 85		48 85		ns
t _{MLQV}	Access time	\overline{MM} ↓	MO0-11	25 40		22 40		ns
t _{CHQV}	Access time	C↑	MO0-11	24 40				ns
t _{AVQV1}	Access time (MM low)	MA	MO0-11	46 70		39 70		ns
t _{MHQV}	Access time	\overline{MM} ↑	MO0-11	24 40		22 40		ns
t _{AVQV2}	Propagation time (MM high)	MA	MO8-11	19 30		13 30		ns
t _{EHQZ}	Disable time	\overline{ME} ↑	MO0-11	14 25		14 25		ns

NOTES: 2. Access times are tested as t_{PLH} and t_{PHL} or t_{PZH} or t_{PZL}. Disable times are tested as t_{PHZ} and t_{PLZ}.

3. Load circuits and voltage waveforms are shown in Section 1.

SN54LS611, SN54LS613, SN74LS611, SN74LS613 MEMORY MAPPERS WITH OPEN-COLLECTOR MAP OUTPUTS

recommended operating conditions

				SN54LS611 SN54LS613			SN74LS611 SN74LS613			UNIT			
				MIN	NOM	MAX	MIN	NOM	MAX				
V _{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V			
V _{IH}	High-level input voltage			2			2			V			
V _{IL}	Low-level input voltage			0.7			0.8			V			
V _{OH}	High-level output voltage			MO			5.5			V			
I _{OH}	High-level output current			D			-1			-2.6	mA		
I _{OL}	Low-level output current			MO			12			24	mA		
				D			4			8			
t _{AVCL}	Address setup time (A _V before C low)	'LS611 only	See Figure 2	30			30			ns			
t _{SLSH}	Duration of strobe input pulse			75			75			ns			
t _{CSLSL}	CS setup time (CS low to strobe low)			20			20			ns			
t _{WLSL}	R/W setup time (R/W low to strobe low)			20			20			ns			
t _{RVSL}	RS setup time (RS valid to strobe low)			20			20			ns			
t _{DVSH}	Data setup time (D0-D11 valid to strobe high)			See Figure 1	75			75			ns		
t _{SHCSH}	CS hold time (Strobe high to CS high)				20			20			ns		
t _{SHWH}	R/W hold time (Strobe high to R/W high)				20			20			ns		
t _{SHRX}	RS hold time (Strobe high to RS invalid)				20			20			ns		
t _{SHDX}	Data hold time (Strobe high to D0-D11 invalid)				20			20			ns		
T _A	Operating free-air temperature				-55			125			0	70	°C

2

LSI Devices

SN54LS611, SN54LS613, SN74LS611, SN74LS613

MEMORY MAPPERS WITH OPEN-COLLECTOR MAP OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS611		SN74LS611		UNIT		
			SN54LS613	SN74LS613	MIN	TYP‡		MAX	MIN
V _{IK}		V _{CC} = MIN, I _I = -18 mA	-1.5		-1.5		V		
V _{OH}	D	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = MAX	2.4		2.4		V		
I _{OH}	MO	V _{CC} = MIN, V _{IH} = 2 V, V _{OH} = 5.5 V	0.1		0.1		mA		
V _{OL}	MO	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OL} = 12 mA		0.25 0.4		V		
			I _{OL} = 24 mA		0.35 0.5				
	D		I _{OL} = 4 mA		0.25 0.4				
			I _{OL} = 8 mA		0.35 0.5				
I _{OZH}	D	V _{CC} = MAX, V _{IL} = MAX, V _{IH} = 2 V, V _O = 2.7 V	20		20		μA		
I _{OZL}	D	V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.4 V	-0.4		-0.4		mA		
I _I	D	V _{CC} = MAX	V _I = 5.5 V		0.1		mA		
	All others		V _I = 7 V		0.1				
I _{IH}		V _{CC} = MAX, V _I = 2.7 V	20		20		μA		
I _{IL}		V _{CC} = MAX, V _I = 0.4 V	-0.4		-0.4		mA		
I _{OS} §	D	V _{CC} = MAX	-30	-130	-30	-130	mA		
I _{CC}		V _{CC} = MAX	Outputs high		100	170	100	170	mA
			Outputs low		100	170	100	170	
			Outputs disabled		110	200	110	200	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, C_L = 45 pF to GND

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS611		'LS613		UNIT		
				MIN	TYP	MAX	MIN		TYP	MAX
t _{CSDLV}	Access (enable) time	$\overline{CS}\downarrow$	D0-11	R _L = 2 kΩ, See Figure 1, See Notes 2 and 3	31	50	28	50	ns	
t _{WHDV}	Access (enable) time	R/ $\overline{W}\uparrow$	D0-11		23	35	21	35	ns	
t _{RDV}	Access time	RS	D0-11		51	75	47	75	ns	
t _{WLDZ}	Disable time	R/ $\overline{W}\downarrow$	D0-11		32	50	31	50	ns	
t _{CSHDZ}	Disable time	$\overline{CS}\uparrow$	D0-11		41	65	40	65	ns	
t _{ELOV}	Access (enable) time	$\overline{ME}\downarrow$	M00-11		R _L = 667 Ω, See Figure 2, See Notes 2 and 3	21	30	19	30	ns
t _{CSHQV}	Access time	$\overline{CS}\uparrow$	M00-11			57	90	53	90	ns
t _{MLQV}	Access time	MM \downarrow	M00-11			25	40	25	40	ns
t _{CHQV}	Access time	C \uparrow	M00-11			30	45			ns
t _{AVQV1}	Access time (MM low)	MA	M00-11			47	70	44	70	ns
t _{MHQV}	Access time	MM \uparrow	M00-11	31		50	31	50	ns	
t _{AVQV2}	Propagation time (MM high)	MA	M08-11	21		30	20	30	ns	
t _{EHQZ}	Disable time	ME \uparrow	M00-11	15		25	15	25	ns	

NOTES: 2. Access times are tested as t_{PLH} and t_{PHL} or t_{PHZ} and t_{PZL}. Disable times are tested as t_{PHZ} and t_{PZL}.

3. Load circuits and voltage waveforms are shown in Section 1.

SN54LS610 THRU SN54LS613, SN74LS610 THRU SN74LS613 MEMORY MAPPERS

explanation of letter symbols

This data sheet uses a new type of letter symbol based on JEDEC Standard 100 to describe time intervals. The format is:

t_{AB-CD}

where: subscripts A and C indicate the names of the signals for which changes of state or level or establishment of state or level constitute signal events assumed to occur first and last, respectively, that is, at the beginning and end of the time interval.

Subscripts B and D indicate the direction of the transitions and/or the final states or levels of the signals represented by A and C, respectively. One or two of the following is used:

- H = high or transition to high
- L = low or transition to low
- V = a valid steady-state level
- X = unknown, changing, or "don't care" level
- Z = high-impedance (off) state.

The hyphen between the B and C subscripts is omitted when no confusion is likely to occur. For these letter symbols on this data sheet, the signal names are further abbreviated as follows:

SIGNAL NAME	A AND C SUBSCRIPT	SIGNAL NAME	A AND C SUBSCRIPT
\overline{CS}	C	\overline{ME}	E
$\overline{DO-11}$	CS	\overline{MM}	M
$\overline{MA0-MA3}$	D	$\overline{R/W}$	W
$\overline{MO0-MO11}$	A	$\overline{RS0-RS3}$	R
	Q	STROBE	S

2
LSI Devices

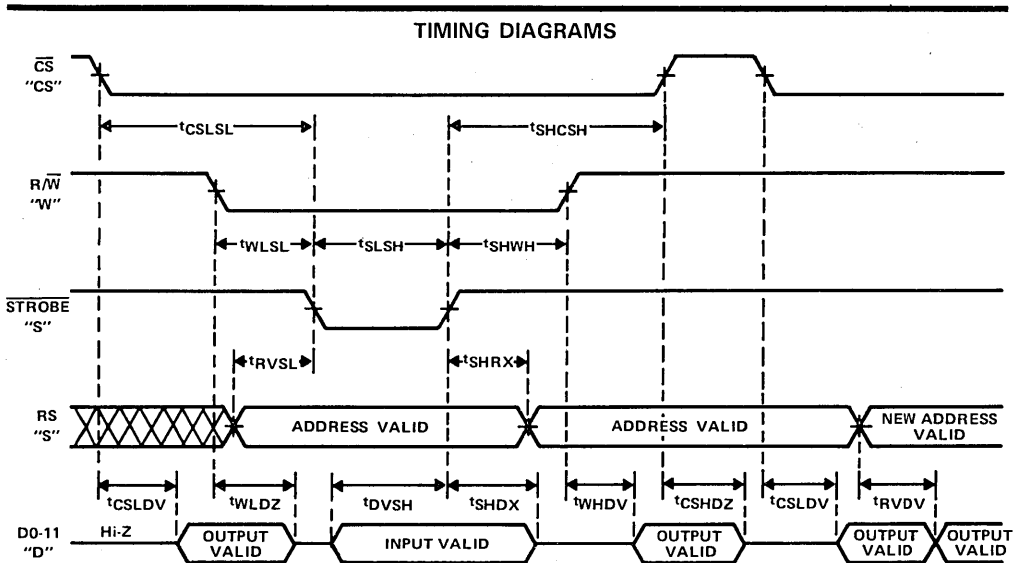


FIGURE 1. WRITE AND READ MODES

**SN54LS610 THRU SN54LS613, SN74LS610 THRU SN74LS613
MEMORY MAPPERS**

TIMING DIAGRAMS

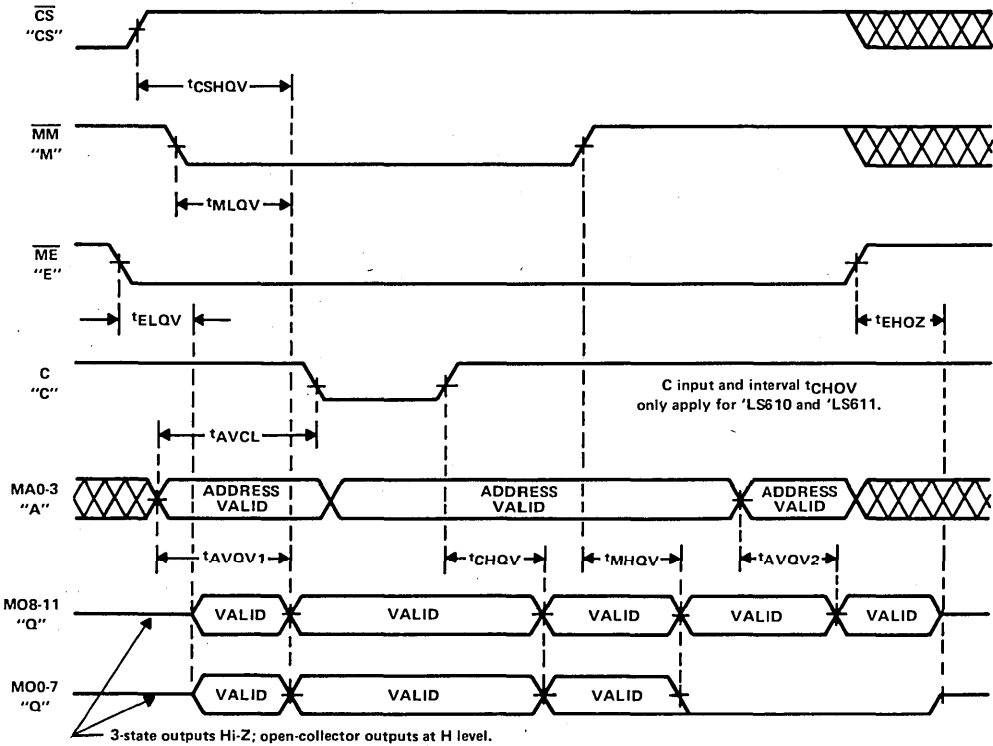


FIGURE 2. MAP AND PASS MODES

2

LSI Devices

SN54ALS616, SN54ALS617, SN74ALS616, SN74ALS617 16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

D2840, APRIL 1984—REVISED SEPTEMBER 1985

- Detects and Corrects Single-Bit Errors
- Detects and Flags Dual-Bit Errors
- Built-In Diagnostic Capability
- Fast Write and Read Cycle Processing Times
- Byte-Write Capability
- Dependable Texas Instruments Quality and Reliability

DEVICE	OUTPUT
'ALS616	3-State
'ALS617	Open-Collector

description

The 'ALS616 and 'ALS617 are 16-bit parallel error detection and correction circuits in 40-pin, 600-mil packages. The EDACs use a modified Hamming code to generate a 6-bit check word from a 16-bit data word. This check word is stored along with the data word during the memory write cycle. During memory read cycles, the 22-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

Single-bit errors in the 16-bit data word are flagged and corrected. Single-bit errors in the 6-bit check word are flagged, but the data word will remain unaltered. The 6-bit error syndrome code will pinpoint the error-generating location.

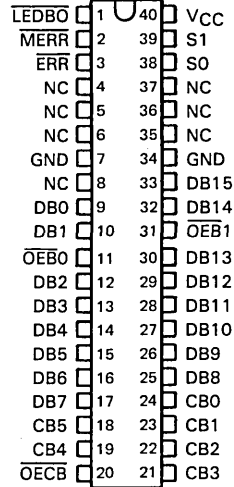
Dual-bit errors are flagged but not corrected. These errors may occur in any two bits of the 22-bit word from memory. The gross-error condition of all lows or all highs from memory will be detected. Otherwise, errors in three or more bits of the 22-bit word are beyond the capabilities of these devices to detect.

Read-modify-write (byte-control) operations can be performed with the 'ALS616 and 'ALS617 EDACs by using output latch enable, LEDBO, and individual OEBO and OEB1 byte control pins.

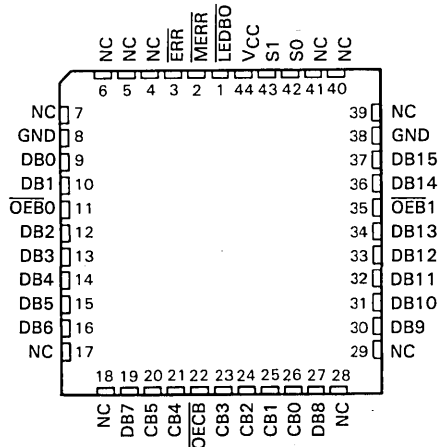
Diagnostics are performed on the EDACs by controls and internal paths that allow the user to read the contents of the DB and CB input latches. These will determine if the failure occurred in memory or in the EDAC.

The SN54ALS616 and SN54ALS617 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS616 and SN74ALS617 are characterized for operation from 0°C to 70°C.

SN54ALS616, SN54ALS617 . . . JD PACKAGE
SN74ALS616, SN74ALS617 . . . JD OR N PACKAGE
(TOP VIEW)



SN74ALS616, SN74ALS617 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

This document contains information on products in more than one phase of development. The status of each device is indicated on the page(s) specifying its electrical characteristics.

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2
LSI Devices

SN54ALS616, SN54ALS617, SN74ALS616, SN74ALS617

16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

TABLE 1. WRITE CONTROL FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1 S0	DATA I/O	DB CONTROL	DB OUTPUT LATCH	CHECK I/O	CB CONTROL	ERROR FLAGS	
				$\overline{OEB0}$ & $\overline{OEB1}$	$\overline{LEDB0}$		\overline{OECB}	ERR	MERR
Write	Generate check word	L L	Input	H	X	Output check bits†	L	H	H

† See Table 2 for details on check bit generation.

memory write cycle details

During a memory write cycle, the check bits (CB0 thru CB5) are generated internally in the EDAC by six 8-input parity generators using the 16-bit data word as defined in Table 2. These six check bits are stored in memory along with the original 16-bit data word. This 22-bit word will later be used in the memory read cycle for error detection and correction.

TABLE 2. PARITY ALGORITHM

CHECK WORD BIT	16-BIT DATA WORD															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CB0			X		X	X	X			X			X		X	X
CB1		X		X		X	X	X			X		X		X	X
CB2	X			X	X			X	X		X			X	X	
CB3	X	X	X				X	X			X	X	X			
CB4	X	X	X	X	X	X			X	X						
CB5									X	X	X	X	X	X	X	X

The six check bits are parity bits derived from the matrix of data bits as indicated by "X" for each bit.

error detection and correction details

During a memory read cycle, the 6-bit check word is retrieved along with the actual data. In order to be able to determine whether the data from memory is acceptable to use as presented to the bus, the error flags must be tested to determine if they are at the high level.

The first case in Table 3 represents the normal, no-error conditions. The EDAC presents highs on both flags. The next two cases of single-bit errors give a high on MERR and a low on ERR, which is the signal for a correctable error, and the EDAC should be sent through the correction cycle. The last three cases of double-bit errors will cause the EDAC to signal lows on both ERR and MERR, which is the interrupt indication for the CPU.

TABLE 3. ERROR FUNCTION

TOTAL NUMBER OF ERRORS	ERROR FLAGS	DATA CORRECTION	
			16-BIT DATA WORD
0	0	H H	Not applicable
1	0	L H	Correction
0	1	L H	Correction
1	1	L L	Interrupt
2	0	L L	Interrupt
0	2	L L	Interrupt

SN54ALS616, SN54ALS617, SN74ALS616, SN74ALS617

16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

TABLE 4. READ, FLAG, AND CORRECT FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL		DATA I/O	DB CONTROL		DB OUTPUT LATCH	CHECK I/O	CB CONTROL	ERROR FLAGS	
		S1	S0		$\overline{OE}B0$	$\overline{OE}B1$				$\overline{LE}DB0$	ERR
Read	Read & flag	H	L	Input	H		X	Input	H	Enabled [†]	
Read	Latch input data & check bits	H	H	Latched input data	H		L	Latched input check word	H	Enabled [†]	
Read	Output corrected data and syndrome bits	H	H	Output corrected data word	L		X	Output syndrome bits [‡]	L	Enabled [†]	

[†]See Table 3 for error description.

[‡]See Table 5 for error location.

Error detection is accomplished as the 6-bit check word and the 16-bit data word from memory are applied to the internal parity generators/checkers. If the parity of all six groupings of data and check bits are correct, it is assumed that no error has occurred and both error flags will be high.

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set low. The two-bit error is not correctable since the parity tree can only identify single-bit errors. Both error flags are set low when any two-bit error is detected.

Three or more simultaneous bit errors can cause the EDAC to believe that no error, a correctable error, or an uncorrectable error has occurred and will produce erroneous results in all three cases. It should be noted that the gross-error conditions of all highs will be detected.

As the corrected word is made available on the data I/O port (DB0 thru DB15), the check word I/O port (CB0 thru CB5) presents a 6-bit syndrome error code. This syndrome code can be used to locate the bad memory chip. See Table 5 for syndrome decoding.

2

LSI Devices

SN54ALS616, SN54ALS617, SN74ALS616, SN74ALS617

16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

TABLE 5. SYNDROME DECODING

SYNDROME BITS						ERROR
5	4	3	2	1	0	
L	L	L	L	L	L	2-bit
L	L	L	L	L	H	unc
L	L	L	L	H	L	unc
L	L	L	L	H	H	2-bit
L	L	L	H	L	L	unc
L	L	L	H	L	H	2-bit
L	L	L	H	H	L	unc
L	L	L	H	H	H	2-bit
L	L	H	L	L	L	unc
L	L	H	L	L	H	2-bit
L	L	H	L	H	L	2-bit
L	L	H	L	H	H	DB7
L	L	H	H	L	L	2-bit
L	L	H	H	L	H	unc
L	L	H	H	H	L	DB6
L	L	H	H	H	H	2-bit

SYNDROME BITS						ERROR
5	4	3	2	1	0	
L	H	L	L	L	L	unc
L	H	L	L	L	H	2-bit
L	H	L	L	H	L	2-bit
L	H	L	L	H	H	DB5
L	H	L	H	L	L	2-bit
L	H	L	H	L	H	DB4
L	H	L	H	H	L	DB3
L	H	L	H	H	H	2-bit
L	H	H	L	L	L	2-bit
L	H	H	L	L	H	DB2
L	H	H	L	H	L	DB1
L	H	H	L	H	H	2-bit
L	H	H	H	L	L	DB0
L	H	H	H	L	H	2-bit
L	H	H	H	H	L	2-bit
L	H	H	H	H	H	CB5

SYNDROME BITS						ERROR
5	4	3	2	1	0	
H	L	L	L	L	L	unc
H	L	L	L	L	H	2-bit
H	L	L	L	H	L	2-bit
H	L	L	L	H	H	DB15
H	L	L	H	L	L	2-bit
H	L	L	H	L	H	DB14
H	L	L	H	H	L	DB13
H	L	L	H	H	H	2-bit
H	L	H	L	L	L	2-bit
H	L	H	L	L	H	DB12
H	L	H	L	H	L	DB11
H	L	H	L	H	H	2-bit
H	L	H	H	L	L	DB10
H	L	H	H	L	H	2-bit
H	L	H	H	H	L	2-bit
H	L	H	H	H	H	CB4

SYNDROME BITS						ERROR
5	4	3	2	1	0	
H	H	L	L	L	L	2-bit
H	H	L	L	L	H	DB8
H	H	L	L	H	L	unc
H	H	L	L	H	H	2-bit
H	H	L	H	L	L	DB9
H	H	L	H	L	H	2-bit
H	H	L	H	H	L	2-bit
H	H	L	H	H	H	CB3
H	H	H	L	L	L	unc
H	H	H	L	L	H	2-bit
H	H	H	L	H	L	2-bit
H	H	H	L	H	H	CB2
H	H	H	H	L	L	2-bit
H	H	H	H	L	H	CB1
H	H	H	H	H	L	CB0
H	H	H	H	H	H	none

CB X = error in check bit X
 DB Y = error in data bit Y
 2-bit = double-bit error
 unc = uncorrectable multibit error

read-modify-write (byte control) operations

The 'ALS616 and 'ALS617 devices are capable of byte-write operations. The 22-bit word from memory must first be latched into the DB and CB input latches. This is easily accomplished by switching from the read and flag mode (S1 = H, S0 = L) to the latch input mode (S1 = H, S0 = H). The EDAC will then make any corrections, if necessary, to the data word and place it at the input of the output data latch. This data word must then be latched into the output data latch by taking $\overline{LEDB0}$ from a low to a high.

Byte control can now be employed on the data word through the $\overline{OEB0}$ or $\overline{OEB1}$ controls. $\overline{OEB0}$ controls DB0-DB7 (byte 0), $\overline{OEB1}$ controls DB8-DB15 (byte 1).

Placing a high on the byte control will disable the output and the user can modify the byte. If a low is placed on the byte control, then the original byte is allowed to pass onto the data bus unchanged. If the original data word is altered through byte control, a new check word must be generated before it is written back into memory. This is easily accomplished by taking control S1 and S0 low. Table 6 lists the read-modify-write functions.

2
LSI Devices

SN54ALS616, SN54ALS617, SN74ALS616, SN74ALS617 16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

TABLE 6. READ-MODIFY-WRITE FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL		BYTE _n [†]	$\overline{OE}B_n$ [†]	DB OUTPUT LATCH LEDBO	CHECK I/O	CB CONTROL	ERROR FLAG	
		S1	S0						ERR	MERR
Read	Read & Flag	H	L	Input	H	X	Input	H	Enabled	
Read	Latch input data & check bits	H	H	Latched Input data	H	L	Latched input check word	H	Enabled	
Read	Latch corrected data word into output latch	H	H	Latched output data word	H	H	Hi-Z Output Syndrome bits	H L	Enabled	
Modify/ write	Modify appropriate byte or bytes & generate new check word	L	L	Input modified BYTE0	H	H	Output check word	L	H H	
				Output unchanged BYTE0	L					

[†] $\overline{OE}B_0$ controls DB0-DB7 (BYTE0), $\overline{OE}B_1$ controls DB8-DB15 (BYTE1)

diagnostic operations

The 'ALS616 and 'ALS617 are capable of diagnostics that allow the user to determine whether the EDAC or the memory is failing. The diagnostic function tables will help the user to see the possibilities for diagnostic control.

In the diagnostic mode (S1 = L, S0 = H), the checkword is latched into the input latch while the data input latch remains transparent. This lets the user apply various data words against a fixed known checkword. If the user applies a diagnostic data word with an error in any bit location, the \overline{ERR} flag should be low. If a diagnostic data word with two errors in any bit location is applied, the \overline{MERR} flag should be low. After the checkword is latched into the input latch, it can be verified by taking \overline{OECB} low. This outputs the latched checkword. The diagnostic data word can be latched into the output data latch and verified via the \overline{LEDBO} control pin. By changing from the diagnostic mode (S1 = L, S0 = H), the user can verify that the EDAC will correct the diagnostic data word. Also, the syndrome bits can be produced to verify that the EDAC pinpoints the error location. Table 7 lists the diagnostic functions.

2
LSI Devices

SN54ALS616, SN54ALS617, SN74ALS616, SN74ALS617
16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

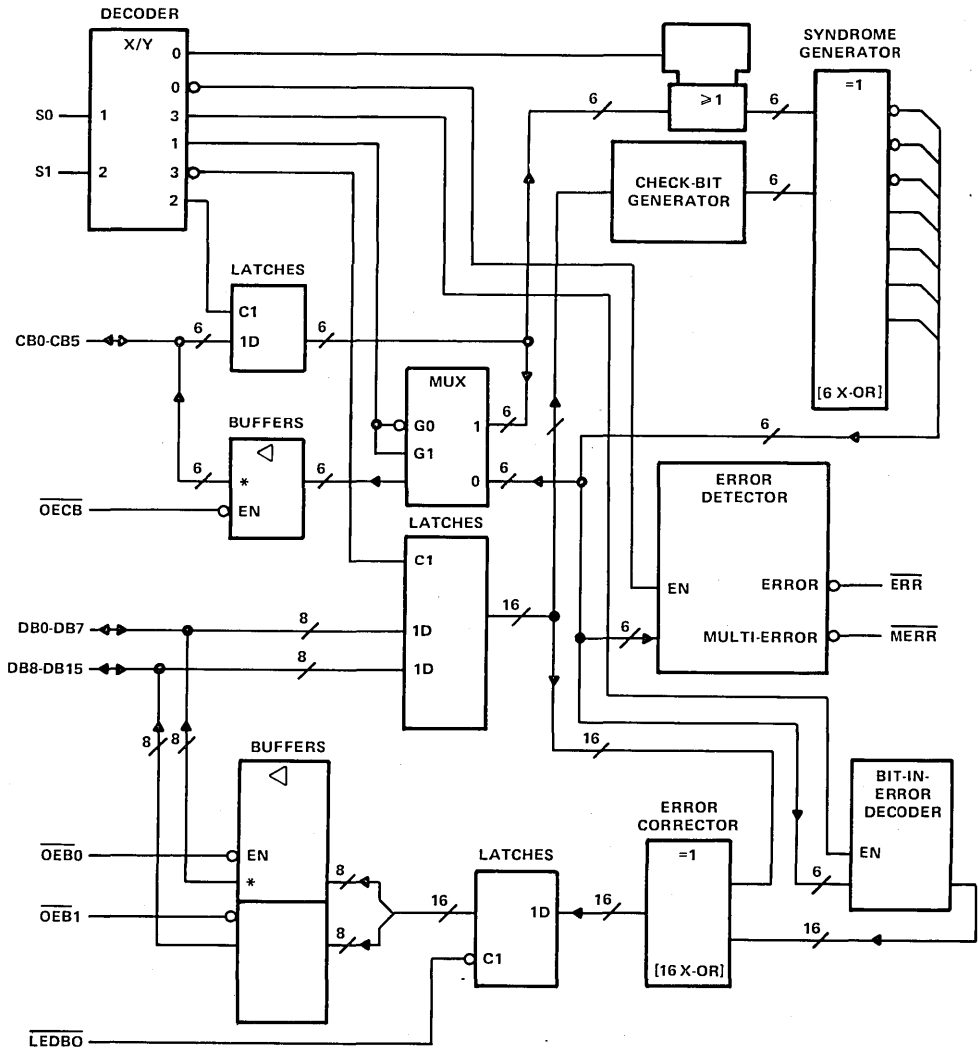
TABLE 7. DIAGNOSTIC FUNCTION

EDAC FUNCTION	CONTROL S1 S0	DATA I/O	DB BYTE CONTROL OEBn	DB OUTPUT LATCH LEDBO	CHECK I/O	CB CONTROL OECB	ERROR FLAGS	
							ERR	MERR
Read & flag	H L	Input correct data word	H	X	Input correct check bits	H	H	H
Latch input check word while data input latch remains transparent	L H	Input diagnostic data word [†]	H	L	Latched input check bits	H	Enabled	
Latch diagnostic data word into output latch	L H	Input diagnostic data word [†]	H	H	Output latched check bits Hi-Z	L H	Enabled	
Latch diagnostic data word into input latch	H H	Latched input diagnostic data word	H	H	Output syndrome bits Hi-Z	L H	Enabled	
Output diagnostic data word & syndrome bits	H H	Output diagnostic data word	L	H	Output syndrome bits Hi-Z	L H	Enabled	
Output corrected diagnostic data word & output syndrome bits	H H	Output corrected diagnostic data word	L	L	Output syndrome bits Hi-Z	L H	Enabled	

[†]Diagnostic data is a data word with an error in one bit location except when testing the MERR error flag. In this case, the diagnostic data word will contain errors in two bit locations.

SN54ALS616, SN54ALS617, SN74ALS616, SN74ALS617 16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

logic diagram (positive logic)



**ALS616 has 3-state (∇) check-bit and data outputs.
 *ALS617 has open-collector (\square) check-bit and data outputs.

2
LSI Devices

SN54ALS616, SN54ALS617, SN74ALS616, SN74ALS617

16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: CB and DB	5.5 V
All others	7 V
Operating case temperature range	SN54ALS616, SN54ALS617,..... -55 °C to 125 °C
Operating free-air temperature range, SN74ALS616, SN74ALS617	0 °C to 70 °C
Storage temperature range	-65 °C to 150 °C

recommended operating conditions

		SN54ALS616			SN74ALS616			UNIT
		SN54ALS617			SN74ALS617			
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage	0.8			0.8			V
V_{OH}	High-level output voltage	DB or CB 'ALS617			5.5			V
I_{OH}	High-level output current	ERR or MERR			-0.4			mA
		DB or CB 'ALS616			-1			
I_{OL}	Low-level output current	ERR or MERR			4			mA
		DB or CB			12			
t_w	Pulse duration	LEDBO low			25			ns
t_{su}	Setup time	(1) Data and check word before $S0\uparrow$ ($S1 = H$)		15		12		ns
		(2) $S0$ high before $\overline{LEDBO}\uparrow$ ($S1 = H$) [†]		45		45		
		(3) \overline{LEDBO} high before the earlier of $S0\uparrow$ or $S1\uparrow$		0		0		
		(4) \overline{LEDBO} high before $S1\uparrow$ ($S0 = H$)		0		0		
		(5) Diagnostic data word before $S1\uparrow$ ($S0 = H$)		28		12		
		(6) Diagnostic check word before the later of $S1\downarrow$ or $S0\downarrow$		15		12		
		(7) Diagnostic data word before $\overline{LEDBO}\uparrow$ ($S1 = L$ and $S0 = H$) [‡]		35		20		
t_h	Hold time	(8) Read-mode, $S0$ low and $S1$ high		35		30		ns
		(9) Data and check word after $S0\uparrow$ ($S1 = H$)		20		15		
		(10) Data word after $S1\uparrow$ ($S0 = H$)		20		15		
		(11) Check word after the later of $S1\downarrow$ or $S0\downarrow$		20		15		
		(12) Diagnostic data word after $\overline{LEDBO}\uparrow$ ($S1 = L$, $S0 = H$) [‡]		0		0		
t_{corr}	Correction time (see Figure 1)	70			65			ns
T_C	Operating case temperature	-55			125			°C
T_A	Operating free-air temperature				0			70 °C

[†]These times ensure that corrected data is saved in the output data latch.

[‡]These times ensure that the diagnostic data word is saved in the output data latch.

SN54ALS616, SN74ALS616

16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

'ALS616 electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS616		SN74ALS616		UNIT
		MIN	TYP† MAX	MIN	TYP† MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA	-1.5		-1.5		V
V _{OH}	All outputs	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA		V _{CC} -2		V
	DB or CB	V _{CC} = 4.5 V, I _{OH} = -1 mA		2.4	3.3	
		V _{CC} = 4.5 V, I _{OH} = -2.6 mA				
V _{OL}	ERR or MERR	V _{CC} = 4.5 V, I _{OH} = 4 mA		0.25	0.4	V
		V _{CC} = 4.5 V, I _{OL} = 8 mA				
	DB or CB	V _{CC} = 4.5 V, I _{OL} = 12 mA		0.25	0.4	
		V _{CC} = 4.5 V, I _{OL} = 24 mA				
				0.35	0.5	
I _I	SO or S1	V _{CC} = 5.5 V, V _I = 7 V		0.1		mA
	DB or CB	V _{CC} = 5.5 V, V _I = 5.5 V		0.1		
I _{IH}	SO or S1	V _{CC} = 5.5 V, V _I = 2.7 V		20		μA
	DB or CB‡			20		
I _{IL}	SO or S1	V _{CC} = 5.5 V, V _I = 0.4 V		-0.4		mA
	DB or CB‡			-0.1		
I _O §	V _{CC} = 5.5 V, V _O = 2.25 V	-30	-112	-30	-112	mA
I _{CC}	V _{CC} = 5.5 V See Note 1	110 190		110 170		mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

NOTE 1: I_{CC} is measured with S0 and S1 at 4.5 V and all CB and DB pins grounded.

'ALS616 switching characteristics, V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_C = -55°C to 125°C for SN54ALS616, T_A = 0°C to 70°C for SN74ALS616

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ALS616		SN74ALS616		UNIT
				MIN	MAX	MIN	MAX	
t _{pd}	DB and CB	ERR	S1 = H, S0 = L, R _L = 500 Ω	10	43	10	40	ns
	DB	ERR	S1 = L, S0 = H, R _L = 500 Ω	10	43	10	40	
t _{pd}	DB and CB	MERR	S1 = H, S0 = L, R _L = 500 Ω	15	65	15	55	ns
	DB	MERR	S1 = L, S0 = H, R _L = 500 Ω	15	65	15	55	
t _{pd}	S0↓ and S1↓	CB	R1 = R2 = 500 Ω	10	60	10	49	ns
t _{pd}	DB	CB	S1 = L, S0 = L, R1 = R2 = 500 Ω	10	60	10	49	ns
t _{pd}	LEDB0↓	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω	7	35	7	30	ns
t _{pd}	S1↑	CB	S0 = H, R1 = R2 = 500 Ω	10	50	10	50	ns
t _{en}	0ECB↓	CB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	30	2	27	ns
t _{dis}	0ECB↑	CB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	30	2	27	ns
t _{en}	0EB0 and 0EB1↓	DB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	30	2	27	ns
t _{dis}	0EB0 and 0EB1↑	DB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	30	2	27	ns

SN54ALS617, SN74ALS617
16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

**PRODUCT
 PREVIEW**

'ALS617 electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS617			SN74ALS617			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	ERR or MERR V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA	V _{CC} -2			V _{CC} -2			V
I _{OH}	DB or CB V _{CC} = 4.5 V, V _{OH} = 5.5 V			0.1			0.1	mA
V _{OL}	ERR or MERR	V _{CC} = 4.5 V, I _{OH} = 4 mA	0.25	0.4	0.25	0.4	V	
		V _{CC} = 4.5 V, I _{OL} = 8 mA			0.35	0.5		
	DB or CB	V _{CC} = 4.5 V, I _{OL} = 12 mA	0.25	0.4	0.25	0.4		
		V _{CC} = 4.5 V, I _{OL} = 24 mA			0.35	0.5		
I _I	S0 or S1 V _{CC} = 5.5 V, V _I = 7 V			0.1		0.1	mA	
	DB or CB	V _{CC} = 5.5 V, V _I = 5.5 V		0.1		0.1		
I _{IH}	S0 or S1	V _{CC} = 5.5 V, V _I = 2.7 V	20		20		μA	
	DB or CB‡		20		20			
I _{IL}	S0 or S1	V _{CC} = 5.5 V, V _I = 0.4 V	-0.4		-0.4		mA	
	DB or CB‡		-0.1		-0.1			
I _O §	ERR or MERR V _{CC} = 5.5 V, V _O = 2.25 V	-30	-112	-30	-112	mA		
I _{CC}	V _{CC} = 5.5 V See Note 1	110			110			mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_OS.

NOTE 1: I_{CC} is measured with S0 and S1 at 4.5 V and all CB and DB pins grounded.

'ALS617 switching characteristics, V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_C = -55°C to 125°C for SN54ALS617, T_A = 0°C to 70°C for SN74ALS617

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ALS617			SN74ALS617			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t _{pd}	DB and CB	ERR	S1=H, S0=L, R _L =500 Ω	26			26			ns
	DB	ERR	S1=L, S0=H, R _L =500 Ω	26			26			
t _{pd}	DB and CB	MERR	S1=H, S0=L, R _L =500 Ω	40			40			ns
			S1=L, S0=H, R _L =500 Ω	40			40			
t _{pd}	S0↑ and S1↓	CB	R _L =680 Ω	40			40			ns
t _{pd}	DB	CB	S1=L, S0=L, R _L =680 Ω	40			40			ns
t _{pd}	LEDB0↓	DB	S1=X, S0=H, R _L =680 Ω	26			26			ns
t _{pd}	S1↑	CB	S0=H, R _L =680 Ω	40			40			ns
t _{PLH}	0ECB↑	CB	S1=X, S0=H, R _L =680 Ω	24			24			ns
t _{PHL}	0ECB↓	CB	S1=X, S0=H, R _L =680 Ω	24			24			ns
t _{PLH}	0EB0 and 0EB1↑	DB	S1=X, S0=H, R _L =680 Ω	24			24			ns
t _{PHL}	0EB0 and 0EB1↓	DB	S1=X, S0=H, R _L =680 Ω	24			24			ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

Additional information on these products can be obtained from the factory as it becomes available.

2
LSI Devices

SN54ALS616, SN54ALS617, SN74ALS616, SN74ALS617 16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

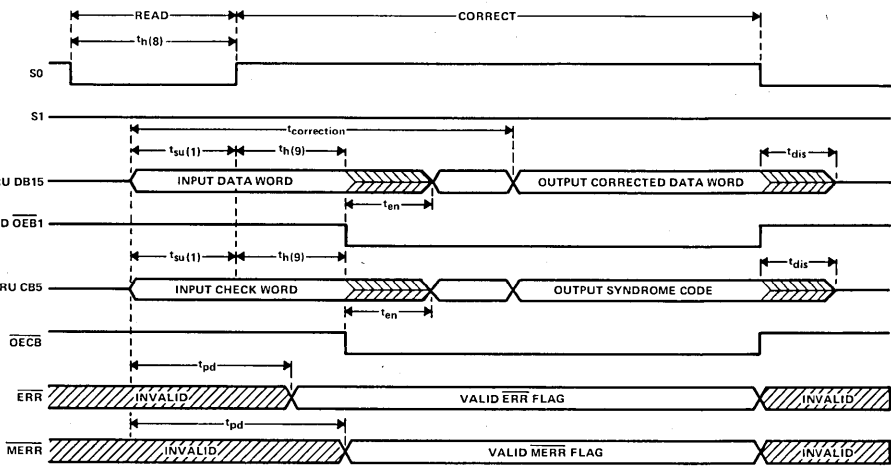


FIGURE 1. READ, FLAG, AND CORRECT MODE SWITCHING WAVEFORMS

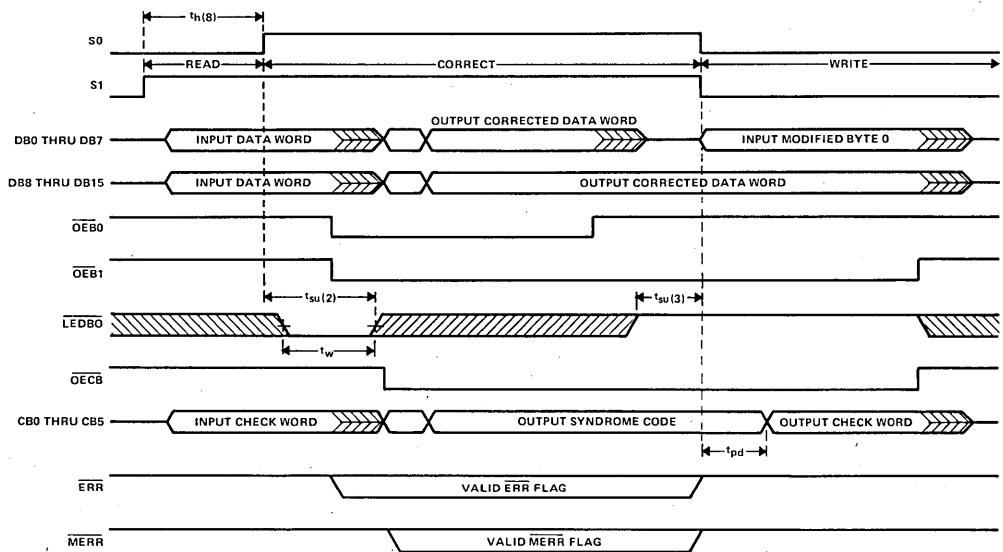


FIGURE 2. READ, CORRECT, MODIFY MODE SWITCHING WAVEFORMS

2
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SN54ALS616, SN54ALS617, SN74ALS616, SN74ALS617
16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

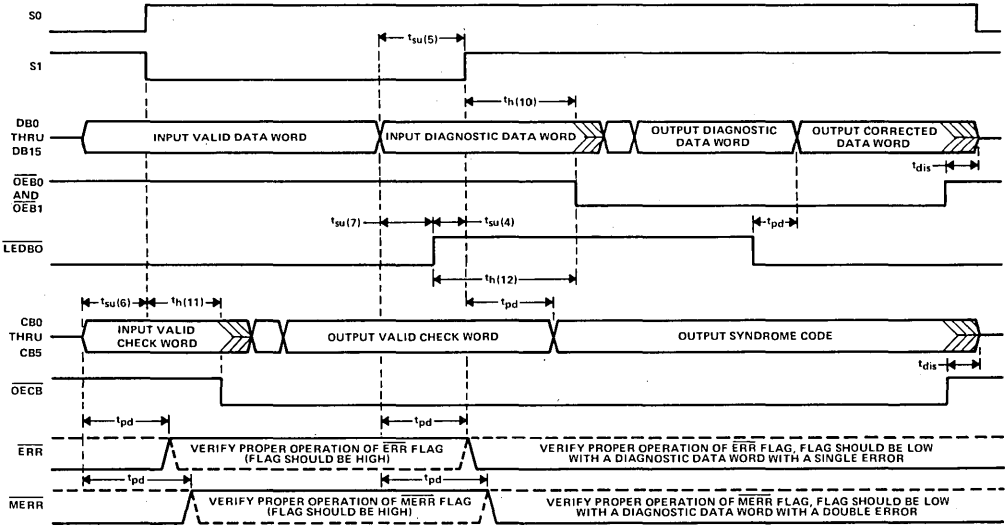


FIGURE 3. DIAGNOSTIC MODE SWITCHING WAVEFORM

2 LSI Devices

SN54ALS632A, SN54ALS633 THRU SN54ALS635 SN74ALS632A, SN74ALS633 THRU SN74ALS635 32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

D2661, DECEMBER 1982—REVISED DECEMBER 1985

- Detects and Corrects Single-Bit Errors
- Detects and Flags Dual-Bit Errors
- Built-In Diagnostic Capability
- Fast Write and Read Cycle Processing Times
- Byte-Write Capability . . . 'ALS632A and 'ALS633
- Dependable Texas Instruments Quality and Reliability

DEVICE	PACKAGE	BYTE-WRITE	OUTPUT
'ALS632A	52-pin	yes	3-State
'ALS633	52-pin	yes	Open-Collector
'ALS634	48-pin	no	3-State
'ALS635	48-pin	no	Open-Collector

description

The 'ALS632A and 'ALS633 through 'ALS635 devices are 32-bit parallel error detection and correction circuits (EDACs) in 52-pin ('ALS632A and 'ALS633) or 48-pin ('ALS634 and 'ALS635) 600-mil packages. The EDACs use a modified Hamming code to generate a 7-bit check word from a 32-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 39-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

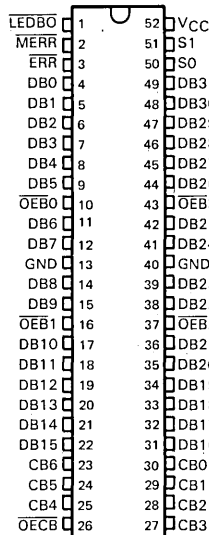
Single-bit errors in the 32-bit data word are flagged and corrected.

Single-bit errors in the 7-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 32-bit data word is not in error. The correction cycle will simply pass along the original 32-bit data word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These errors may occur in any two bits of the 39-bit data word from memory (two errors in the 32-bit data word, two errors in the 7-bit check word, or one error in each word). The gross-error condition of all lows or all highs from memory will be detected. Otherwise, errors in three or more bits of the 39-bit word are beyond the capabilities of these devices to detect.

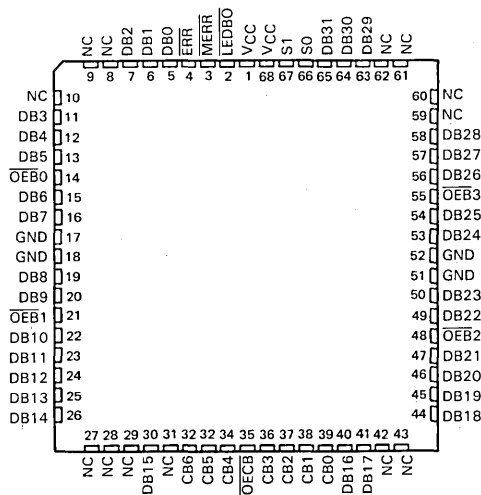
'ALS632A, 'ALS633 . . . JD PACKAGE

(TOP VIEW)



'ALS632A, 'ALS633 . . . FN PACKAGE

(TOP VIEW)



NC—No internal connection

2
LSI Devices

This document contains information on products in more than one phase of development. The status of each device is indicated on the page(s) specifying its electrical characteristics.

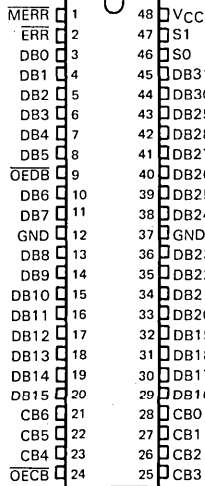


SN54ALS632A, SN54ALS633 THRU SN54ALS635 SN74ALS632A, SN74ALS633 THRU SN74ALS635 32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

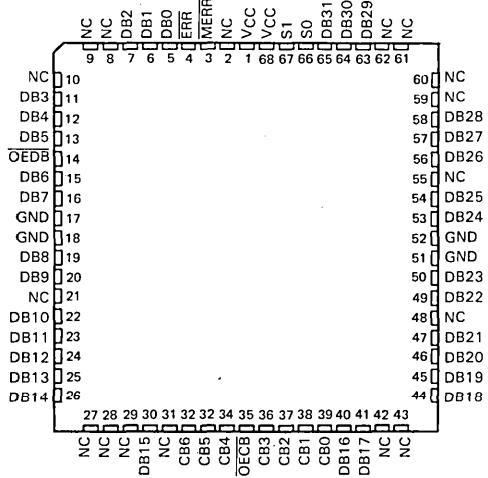
Read-modify-write (byte-control) operations can be performed with the 'ALS632A and 'ALS633 EDACs by using output latch enable, LEDBO, and the individual OEBO thru OEB3 byte control pins.

Diagnostics are performed on the EDACs by controls and internal paths that allow the user to read the contents of the DB and CB input latches. These will determine if the failure occurred in memory or in the EDAC.

'ALS634, 'ALS635 . . . JD PACKAGE
(TOP VIEW)



'ALS634, 'ALS635 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

TABLE 1. WRITE CONTROL FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL		DATA I/O	DB CONTROL OE _{Bn} OR OEDB	DB OUTPUT LATCH ('ALS632A, 'ALS633) LEDBO	CHECK I/O	CB CONTROL		ERROR FLAGS	
		S1	S0					OECEB	ERR	MERR	
Write	Generate check word	L	L	Input	H	X	Output check bits†	L	H	H	H

†See Table 2 for details on check bit generation.

memory write cycle details

During a memory write cycle, the check bits (CB0 thru CB6) are generated internally in the EDAC by seven 16-input parity generators using the 32-bit data word as defined in Table 2. These seven check bits are stored in memory along with the original 32-bit data word. This 32-bit word will later be used in the memory read cycle for error detection and correction.

**SN54ALS632A, SN54ALS633 THRU SN54ALS635
SN74ALS632A, SN74ALS633 THRU SN74ALS635
32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS**

TABLE 2. PARITY ALGORITHM

CHECK WORD BIT	32-BIT DATA WORD																															
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CB0	X		X	X		X				X		X	X	X		X			X		X		X	X	X	X		X				X
CB1				X	X		X		X		X		X	X	X				X		X		X	X	X	X		X	X	X	X	X
CB2	X		X			X	X		X		X	X			X	X		X		X		X	X	X	X		X	X	X	X	X	
CB3			X	X	X				X	X	X				X	X		X	X	X					X	X	X		X	X	X	
CB4	X	X							X	X	X	X	X	X			X	X							X	X	X	X	X	X	X	
CB5	X	X	X	X	X	X	X	X									X	X	X	X	X	X	X	X								
CB6	X	X	X	X	X	X	X	X																		X	X	X	X	X	X	

The seven check bits are parity bits derived from the matrix of data bits as indicated by "X" for each bit.

error detection and correction details

During a memory read cycle, the 7-bit check word is retrieved along with the actual data. In order to be able to determine whether the data from memory is acceptable to use as presented to the bus, the error flags must be tested to determine if they are at the high level.

The first case in Table 3 represents the normal, no-error conditions. The EDAC presents highs on both flags. The next two cases of single-bit errors give a high on $\overline{\text{MERR}}$ and a low on $\overline{\text{ERR}}$, which is the signal for a correctable error, and the EDAC should be sent through the correction cycle. The last three cases of double-bit errors will cause the EDAC to signal lows on both $\overline{\text{ERR}}$ and $\overline{\text{MERR}}$, which is the interrupt indication for the CPU.

TABLE 3. ERROR FUNCTION

TOTAL NUMBER OF ERRORS		ERROR FLAGS		DATA CORRECTION
32-BIT DATA WORD	7-BIT CHECK WORD	ERR	MERR	
0	0	H	H	Not applicable
1	0	L	H	Correction
0	1	L	H	Correction
1	1	L	L	Interrupt
2	0	L	L	Interrupt
0	2	L	L	Interrupt

Error detection is accomplished as the 7-bit check word and the 32-bit data word from memory are applied to internal parity generators/checkers. If the parity of all seven groupings of data and check bits are correct, it is assumed that no error has occurred and both error flags will be high.

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set low. Any single error in the 32-bit data word will change the state of either three or five bits of the 7-bit check word. Any single error in the 7-bit check word changes the state of only that one bit. In either case, the single error flag ($\overline{\text{ERR}}$) will be set low while the dual error flag ($\overline{\text{MERR}}$) will remain high.

Any two-bit error will change the state of an even number of check bits. The two-bit error is not correctable since the parity tree can only identify single-bit errors. Both error flags are set low when any two-bit error is detected.

Three or more simultaneous bit errors can cause the EDAC to believe that no error, a correctable error, or an uncorrectable error has occurred and will produce erroneous results in all three cases. It should be noted that the gross-error conditions of all lows and all highs will be detected.

2
LSI Devices

**SN54ALS632A, SN54ALS633 THRU SN54ALS635
 SN74ALS632A, SN74ALS633 THRU SN74ALS635
 32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS**

TABLE 4. READ, FLAG, AND CORRECT FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL		DATA I/O	DB CONTROL	DB OUTPUT LATCH	CHECK I/O	CB CONTROL	ERROR FLAGS	
		S1	S0		$\overline{\text{OEBn}}$ OR $\overline{\text{OEDB}}$	($\overline{\text{ALS632A}}$, $\overline{\text{ALS633}}$) $\overline{\text{LEDBO}}$		$\overline{\text{OECB}}$	$\overline{\text{ERR}}$	$\overline{\text{MERR}}$
Read	Read & flag	H	L	Input	H	X	Input	H	Enabled†	
Read	Latch input data & check bits	H	H	Latched input data	H	L	Latched input check word	H	Enabled†	
Read	Output corrected data & syndrome bits	H	H	Output corrected data word	L	X	Output syndrome bits‡	L	Enabled†	

†See Table 3 for error description.

‡See Table 5 for error location.

As the corrected word is made available on the data I/O port (DB0 thru DB31), the check word I/O port (CBO thru CB6) presents a 7-bit syndrome error code. This syndrome error code can be used to locate the bad memory chip. See Table 5 for syndrome decoding.

2

LSI Devices

SN54ALS632A, SN54ALS633 THRU SN54ALS635 SN74ALS632A, SN74ALS633 THRU SN74ALS635 32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

TABLE 5. SYNDROME DECODING

SYNDROME BITS							ERROR	SYNDROME BITS							ERROR	SYNDROME BITS							ERROR	SYNDROME BITS							ERROR	
6	5	4	3	2	1	0		6	5	4	3	2	1	0		6	5	4	3	2	1	0		6	5	4	3	2	1	0		
L	L	L	L	L	L	L	unc	L	H	L	L	L	L	L	2-bit	H	L	L	L	L	L	L	2-bit	H	H	L	L	L	L	L	unc	
L	L	L	L	L	L	L	2-bit	L	H	L	L	L	L	L	H	unc	H	L	L	L	L	L	H	unc	H	H	L	L	L	L	H	2-bit
L	L	L	L	L	H	L	2-bit	L	H	L	L	L	H	L	DB7	H	L	L	L	L	H	L	unc	H	H	L	L	L	H	L	2-bit	
L	L	L	L	L	H	H	unc	L	H	L	L	L	H	H	2-bit	H	L	L	L	L	H	H	2-bit	H	H	L	L	L	H	H	DB23	
L	L	L	L	H	L	L	2-bit	L	H	L	L	H	L	L	DB6	H	L	L	L	H	L	L	unc	H	H	L	L	H	L	L	2-bit	
L	L	L	L	H	L	H	unc	L	H	L	L	H	L	H	2-bit	H	L	L	L	H	L	H	2-bit	H	H	L	L	H	L	H	DB22	
L	L	L	L	H	H	L	unc	L	H	L	L	H	H	L	2-bit	H	L	L	L	H	H	L	2-bit	H	H	L	L	H	H	L	DB21	
L	L	L	L	H	H	H	2-bit	L	H	L	L	H	H	H	DB5	H	L	L	L	H	H	H	unc	H	H	L	L	H	H	H	2-bit	
L	L	L	H	L	L	L	2-bit	L	H	L	H	L	L	L	DB4	H	L	L	H	L	L	L	unc	H	H	L	H	L	L	L	2-bit	
L	L	L	H	L	L	L	unc	L	H	L	H	L	L	H	2-bit	H	L	L	H	L	L	H	2-bit	H	H	L	H	L	L	H	DB20	
L	L	L	H	L	H	L	DB31	L	H	L	H	L	H	L	2-bit	H	L	L	H	L	H	L	2-bit	H	H	L	H	L	H	L	DB19	
L	L	L	H	L	H	H	2-bit	L	H	L	H	L	H	H	DB3	H	L	L	H	L	H	H	DB15	H	H	L	H	L	H	H	2-bit	
L	L	L	H	H	L	L	unc	L	H	L	H	H	L	L	2-bit	H	L	L	H	H	L	L	2-bit	H	H	L	H	H	L	L	DB18	
L	L	L	H	H	L	H	2-bit	L	H	L	H	H	L	H	DB2	H	L	L	H	H	L	H	unc	H	H	L	H	H	L	L	2-bit	
L	L	L	H	H	H	L	2-bit	L	H	L	H	H	H	L	unc	H	L	L	H	H	H	L	DB14	H	H	L	H	H	H	L	2-bit	
L	L	L	H	H	H	H	DB30	L	H	L	H	H	H	H	2-bit	H	L	L	H	H	H	H	2-bit	H	H	L	H	H	H	H	CB4	
L	L	H	L	L	L	L	2-bit	L	H	H	L	L	L	L	DB0	H	L	H	L	L	L	L	unc	H	H	H	L	L	L	L	2-bit	
L	L	H	L	L	L	L	unc	L	H	H	L	L	L	H	2-bit	H	L	H	L	L	L	H	2-bit	H	H	H	L	L	L	H	DB16	
L	L	H	L	L	H	L	DB29	L	H	H	L	L	H	L	2-bit	H	L	H	L	L	H	L	2-bit	H	H	H	L	L	H	L	unc	
L	L	H	L	L	H	H	2-bit	L	H	H	L	L	H	H	unc	H	L	H	L	L	H	H	DB13	H	H	H	L	L	H	H	2-bit	
L	L	H	L	H	L	L	DB28	L	H	H	L	H	L	L	2-bit	H	L	H	L	H	L	L	2-bit	H	H	H	L	H	L	L	DB17	
L	L	H	L	H	L	H	2-bit	L	H	H	L	H	L	H	DB1	H	L	H	L	H	L	H	DB12	H	H	H	L	H	L	H	2-bit	
L	L	H	L	H	H	L	2-bit	L	H	H	L	H	H	L	unc	H	L	H	L	H	H	L	DB11	H	H	H	L	H	H	L	2-bit	
L	L	H	L	H	H	H	DB27	L	H	H	L	H	H	H	2-bit	H	L	H	L	H	H	H	2-bit	H	H	H	L	H	H	L	CB3	
L	L	H	H	L	L	L	DB26	L	H	H	H	L	L	L	2-bit	H	L	H	H	L	L	L	2-bit	H	H	H	H	L	L	L	unc	
L	L	H	H	L	L	L	2-bit	L	H	H	H	L	L	H	unc	H	L	H	H	L	L	H	DB10	H	H	H	H	L	L	L	2-bit	
L	L	H	H	L	L	L	2-bit	L	H	H	H	L	L	H	unc	H	L	H	H	L	L	H	DB9	H	H	H	H	L	L	L	2-bit	
L	L	H	H	L	L	H	DB25	L	H	H	H	L	H	H	2-bit	H	L	H	H	L	H	H	2-bit	H	H	H	H	L	H	H	CB2	
L	L	H	H	H	L	L	2-bit	L	H	H	H	H	L	L	unc	H	L	H	H	H	L	L	DB8	H	H	H	H	L	L	L	2-bit	
L	L	H	H	H	L	H	DB24	L	H	H	H	H	L	L	2-bit	H	L	H	H	H	L	L	2-bit	H	H	H	H	L	L	H	CB1	
L	L	H	H	H	H	L	unc	L	H	H	H	H	L	L	2-bit	H	L	H	H	H	H	L	2-bit	H	H	H	H	H	L	L	CB0	
L	L	H	H	H	H	H	2-bit	L	H	H	H	H	H	H	CB6	H	L	H	H	H	H	H	CB5	H	H	H	H	H	H	H	none	

CB X= error in check bit X
DB Y= error in data bit Y
2-bit = double-bit error
unc = uncorrectable multibit error

read-modify-write (byte control) operations

The 'ALS632A and 'ALS633 devices are capable of byte-write operations. The 39-bit word from memory must first be latched into the DB and CB input latches. This is easily accomplished by switching from the read and flag mode (S1 = H, S0 = L) to the latch input mode (S1 = H, S0 = H). The EDAC will then make any corrections, if necessary, to the data word and place it at the input of the output data latch. This data word must then be latched into the output data latch by taking $\overline{\text{LEDBO}}$ from a low to a high.

Byte control can now be employed on the data word through the $\overline{\text{OEB0}}$ through $\overline{\text{OEB3}}$ controls. $\overline{\text{OEB0}}$ controls DB0-DB7 (byte 0), $\overline{\text{OEB1}}$ controls DB8-DB15 (byte 1), $\overline{\text{OEB2}}$ controls DB16-DB23 (byte 2), and $\overline{\text{OEB3}}$ controls DB24-DB31 (byte 3). Placing a high on the byte control will disable the output and the user can modify the byte. If a low is placed on the byte control, then the original byte is allowed to pass onto the data bus unchanged. If the original data word is altered through byte control, a new check word must be generated before it is written back into memory. This is easily accomplished by taking control S1 and S0 low. Table 6 lists the read-modify-write functions.

2
LSI Devices

**SN54ALS632A, SN54ALS633 THRU SN54ALS635
SN74ALS632A, SN74ALS633 THRU SN74ALS635
32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS**

TABLE 6. READ-MODIFY-WRITE FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL		BYTE ⁿ	$\overline{OE}Bn$	DB OUTPUT LATCH LEDB \overline{O}	CHECK I/O	CB CONTROL	ERROR FLAG	
		S1	S0						ERR	MERR
Read	Read & Flag	H	L	Input	H	X	Input	H	Enabled	
Read	Latch input data & check bits	H	H	Latched Input data	H	L	Latched input check word	H	Enabled	
Read	Latch corrected data word into output latch	H	H	Latched output data word	H	H	Hi-Z Output Syndrome bits	H L	Enabled	
Modify /write	Modify appropriate byte or bytes & generate new check word	L	L	Input modified BYTE \overline{O}	H	H	Output check word	L	H H	
				Output unchanged BYTE \overline{O}	L					

[†] $\overline{OE}B0$ controls DB0-DB7 (BYTE0), $\overline{OE}B1$ controls DB8-DB15 (BYTE1), $\overline{OE}B3$ controls DB16-DB23 (BYTE2), $\overline{OE}B3$ controls DB24-DB31 (BYTE3).

diagnostic operations

The 'ALS632A and 'ALS633 thru 'ALS635 are capable of diagnostics that allow the user to determine whether the EDAC or the memory is failing. The diagnostic function tables will help the user to see the possibilities for diagnostic control.

In the diagnostic mode (S1 = L, S0 = H), the checkword is latched into the input latch while the data input latch remains transparent. This lets the user apply various data words against a fixed known checkword. If the user applies a diagnostic data word with an error in any bit location, the ERR flag should be low. If a diagnostic data word with two errors in any bit location is applied, the MERR flag should be low. After the checkword is latched into the input latch, it can be verified by taking $\overline{OE}CB$ low. This outputs the latched checkword. With the 'ALS632A and 'ALS633, the diagnostic data word can be latched into the output data latch and verified. It should be noted that the 'ALS634 and 'ALS635 do not have this pass-through capability because they do not contain an output data latch. By changing from the diagnostic mode (S1 = L, S0 = H) to the correction mode (S1 = H, S0 = H), the user can verify that the EDAC will correct the diagnostic data word. Also, the syndrome bits can be produced to verify that the EDAC pinpoints the error location. Table 7 ('ALS632A and 'ALS633) and Table 8 ('ALS634 and 'ALS635) list the diagnostic functions.

**SN54ALS632A, SN54ALS633 THRU SN54ALS635
SN74ALS632A, SN74ALS633 THRU SN74ALS635
32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS**

TABLE 7. 'ALS632A, 'ALS633 DIAGNOSTIC FUNCTION

EDAC FUNCTION	CONTROL		DATA I/O	DB BYTE CONTROL OEB _n	DB OUTPUT LATCH LEDB ₀	CHECK I/O	CB CONTROL OECB	ERROR FLAGS	
	S1	S0						ERR	MERR
Read & flag	H	L	Input correct data word	H	X	Input correct check bits	H	H	H
Latch input check word while data input latch remains transparent	L	H	Input diagnostic data word [†]	H	L	Latched input check bits	H		Enabled
Latch diagnostic data word into output latch	L	H	Input diagnostic data word [†]	H	H	Output latched check bits ----- Hi-Z	L ----- H		Enabled
Latch diagnostic data word into input latch	H	H	Latched input diagnostic data word	H	H	Output syndrome bits ----- Hi-Z	L ----- H		Enabled
Output diagnostic data word & syndrome bits	H	H	Output diagnostic data word	L	H	Output syndrome bits ----- Hi-Z	L ----- H		Enabled
Output corrected diagnostic data word & output syndrome bits	H	H	Output corrected diagnostic data word	L	L	Output syndrome bits ----- Hi-Z	L ----- H		Enabled

[†]Diagnostic data is a data word with an error in one bit location except when testing the $\overline{\text{MERR}}$ error flag. In this case, the diagnostic data word will contain errors in two bit locations.

TABLE 8. 'ALS634, 'ALS635 DIAGNOSTIC FUNCTION

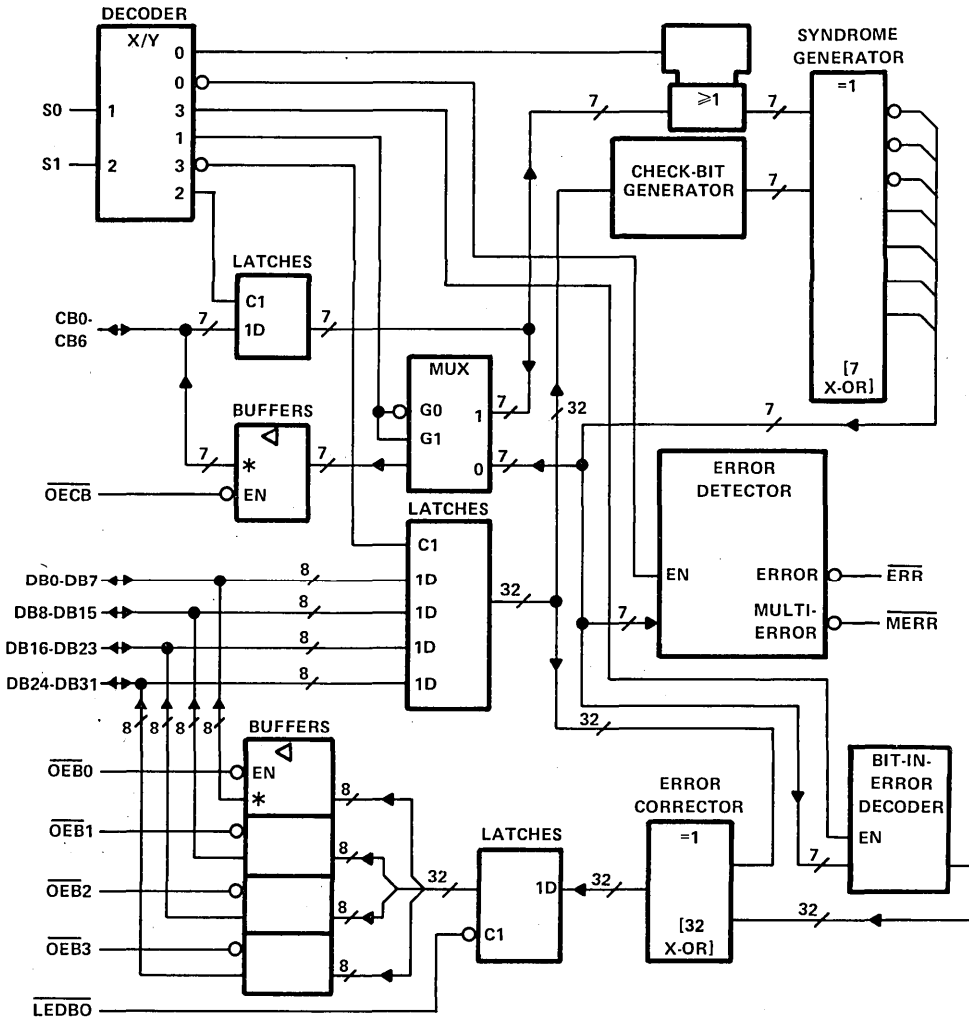
EDAC FUNCTION	CONTROL		DATA I/O	DB CONTROL OEDB	CHECK I/O	DB CONTROL OECB	ERROR FLAGS	
	S1	S0					ERR	MERR
Read & flag	H	L	Input correct data word	H	Input correct check bits	H	H	H
Latch input check bits while data input latch remains transparent	L	H	Input diagnostic data word [†]	H	Latched input check bits	H		Enabled
Output input check bits	L	H	Input diagnostic data word [†]	H	Output input check bits	L		Enabled
Latch diagnostic data into input latch	H	H	Latched input diagnostic data word	H	Output syndrome bits ----- Hi-Z	L ----- H		Enabled
Output corrected diagnostic data word	H	H	Output corrected diagnostic data word	L	Output syndrome bits ----- Hi-Z	L ----- H		Enabled

[†]Diagnostic data is a data word with an error in one bit location except when testing the $\overline{\text{MERR}}$ error flag. In this case, the diagnostic data word will contain errors in two bit locations.

2
LSI Devices

SN54ALS632A, SN54ALS633, SN74ALS632A, SN74ALS633
32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

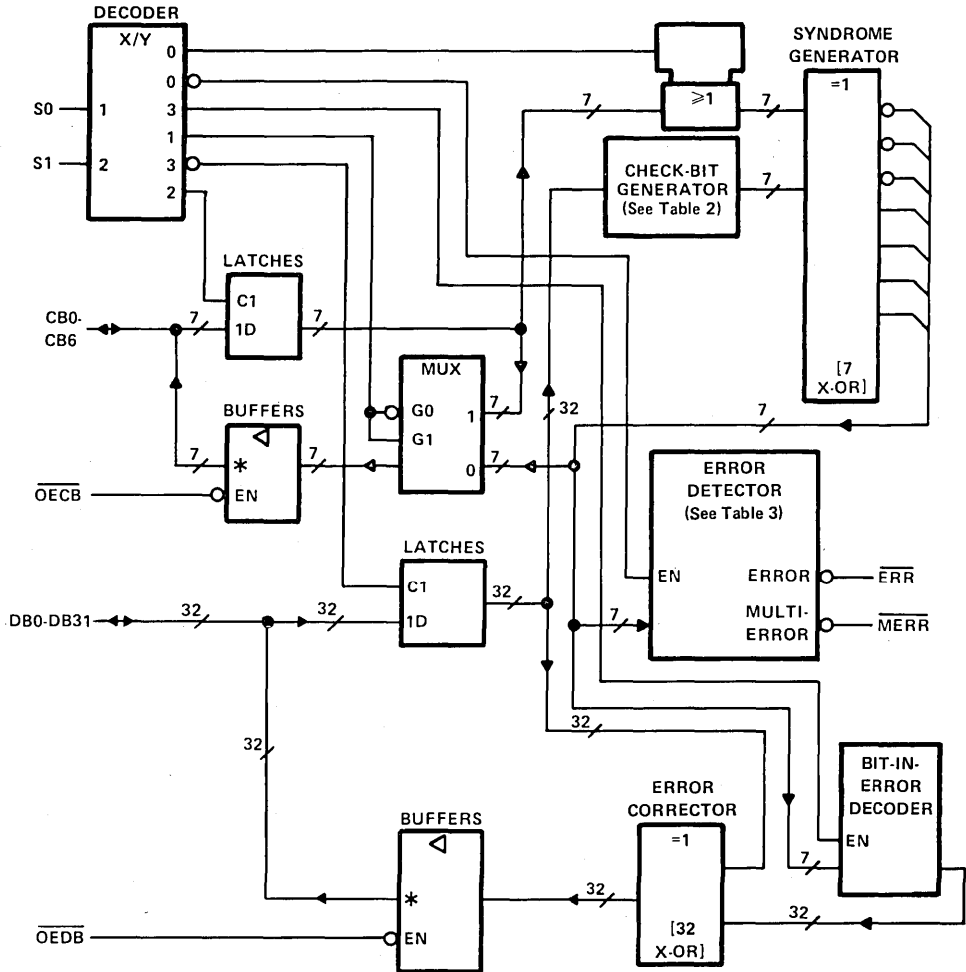
'ALS632A, 'ALS633 logic diagram (positive logic)



*'ALS632A has 3-state (∇) check-bit and data outputs.
 'ALS633 has open-collector (⊕) check-bit and data outputs.

SN54ALS634, SN54ALS635, SN74ALS634, SN74ALS635 32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

'ALS634, 'ALS635 logic diagram (positive logic)



*'ALS634 has 3-state (▽) check-bit and data outputs.
'ALS635 has open-collector (⊕) check-bit and data outputs.

**SN54ALS632A, SN54ALS633 THRU SN54ALS635
SN74ALS632A, SN74ALS633 THRU SN74ALS635
32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage: CB and DB	5.5 V
All others	7 V
Operating free-air temperature range:	
SN74ALS632A, SN74ALS633 thru SN74ALS635	0°C to 70°C
Operating case temperature range:	
SN54ALS632A, SN54ALS633 thru SN54ALS635	-55°C to 125°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54ALS632A SN54ALS633 THRU SN54ALS635			SN74ALS632A SN74ALS633 THRU SN74ALS635			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current	ERR or MERR		-0.4	-0.4		mA	
		DB or CB	'ALS632A, 'ALS634	-1	-2.6			
I _{OL}	Low-level output current	ERR or MERR		4	8		mA	
		DB or CB		12	24			
t _w	Pulse duration	LEDBO low			25	25		ns
t _{su}	Setup time	(1) Data and check word before S0↑ (S1 = H)		15	10		ns	
		(2) S0 high before LEDB0↑ (S1 = H) [†]		45	45			
		(3) LEDB0 high before the earlier of S0↓ or S1↓ [†]		0	0			
		(4) LEDB0 high before S1↑ (S0 = H)		0	0			
		(5) Diagnostic data word before S1↑ (S0 = H)		15	10			
		(6) Diagnostic check word before the later of S1↓ or S0↑		15	10			
		(7) Diagnostic data word before LEDB0↑ (S1 = L and S0 = H) [‡]		25	20			
t _h	Hold time	(8) Read-mode, S0 low and S1 high		35	30		ns	
		(9) Data and check word after S0↑ (S1 = H)		20	15			
		(10) Data word after S1↑ (S0 = H)		20	15			
		(11) Check word after the later of S1↓ or S0↑		20	15			
		(12) Diagnostic data word after LEDB0↑ (S1 = L, S0 = H) [‡]		0	0			
t _{corr}	Correction time (see Figure 1)	65			58		ns	
T _C	Operating case temperature	-55			125		°C	
T _A	Operating free-air temperature				0		70	°C

[†]These times ensure that corrected data is saved in the output data latch.

[‡]These times ensure that the diagnostic data word is saved in the output data latch.

2 LSI Devices

SN54ALS632A, SN54ALS634, SN74ALS632A, SN74ALS634

32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS WITH 3-STATE OUTPUTS

'ALS632A, 'ALS634 electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS632A SN54ALS634		SN74ALS632A SN74ALS634		UNIT
		MIN	TYP [†] MAX	MIN	TYP [†] MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA	-1.5		-1.5		V
V _{OH}	All outputs V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA	V _{CC} -2		V _{CC} -2		V
	DB or CB V _{CC} = 4.5 V, I _{OH} = -1 mA	2.4	3.3			
V _{OL}	ERR or MERR V _{CC} = 4.5 V, I _{OL} = 4 mA	0.25	0.4	0.25	0.4	V
	V _{CC} = 4.5 V, I _{OL} = 8 mA			0.35	0.5	
	DB or CB V _{CC} = 4.5 V, I _{OL} = 12 mA	0.25	0.4	0.25	0.4	
	V _{CC} = 4.5 V, I _{OL} = 24 mA			0.35	0.5	
I _I	S0 or S1 V _{CC} = 5.5 V, V _I = 7 V		0.1		0.1	mA
	All others V _{CC} = 5.5 V, V _I = 5.5 V		0.1		0.1	
I _{IH}	S0 or S1 V _{CC} = 5.5 V, V _I = 2.7 V		20		20	μA
	All others [‡]		20		20	
I _{IL}	S0 or S1 V _{CC} = 5.5 V, V _I = 0.4 V		-0.4		-0.4	mA
	All others [‡]		-0.1		-0.1	
I _O [§]	V _{CC} = 5.5 V, V _O = 2.25 V	-30	-112	-30	-112	mA
I _{CC}	V _{CC} = 5.5 V, See Note 1	150	250	150	250	mA

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_OS.

NOTE 1: I_{CC} is measured with S0 and S1 at 4.5 V and all CB and DB pins grounded.

'ALS632A switching characteristics, V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_C = -55°C to 125°C for SN54ALS632A, T_A = 0°C to 70°C for SN74ALS632A

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ALS632A		SN74ALS632A		UNIT
				MIN	MAX	MIN	MAX	
t _{pd}	DB and CB	ERR	S1 = H, S0 = L, R _L = 500 Ω	10	43	10	40	ns
	DB	ERR	S1 = L, S0 = H, R _L = 500 Ω	10	43	10	40	
t _{pd}	DB and CB	MERR	S1 = H, S0 = L, R _L = 500 Ω	15	67	15	55	ns
	DB	MERR	S1 = L, S0 = H, R _L = 500 Ω	15	67	15	55	
t _{pd}	S0↓ and S1↓	CB	R1 = R2 = 500 Ω	10	60	10	48	ns
t _{PLH}	S0↓ and S1↓	ERR	R _L = 500 Ω	5	30	5	25	ns
t _{pd}	DB	CB	S1 = L, S0 = L, R1 = R2 = 500 Ω	10	60	10	48	ns
t _{pd}	LEDB0↓	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω	7	35	7	30	ns
t _{pd}	S1↑	CB	S0 = H, R1 = R2 = 500 Ω	10	60	10	50	ns
t _{en}	OECEB↓	CB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	30	2	25	ns
t _{dis}	OECEB↑	CB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	30	2	25	ns
t _{en}	OEBO thru OEB3↓	DB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	30	2	25	ns
t _{dis}	OEBO thru OEB3↑	DB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	30	2	25	ns

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**TEXAS
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SN54ALS634, SN74ALS634
32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS
WITH 3-STATE OUTPUTS

*ALS634 switching characteristics, $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $T_C = -55^\circ\text{C to } 125^\circ\text{C}$
 for SN54ALS634, $T_A = 0^\circ\text{C to } 70^\circ\text{C}$ for SN74ALS634

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ALS634		SN74ALS634		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}	DB and CB	$\overline{\text{ERR}}$	$S1 = H, S0 = L, R_L = 500 \Omega$	10	43	10	40	ns
			$S1 = L, S0 = H, R_L = 500 \Omega$	10	43	10	40	
t_{pd}	DB and CB	$\overline{\text{MERR}}$	$S1 = H, S0 = L, R_L = 500 \Omega$	15	67	15	55	ns
			$S1 = L, S0 = H, R_L = 500 \Omega$	15	67	15	55	
t_{pd}	$S0\uparrow$ and $S1\downarrow$	CB	$R1 = R2 = 500 \Omega$	10	60	10	48	ns
t_{PLH}	$S0\uparrow$ and $S1\downarrow$	$\overline{\text{ERR}}$	$R_L = 500 \Omega$	5	30	5	25	ns
t_{pd}	DB	CB	$S1 = L, S0 = L, R1 = R2 = 500 \Omega$	10	60	10	48	ns
t_{pd}	$S1\uparrow$	CB	$S0 = H, R1 = R2 = 500 \Omega$	7	35	7	30	ns
t_{en}	$\overline{\text{OECB}}\downarrow$	CB	$S1 = X, S0 = H, R1 = R2 = 500 \Omega$	2	30	2	25	ns
t_{dis}	$\overline{\text{OECB}}\uparrow$	CB	$S1 = X, S0 = H, R1 = R2 = 500 \Omega$	2	30	2	25	ns
t_{en}	$\overline{\text{OEDB}}\downarrow$	DB	$S1 = X, S0 = H, R1 = R2 = 500 \Omega$	2	30	2	30	ns
t_{dis}	$\overline{\text{OEDB}}\uparrow$	DB	$S1 = X, S0 = H, R1 = R2 = 500 \Omega$	2	30	2	25	ns

2

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2-92



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'ALS633 electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS633			SN74ALS633			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.5			-1.5	V
V _{OH} ERR or MERR	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA	V _{CC} -2			V _{CC} -2			V
I _{OH} DB or CB	V _{CC} = 4.5 V, V _{OH} = 5.5 V			0.1			0.1	mA
V _{OL}	ERR or MERR	V _{CC} = 4.5 V, I _{OL} = 4 mA	0.25	0.4		0.25	0.4	V
		V _{CC} = 4.5 V, I _{OL} = 8 mA				0.35	0.5	
	DB or CB	V _{CC} = 4.5 V, I _{OL} = 12 mA	0.25	0.4		0.25	0.4	
		V _{CC} = 4.5 V, I _{OL} = 24 mA				0.35	0.5	
I _I	S0 or S1	V _{CC} = 5.5 V, V _I = 7 V		0.1			0.1	mA
	All others	V _{CC} = 5.5 V, V _I = 5.5 V		0.1			0.1	
I _{IH}	S0 or S1	V _{CC} = 5.5 V, V _I = 2.7 V		20			20	μA
	All others†			20			20	
I _{IL}	S0 or S1	V _{CC} = 5.5 V, V _I = 0.4 V		-0.4			-0.4	mA
	All others†			-0.1			-0.1	
I _O ‡	ERR or MERR	V _{CC} = 5.5 V, V _O = 2.25 V	-30	-112	-30	-112	mA	
I _{CC}	V _{CC} = 5.5 V, See Note 1		150	250		150	250	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_OS.

NOTE 1: I_{CC} is measured with S0 and S1 at 4.5 V and all CB and DB pins grounded.

'ALS633 switching characteristics, V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_C = -55 °C to 125 °C for SN54ALS633, T_A = 0 °C to 70 °C for SN74ALS633

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ALS633		SN74ALS633		UNIT
				MIN	MAX	MIN	MAX	
t _{pd}	DB and CB	ERR	S1 = H, S0 = L, R _L = 500 Ω	10	43	10	40	ns
	DB	ERR	S1 = L, S0 = H, R _L = 500 Ω	10	43	10	40	
t _{pd}	DB and CB	MERR	S1 = H, S0 = L, R _L = 500 Ω	15	67	15	55	ns
			S1 = L, S0 = H, R _L = 500 Ω	15	67	15	55	
t _{pd}	S0↓ and S1↓	CB	R _L = 680 Ω	10	75	10	60	ns
t _{PLH}	S0↓ and S1↓	ERR	R _L = 500 Ω	5	30	5	25	ns
t _{pd}	DB	CB	S1 = L, S0 = L, R _L = 680 Ω	10	70	10	60	ns
t _{pd}	LEDB0↓	DB	S1 = X, S0 = H, R _L = 680 Ω	15	70	15	50	ns
t _{pd}	S1↑	CB	S0 = H, R _L = 680 Ω	10	60	10	45	ns
t _{PLH}	OE _{CB} ↑	CB	S1 = X, S0 = H, R _L = 680 Ω	2	35	2	30	ns
t _{PHL}	OE _{CB} ↓	CB	S1 = X, S0 = H, R _L = 680 Ω	2	35	2	30	ns
t _{PLH}	OE _{B0} thru OE _{B3} ↑	DB	S1 = X, S0 = H, R _L = 680 Ω	2	35	2	30	ns
t _{PHL}	OE _{B0} thru OE _{B3} ↓	DB	S1 = X, S0 = H, R _L = 680 Ω	2	35	2	30	ns

SN54ALS635, SN74ALS635
32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS
WITH OPEN-COLLECTOR OUTPUTS

**PRODUCT
 PREVIEW**

*ALS635 electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS635			SN74ALS635		UNIT
		MIN	TYP†	MAX	MIN	TYP†	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.5			V
V _{OH}	ERR or MERR V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA	V _{CC} -2			V _{CC} -2		V
I _{OH}	DB or CB V _{CC} = 4.5 V, V _{OH} = 5.5 V		0.1			0.1	mA
V _{OL}	ERR or MERR	V _{CC} = 4.5 V, I _{OL} = 4 mA	0.25	0.4	0.25	0.4	V
		V _{CC} = 4.5 V, I _{OL} = 8 mA			0.35	0.5	
	DB or CB	V _{CC} = 4.5 V, I _{OL} = 12 mA	0.25	0.4	0.25	0.4	
		V _{CC} = 4.5 V, I _{OL} = 24 mA			0.35	0.5	
I _I	S0 or S1 V _{CC} = 5.5 V, V _I = 7 V						mA
	All others V _{CC} = 5.5 V, V _I = 5.5 V						
I _{IH}	S0 or S1 V _{CC} = 5.5 V, V _I = 2.7 V						μA
	All others‡						
I _{IL}	S0 or S1 V _{CC} = 5.5 V, V _I = 0.4 V						mA
	All others‡						
I _O §	ERR or MERR V _{CC} = 5.5 V, V _O = 2.25 V	-30	-112	-30	-112		mA
I _{CC}	V _{CC} = 5.5 V, See Note 1		150			150	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_OS.

NOTE 1: I_{CC} is measured with S0 and S1 at 4.5 V and all CB and DB pins grounded.

*ALS635 switching characteristics, V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_C = -55°C to 125°C for SN54ALS635, T_A = 0°C to 70°C for SN74ALS635

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ALS635		SN74ALS635		UNIT
				MIN	TYP†	MAX	MIN	
t _{pd}	DB and CB	ERR	S1 = H, S0 = L, R _L = 500 Ω		26		26	ns
		DB	ERR	S1 = L, S0 = H, R _L = 500 Ω		26		
t _{pd}	DB and CB	MERR	S1 = H, S0 = L, R _L = 500 Ω		40		40	ns
			S1 = L, S0 = H, R _L = 500 Ω		40		40	
t _{pd}	S0↓ and S1↓	CB	R _L = 680 Ω		40		40	ns
t _{PLH}	S0↓ and S1↓	ERR	R _L = 500 Ω		14		14	ns
t _{pd}	DB	CB	S1 = L, S0 = L, R _L = 680 Ω		40		40	ns
t _{pd}	S1↑	DB	S0 = H, R _L = 680 Ω		40		40	ns
t _{PLH}	OE _{CB} ↑	CB	S1 = X, S0 = H, R _L = 680 Ω		24		24	ns
t _{PHL}	OE _{CB} ↓	CB	S1 = X, S0 = H, R _L = 680 Ω		24		24	ns
t _{PLH}	OE _{DB} ↑	DB	S1 = X, S0 = H, R _L = 680 Ω		24		24	ns
t _{PHL}	OE _{DB} ↓	DB	S1 = X, S0 = H, R _L = 680 Ω		24		24	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

2 LSI Devices

**SN54ALS632A, SN54ALS633 THRU SN54ALS635
SN74ALS632A, SN74ALS633 THRU SN74ALS635**
32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

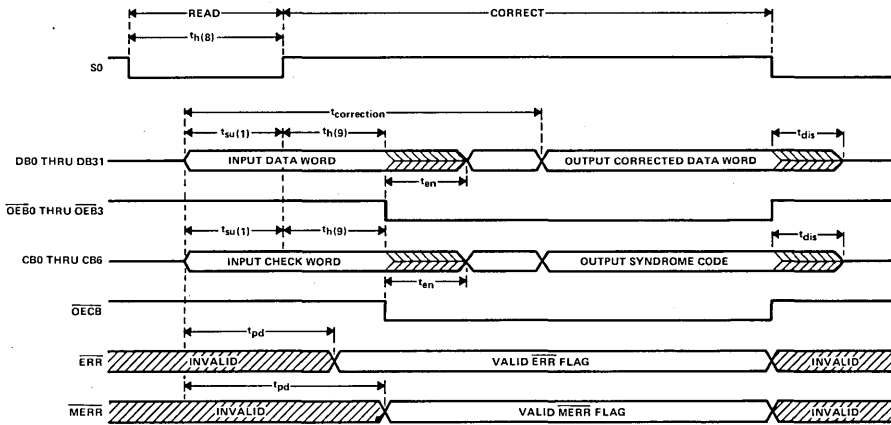


FIGURE 1. READ, FLAG, AND CORRECT MODE SWITCHING WAVEFORMS

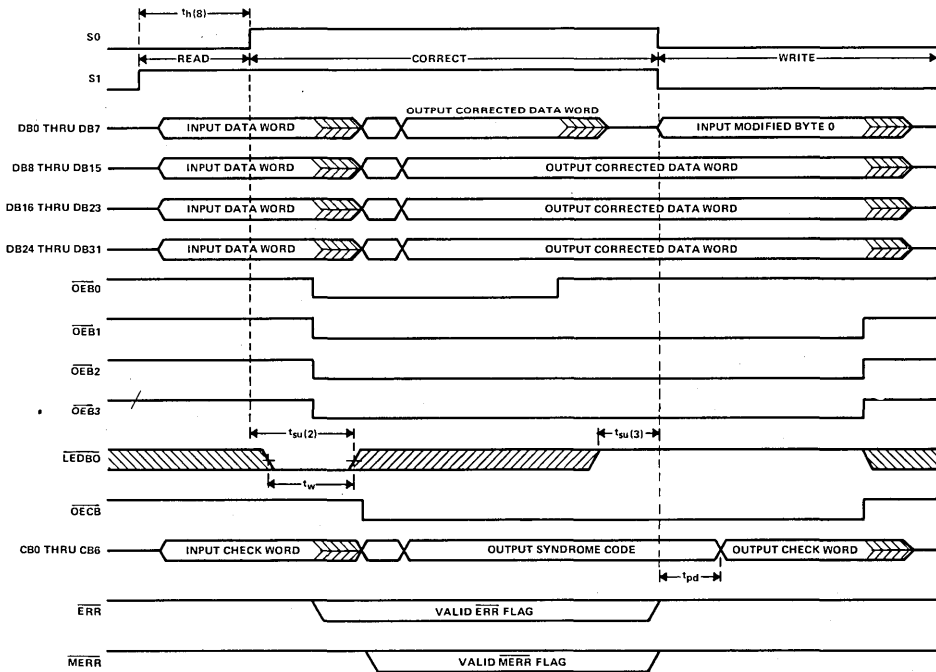


FIGURE 2. READ, CORRECT, MODIFY MODE SWITCHING WAVEFORMS

2

LSI Devices

**SN54ALS632A, SN54ALS633 THRU SN54ALS635
 SN74ALS632A, SN74ALS633 THRU SN74ALS635
 32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS**

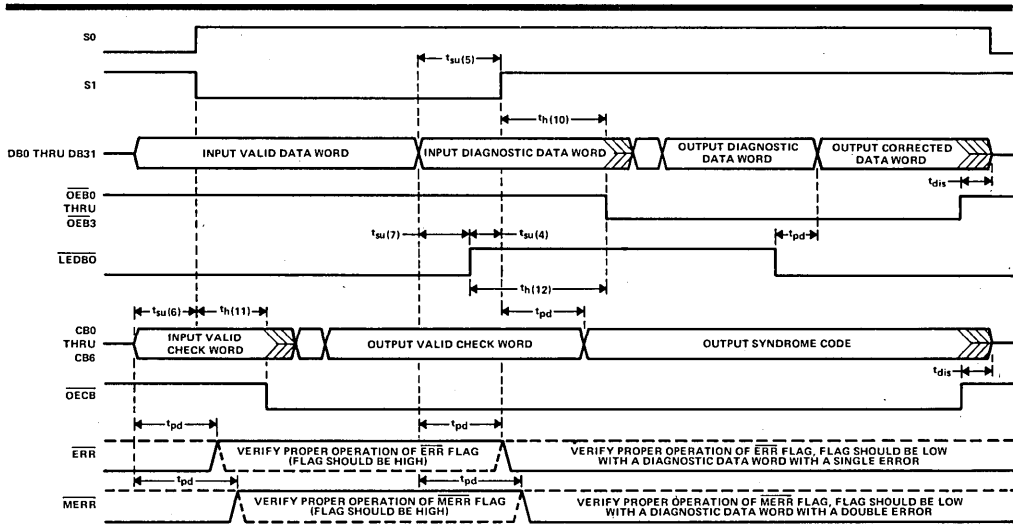


FIGURE 3. DIAGNOSTIC MODE SWITCHING WAVEFORM

2

LSI Devices

**SN54AS632, SN54AS634
SN74AS632, SN74AS634
32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS**

D2661, JANUARY 1986

- Detects and Corrects Single-Bit Errors
- Detects and Flags Dual-Bit Errors
- Built-In Diagnostic Capability
- Fast Write and Read Cycle Processing Times
- Byte-Write Capability . . . 'AS632
- Dependable Texas Instruments Quality and Reliability

DEVICE	PACKAGE	BYTE-WRITE	OUTPUT
'AS632	52-pin	yes	3-State
'AS634	48-pin	no	3-State

description

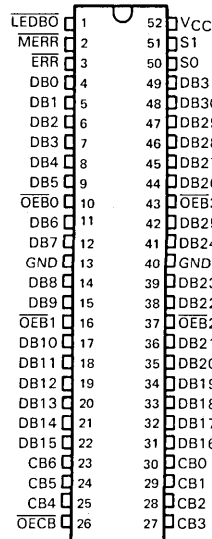
The 'AS632 and 'AS634 devices are 32-bit parallel error detection and correction circuits (EDACs) in 52-pin ('AS632) or 48-pin ('AS634) 600-mil packages. The EDACs use a modified Hamming code to generate a 7-bit check word from a 32-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 39-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

Single-bit errors in the 32-bit data word are flagged and corrected.

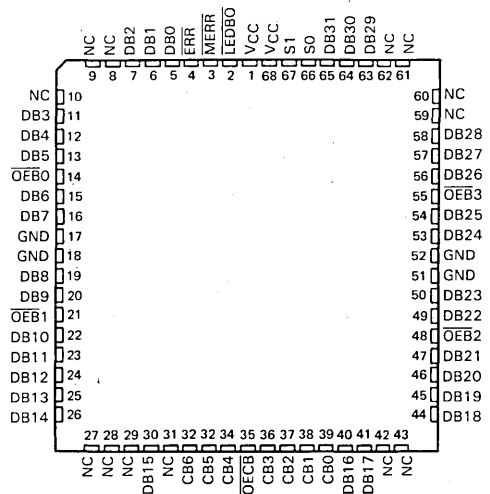
Single-bit errors in the 7-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 32-bit data word is not in error. The correction cycle will simply pass along the original 32-bit data word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These errors may occur in any two bits of the 39-bit data word from memory (two errors in the 32-bit data word, two errors in the 7-bit check word, or one error in each word). The gross-error condition of all lows or all highs from memory will be detected. Otherwise, errors in three or more bits of the 39-bit word are beyond the capabilities of these devices to detect.

**'AS632 . . . JD PACKAGE
(TOP VIEW)**



**'AS632 . . . FN PACKAGE
(TOP VIEW)**



NC—No internal connection

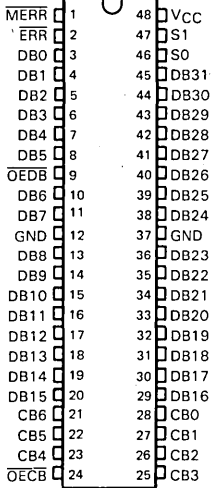
**2
LSI Devices**

**SN54AS632, SN54AS634
SN74AS632, SN74AS634
32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS**

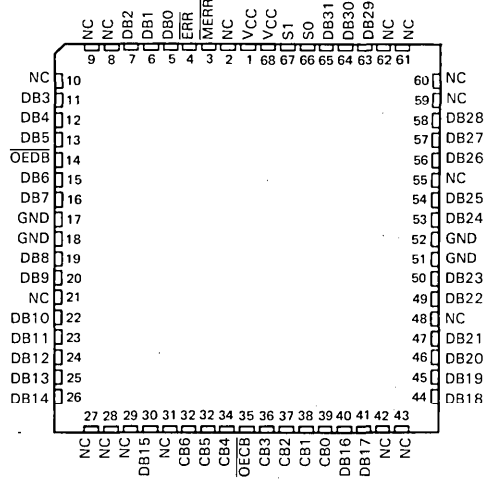
Read-modify-write (byte-control) operations can be performed with the 'AS632 EDAC by using output latch enable, LEDB0, and the individual OEB0 thru OEB3 byte control pins.

Diagnostics are performed on the EDACs by controls and internal paths that allow the user to read the contents of the DB and CB input latches. These will determine if the failure occurred in memory or in the EDAC.

'AS634 . . . JD PACKAGE
(TOP VIEW)



'AS634 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

TABLE 1. WRITE CONTROL FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL		DATA I/O	DB CONTROL OEBn OR OEDB	DB OUTPUT LATCH ('AS632) LEDB0	CHECK I/O	CB CONTROL OECB	ERROR FLAGS	
		S1	S0						ERR	MERR
Write	Generate check word	L	L	Input	H	X	Output check bits†	L	H	H

† See Table 2 for details on check bit generation.

memory write cycle details

During a memory write cycle, the check bits (CB0 thru CB6) are generated internally in the EDAC by seven 16-input parity generators using the 32-bit data word as defined in Table 2. These seven check bits are stored in memory along with the original 32-bit data word. This 32-bit word will later be used in the memory read cycle for error detection and correction.

32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

TABLE 2. PARITY ALGORITHM

CHECK WORD BIT	32-BIT DATA WORD																															
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CB0	X	X	X	X						X	X	X	X			X			X		X	X	X	X	X	X	X					X
CB1				X	X	X	X	X	X	X	X	X	X	X	X					X	X	X	X	X	X	X	X	X	X	X	X	X
CB2	X	X			X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
CB3		X	X	X				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
CB4	X	X						X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
CB5	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
CB6	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	

The seven check bits are parity bits derived from the matrix of data bits as indicated by "X" for each bit.

error detection and correction details

During a memory read cycle, the 7-bit check word is retrieved along with the actual data. In order to be able to determine whether the data from memory is acceptable to use as presented to the bus, the error flags must be tested to determine if they are at the high level.

The first case in Table 3 represents the normal, no-error conditions. The EDAC presents highs on both flags. The next two cases of single-bit errors give a high on $\overline{\text{MERR}}$ and a low on $\overline{\text{ERR}}$, which is the signal for a correctable error, and the EDAC should be sent through the correction cycle. The last three cases of double-bit errors will cause the EDAC to signal lows on both $\overline{\text{ERR}}$ and $\overline{\text{MERR}}$, which is the interrupt indication for the CPU.

TABLE 3. ERROR FUNCTION

TOTAL NUMBER OF ERRORS		ERROR FLAGS		DATA CORRECTION
32-BIT DATA WORD	7-BIT CHECK WORD	$\overline{\text{ERR}}$	$\overline{\text{MERR}}$	
0	0	H	H	Not applicable
1	0	L	H	Correction
0	1	L	H	Correction
1	1	L	L	Interrupt
2	0	L	L	Interrupt
0	2	L	L	Interrupt

Error detection is accomplished as the 7-bit check word and the 32-bit data word from memory are applied to internal parity generators/checkers. If the parity of all seven groupings of data and check bits are correct, it is assumed that no error has occurred and both error flags will be high.

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set low. Any single error in the 32-bit data word will change the state of either three or five bits of the 7-bit check word. Any single error in the 7-bit check word changes the state of only that one bit. In either case, the single error flag ($\overline{\text{ERR}}$) will be set low while the dual error flag ($\overline{\text{MERR}}$) will remain high.

Any two-bit error will change the state of an even number of check bits. The two-bit error is not correctable since the parity tree can only identify single-bit errors. Both error flags are set low when any two-bit error is detected.

Three or more simultaneous bit errors can cause the EDAC to believe that no error, a correctable error, or an uncorrectable error has occurred and will produce erroneous results in all three cases. It should be noted that the gross-error conditions of all lows and all highs will be detected.

SN54AS632, SN54AS634
SN74AS632, SN74AS634
32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

TABLE 4. READ, FLAG, AND CORRECT FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL		DATA I/O	DB CONTROL	DB OUTPUT LATCH	CHECK I/O	CB CONTROL	ERROR FLAGS
		S1	S0		$\overline{\text{OEB}}_n$ OR $\overline{\text{OEDB}}$	('AS632) $\overline{\text{LEDB0}}$		$\overline{\text{OECB}}$	$\overline{\text{ERR}}$ $\overline{\text{MERR}}$
Read	Read & flag	H	L	Input	H	X	Input	H	Enabled†
Read	Latch input data & check bits	H	H	Latched input data	H	L	Latched input check word	H	Enabled†
Read	Output corrected data & syndrome bits	H	H	Output corrected data word	L	X	Output syndrome bits‡	L	Enabled†

†See Table 3 for error description.

‡See Table 5 for error location.

As the corrected word is made available on the data I/O port (DB0 thru DB31), the check word I/O port (CB0 thru CB6) presents a 7-bit syndrome error code. This syndrome error code can be used to locate the bad memory chip. See Table 5 for syndrome decoding.

2

LSI Devices

32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

TABLE 5. SYNDROME DECODING

SYNDROME BITS							ERROR	SYNDROME BITS							ERROR	SYNDROME BITS							ERROR	SYNDROME BITS							ERROR								
6	5	4	3	2	1	0		6	5	4	3	2	1	0		6	5	4	3	2	1	0		6	5	4	3	2	1	0		6	5	4	3	2	1	0	
L	L	L	L	L	L	L	unc	L	H	L	L	L	L	L	2-bit	H	L	L	L	L	L	L	L	L	L	L	L	L	L	unc									
L	L	L	L	L	L	H	2-bit	L	H	L	L	L	L	H	unc	H	L	L	L	L	L	H	H	L	L	L	L	L	H	2-bit									
L	L	L	L	L	H	L	2-bit	L	H	L	L	L	H	L	DB7	H	L	L	L	L	H	L	H	L	L	L	L	H	L	2-bit									
L	L	L	L	L	H	H	unc	L	H	L	L	L	H	H	2-bit	H	L	L	L	L	H	H	H	L	L	L	L	H	H	DB23									
L	L	L	L	H	L	L	2-bit	L	H	L	L	H	L	L	DB6	H	L	L	L	H	L	L	L	L	L	L	L	L	L	2-bit									
L	L	L	L	H	L	H	unc	L	H	L	L	H	L	H	2-bit	H	L	L	L	H	L	H	L	L	L	L	L	L	H	DB22									
L	L	L	L	H	H	L	unc	L	H	L	L	H	H	L	2-bit	H	L	L	L	H	H	L	L	L	L	L	L	L	H	DB21									
L	L	L	L	H	H	H	2-bit	L	H	L	L	H	H	H	DB5	H	L	L	L	H	H	H	L	L	L	L	L	L	H	2-bit									
L	L	L	H	L	L	L	2-bit	L	H	L	H	L	L	L	DB4	H	L	L	H	L	L	L	L	L	L	L	L	L	L	2-bit									
L	L	L	H	L	L	H	unc	L	H	L	H	L	L	H	2-bit	H	L	L	H	L	L	L	H	L	L	L	L	L	H	DB20									
L	L	L	H	L	H	L	DB31	L	H	L	H	L	H	L	2-bit	H	L	L	H	L	H	L	L	L	L	L	L	L	H	DB19									
L	L	L	H	L	H	H	2-bit	L	H	L	H	L	H	H	DB3	H	L	L	H	L	H	L	H	H	L	L	L	L	H	2-bit									
L	L	L	H	H	L	L	unc	L	H	L	H	H	L	L	2-bit	H	L	L	H	H	L	L	L	L	L	L	L	L	L	DB18									
L	L	L	H	H	L	H	2-bit	L	H	L	H	H	L	H	DB2	H	L	L	H	H	L	L	L	L	L	L	L	L	L	2-bit									
L	L	L	H	H	H	L	2-bit	L	H	L	H	H	H	L	unc	H	L	L	H	H	H	L	L	L	L	L	L	L	L	2-bit									
L	L	L	H	H	H	H	DB30	L	H	L	H	H	H	H	2-bit	H	L	L	H	H	H	H	L	L	L	L	L	L	L	CB4									
L	L	H	L	L	L	L	2-bit	L	H	H	L	L	L	L	DB0	H	L	H	L	L	L	L	L	L	L	L	L	L	L	2-bit									
L	L	H	L	L	L	H	unc	L	H	H	L	L	L	H	2-bit	H	L	H	L	L	L	L	H	L	L	L	L	L	L	DB16									
L	L	H	L	L	L	L	DB29	L	H	H	L	L	H	L	2-bit	H	L	H	L	L	L	L	L	L	L	L	L	L	L	unc									
L	L	H	L	L	H	H	2-bit	L	H	H	L	L	H	H	unc	H	L	H	L	L	H	H	L	L	L	L	L	L	L	2-bit									
L	L	H	L	H	L	L	DB28	L	H	H	L	L	L	L	2-bit	H	L	H	L	L	L	L	L	L	L	L	L	L	L	DB17									
L	L	H	L	H	L	H	2-bit	L	H	H	L	H	L	H	DB1	H	L	L	H	L	L	H	L	L	L	L	L	L	L	2-bit									
L	L	H	L	H	H	L	2-bit	L	H	H	L	H	H	L	unc	H	L	L	H	H	L	L	L	L	L	L	L	L	L	2-bit									
L	L	H	L	H	H	H	DB27	L	H	H	L	H	H	H	2-bit	H	L	H	L	H	H	H	L	L	L	L	L	L	L	CB3									
L	L	H	H	L	L	L	DB26	L	H	H	H	L	L	L	2-bit	H	L	H	H	L	L	L	L	L	L	L	L	L	L	unc									
L	L	H	H	L	L	H	2-bit	L	H	H	H	L	L	H	unc	H	L	H	H	L	L	H	L	L	L	L	L	L	L	2-bit									
L	L	H	H	L	H	L	2-bit	L	H	H	H	L	L	L	unc	H	L	H	H	L	L	L	L	L	L	L	L	L	L	2-bit									
L	L	H	H	L	H	H	DB25	L	H	H	H	L	H	H	2-bit	H	L	H	H	L	H	L	L	L	L	L	L	L	L	CB2									
L	L	H	H	H	L	L	2-bit	L	H	H	H	H	L	L	unc	H	L	H	H	H	L	L	L	L	L	L	L	L	L	2-bit									
L	L	H	H	H	L	H	DB24	L	H	H	H	H	L	H	2-bit	H	L	H	H	H	L	L	L	L	L	L	L	L	L	CB1									
L	L	H	H	H	H	L	unc	L	H	H	H	H	L	L	2-bit	H	L	H	H	H	L	L	L	L	L	L	L	L	L	CB0									
L	L	H	H	H	H	H	2-bit	L	H	H	H	H	H	H	CB6	H	L	H	H	H	H	L	L	L	L	L	L	L	L	none									

CB X = error in check bit X
DB Y = error in data bit Y
2-bit = double-bit error
unc = uncorrectable multibit error

read-modify-write (byte control) operations

The 'AS632 is capable of byte-write operations. The 39-bit word from memory must first be latched into the DB and CB input latches. This is easily accomplished by switching from the read and flag mode (S1 = H, S0 = L) to the latch input mode (S1 = H, S0 = H). The EDAC will then make any corrections, if necessary, to the data word and place it at the input of the output data latch. This data word must then be latched into the output data latch by taking $\overline{\text{LEDB0}}$ from a low to a high.

Byte control can now be employed on the data word through the $\overline{\text{OEB0}}$ through $\overline{\text{OEB3}}$ controls. $\overline{\text{OEB0}}$ controls DB0-DB7 (byte 0), $\overline{\text{OEB1}}$ controls DB8-DB15 (byte 1), $\overline{\text{OEB2}}$ controls DB16-DB23 (byte 2), and $\overline{\text{OEB3}}$ controls DB24-DB31 (byte 3). Placing a high on the byte control will disable the output and the user can modify the byte. If a low is placed on the byte control, then the original byte is allowed to pass onto the data bus unchanged. If the original data word is altered through byte control, a new check word must be generated before it is written back into memory. This is easily accomplished by taking control S1 and S0 low. Table 6 lists the read-modify-write functions.

2
LSI Devices

**SN54AS632, SN54AS634
SN74AS632, SN74AS634
32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS**

TABLE 6. READ-MODIFY-WRITE FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1 S0	BYTE _n	$\overline{OE}B_n$	DB OUTPUT LATCH LEDB0	CHECK I/O	CB CONTROL	ERROR FLAG ERR MERR
Read	Read & Flag	H L	Input	H	X	Input	H	Enabled
Read	Latch input data & check bits	H H	Latched Input data	H	L	Latched input check word	H	Enabled
Read	Latch corrected data word into output latch	H H	Latched output data word	H	H	Hi-Z Output Syndrome bits	H L	Enabled
Modify /write	Modify appropriate byte or bytes & generate new check word	L L	Input modified BYTE0 Output unchanged BYTE0	H L	H	Output check word	L	H H

† $\overline{OE}B0$ controls DB0-DB7 (BYTE0), $\overline{OE}B1$ controls DB8-DB15 (BYTE1), $\overline{OE}B3$ controls DB16-DB23 (BYTE2), $\overline{OE}B3$ controls DB24-DB31 (BYTE3).

2

LSI Devices

diagnostic operations

The 'AS632 and 'AS634 are capable of diagnostics that allow the user to determine whether the EDAC or the memory is failing. The diagnostic function tables will help the user to see the possibilities for diagnostic control.

In the diagnostic mode (S1 = L, S0 = H), the checkword is latched into the input latch while the data input latch remains transparent. This lets the user apply various data words against a fixed known checkword. If the user applies a diagnostic data word with an error in any bit location, the \overline{ERR} flag should be low. If a diagnostic data word with two errors in any bit location is applied, the \overline{MERR} flag should be low. After the checkword is latched into the input latch, it can be verified by taking \overline{OECB} low. This outputs the latched checkword. With the 'AS632, the diagnostic data word can be latched into the output data latch and verified. It should be noted that the 'AS634 does not have this pass-through capability because they do not contain an output data latch. By changing from the diagnostic mode (S1 = L, S0 = H) to the correction mode (S1 = H, S0 = H), the user can verify that the EDAC will correct the diagnostic data word. Also, the syndrome bits can be produced to verify that the EDAC pinpoints the error location. Table 7 ('AS632) and Table 8 ('AS634) list the diagnostic functions.

32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

TABLE 7. 'AS632 DIAGNOSTIC FUNCTION

EDAC FUNCTION	CONTROL S1 S0	DATA I/O	DB BYTE CONTROL $\overline{\text{OEB}}_n$	DB OUTPUT LATCH $\overline{\text{LEDBO}}$	CHECK I/O	CB CONTROL $\overline{\text{OECB}}$		ERROR FLAGS ERR MERR	
Read & flag	H L	Input correct data word	H	X	Input correct check bits	H		H	H
Latch input check word while data input latch remains transparent	L H	Input diagnostic data word [†]	H	L	Latched input check bits	H		Enabled	
Latch diagnostic data word into output latch	L H	Input diagnostic data word [†]	H	H	Output latched check bits	L		Enabled	
Latch diagnostic data word into input latch	H H	Latched input diagnostic data word	H	H	Output syndrome bits	L		Enabled	
Output diagnostic data word & syndrome bits	H H	Output diagnostic data word	L	H	Output syndrome bits	L		Enabled	
Output corrected diagnostic data word & output syndrome bits	H H	Output corrected diagnostic data word	L	L	Output syndrome bits	L		Enabled	

TABLE 8. 'AS634 DIAGNOSTIC FUNCTION

EDAC FUNCTION	CONTROL S1 S0	DATA I/O	DB CONTROL $\overline{\text{OEDB}}$	CHECK I/O	DB CONTROL $\overline{\text{OECB}}$	ERROR FLAGS ERR MERR	
Read & flag	H L	Input correct data word	H	Input correct check bits	H		H H
Latch input check bits while data input latch remains transparent	L H	Input diagnostic data word [†]	H	Latched input check bits	H		Enabled
Output input check bits	L H	Input diagnostic data word [†]	H	Output input check bits	L		Enabled
Latch diagnostic data into input latch	H H	Latched input diagnostic data word	H	Output syndrome bits	L		Enabled
Output corrected diagnostic data word	H H	Output corrected diagnostic data word	L	Output syndrome bits	L		Enabled

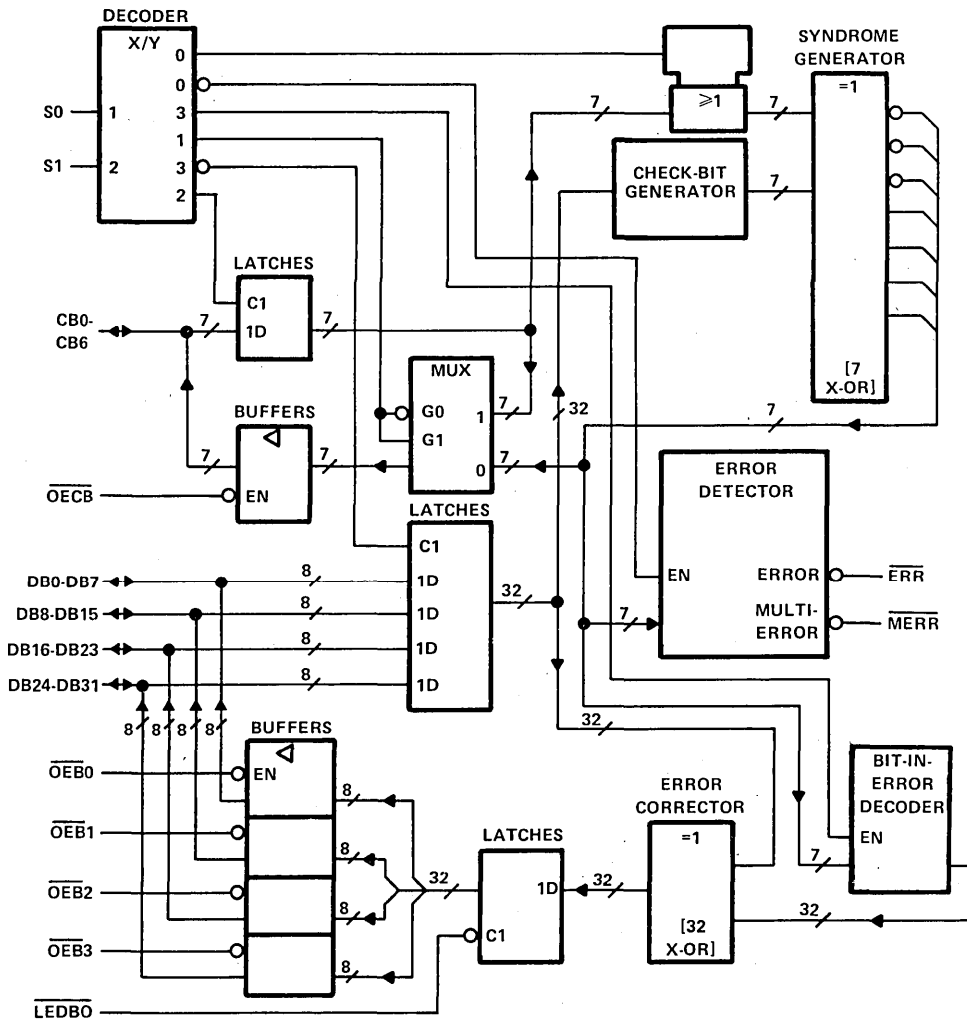
[†] Diagnostic data is a data word with an error in one bit location except when testing the $\overline{\text{MERR}}$ error flag. In this case, the diagnostic data word will contain errors in two bit locations.

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LSI Devices

SN54AS632, SN74AS632
32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

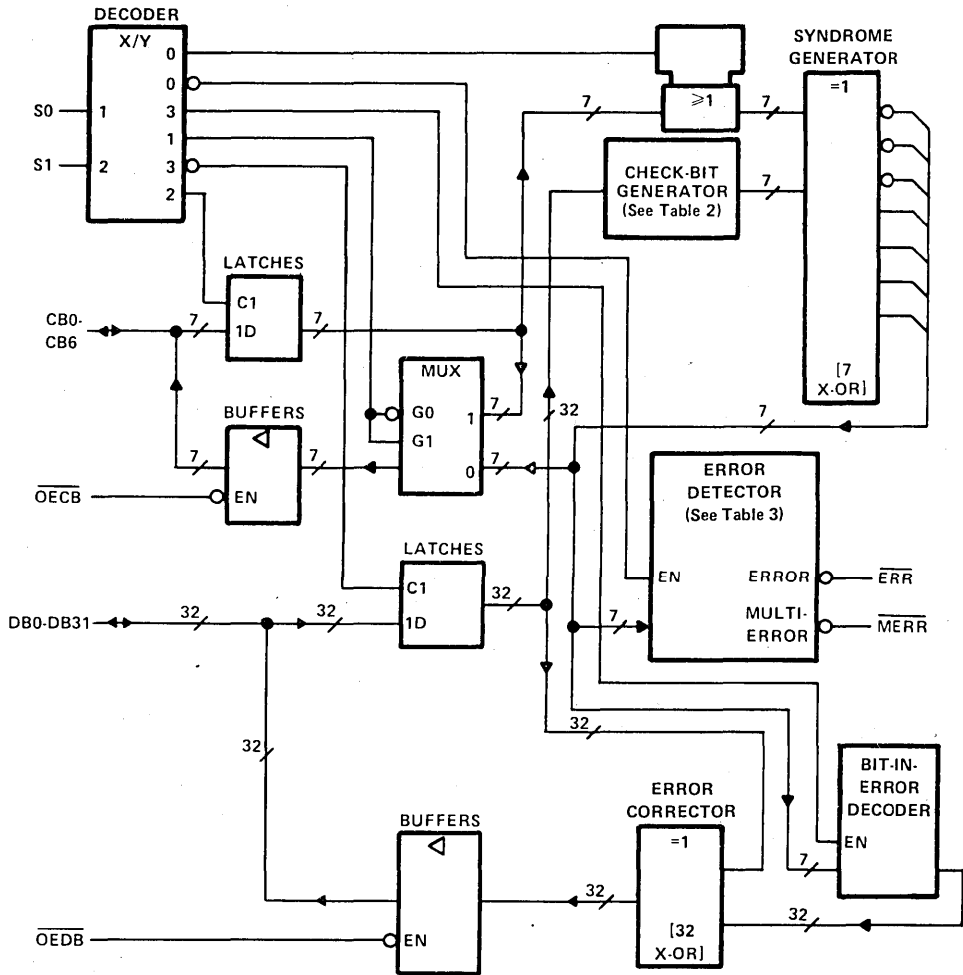
'AS632 logic diagram (positive logic)



2 LSI Devices

SN54AS634, SN74AS634
32-BIT PARALLEL ERROR DETECTIN AND CORRECTION CIRCUITS

'AS634 logic diagram (positive logic)



2

LSI Devices

SN54AS632, SN54AS634
SN74AS632, SN74AS634
32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: CB and DB	5.5 V
All others	7 V
Operating free-air temperature range:	
SN74AS632, SN74AS634	0°C to 70°C
Operating case temperature range:	
SN54AS632, SN54AS634	-55°C to 125°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54AS632			SN74AS632			UNIT	
		SN54AS634			SN74AS634				
		MIN	NOM	MAX	MIN	NOM	MAX		
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
V_{IH}	High-level input voltage	2			2			V	
V_{IL}	Low-level input voltage							V	
I_{OH}	High-level output current	ERR or MERR			-0.4			mA	
		DB or CB			-1				
I_{OL}	Low-level output current	ERR or MERR			4			mA	
		DB or CB			12				
t_w	Pulse duration	LEDBO low			25			ns	
t_{su}	Setup time	(1) Data and check word before $S0\uparrow$ ($S1 = H$)			15			ns	
		(2) $S0$ high before $LEDBO\uparrow$ ($S1 = H$) [†]			45				
		(3) $LEDBO$ high before the earlier of $S0\downarrow$ or $S1\downarrow$ [†]			0				
		(4) $LEDBO$ high before $S1\uparrow$ ($S0 = H$)			0				
		(5) Diagnostic data word before $S1\uparrow$ ($S0 = H$)			15				
		(6) Diagnostic check word before the later of $S1\downarrow$ or $S0\uparrow$			15				
		(7) Diagnostic data word before $LEDBO\uparrow$ ($S1 = L$ and $S0 = H$) [‡]			25				
t_h	Hold time	(8) Read-mode, $S0$ low and $S1$ high			35			ns	
		(9) Data and check word after $S0\uparrow$ ($S1 = H$)			20				
		(10) Data word after $S1\uparrow$ ($S0 = H$)			20				
		(11) Check word after the later of $S1\downarrow$ or $S0\uparrow$			20				
		(12) Diagnostic data word after $LEDBO\uparrow$ ($S1 = L$, $S0 = H$) [‡]			0				
t_{corr}	Correction time (see Figure 1)	65			58			ns	
T_C	Operating case temperature	-55			125			°C	
T_A	Operating free-air temperature				0			70	°C

[†] These times ensure that corrected data is saved in the output data latch.

[‡] These times ensure that the diagnostic data word is saved in the output data latch.

SN54AS632, SN54AS634, SN74AS632, SN74AS634

32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS WITH 3-STATE OUTPUTS

'AS632, 'AS634 electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS632 SN54AS634		SN74AS632 SN74AS634		UNIT	
		MIN	TYP [†] MAX	MIN	TYP [†] MAX		
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA	-1.5		-1.5		V	
V _{OH}	All outputs	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA		V _{CC} - 2		V	
	DB or CB	V _{CC} = 4.5 V, I _{OH} = -1 mA		2.4	3.3		
V _{OL}	ERR or MERR	V _{CC} = 4.5 V, I _{OH} = -2.6 mA		2.4 3.2		V	
		V _{CC} = 4.5 V, I _{OH} = 4 mA		0.25	0.4		0.25
	DB or CB	V _{CC} = 4.5 V, I _{OL} = 8 mA		0.35 0.5			
		V _{CC} = 4.5 V, I _{OL} = 12 mA		0.25	0.4		0.25
I _I	S0 or S1	V _{CC} = 5.5 V, V _I = 7 V		0.1		0.1	
	All others	V _{CC} = 5.5 V, V _I = 5.5 V		0.1		0.1	
I _{IH}	DB or CB [‡]	V _{CC} = 5.5 V, V _I = 2.7 V		20		20	
	All others [‡]			20		20	
I _{IL}	S0 or S1	V _{CC} = 5.5 V, V _I = 0.4 V		-0.4		-0.4	
	All others [‡]			-0.1		-0.1	
I _O [§]	V _{CC} = 5.5 V, V _O = 2.25 V	-30	-112	-30	-112	mA	
I _{CC}	V _{CC} = 5.5 V, See Note 1	150		150		mA	

NOTE 1: I_{CC} is measured with S0 and S1 at 4.5 V and all CB and DB pins grounded.

'AS632 switching characteristics, V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_C = -55°C to 125°C for SN54AS632, T_A = 0°C to 70°C for SN74AS632

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54AS632		SN74AS632		UNIT
				MIN	TYP [†] MAX	MIN	TYP [†] MAX	
t _{pd}	DB and CB	ERR	S1 = H, S0 = L, R _L = 500 Ω	17		17		ns
	DB	ERR	S1 = L, S0 = H, R _L = 500 Ω	17		17		
t _{pd}	DB and CB	MERR	S1 = H, S0 = L, R _L = 500 Ω	26		26		ns
	DB	MERR	S1 = L, S0 = H, R _L = 500 Ω	26		26		
t _{pd}	S0 _↓ and S1 _↓	CB	R1 = R2 = 500 Ω	26		26		ns
t _{PLH}	S0 _↓ and S1 _↓	ERR	R _L = 500 Ω	9		9		ns
t _{pd}	DB	CB	S1 = L, S0 = L, R1 = R2 = 500 Ω	26		26		ns
t _{pd}	LEDB0 _↓	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω	17		17		ns
t _{pd}	S1 _↑	CB	S0 = H, R1 = R2 = 500 Ω	26		26		ns
t _{en}	OE _{CB} _↓	CB	S0 = H, S1 = X, R1 = R2 = 500 Ω	12		12		ns
t _{dis}	OE _{CB} _↑	CB	S0 = H, S1 = X, R1 = R2 = 500 Ω	12		12		ns
t _{en}	OE _{B0} thru OE _{B3} _↓	DB	S0 = H, S1 = X, R1 = R2 = 500 Ω	12		12		ns
t _{dis}	OE _{B0} thru OE _{B3} _↑	DB	S0 = H, S1 = X, R1 = R2 = 500 Ω	12		12		ns

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

2

LSI Devices

SN54AS634, SN74AS634
32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS
WITH 3-STATE OUTPUTS

'AS634 switching characteristics, $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $T_C = -55^\circ\text{C to } 125^\circ\text{C}$
 for SN54AS634, $T_A = 0^\circ\text{C to } 70^\circ\text{C}$ for SN74AS634

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54AS634		SN74AS634		UNIT
				MIN	TYP†	MAX	MIN	
t_{pd}	DB and CB	$\overline{\text{ERR}}$	$S1 = H, S0 = L, R_L = 500 \Omega$		17		17	ns
			$S1 = L, S0 = H, R_L = 500 \Omega$		17		17	
t_{pd}	DB and CB	$\overline{\text{MERR}}$	$S1 = H, S0 = L, R_L = 500 \Omega$		26		26	ns
			$S1 = L, S0 = H, R_L = 500 \Omega$		26		26	
t_{pd}	$S0\downarrow$ and $S1\downarrow$	CB	$R1 = R2 = 500 \Omega$		23		23	ns
t_{PLH}	$S0\downarrow$ and $S1\downarrow$	$\overline{\text{ERR}}$	$R_L = 500 \Omega$		9		9	ns
t_{pd}	DB	CB	$S1 = L, S0 = L, R1 = R2 = 500 \Omega$		23		23	ns
t_{pd}	$S1\uparrow$	CB	$S0 = H, R1 = R2 = 500 \Omega$		23		23	ns
t_{en}	$\overline{\text{OECB}}\downarrow$	CB	$S1 = X, S0 = H, R1 = R2 = 500 \Omega$		12		12	ns
t_{dis}	$\overline{\text{OECB}}\uparrow$	CB	$S1 = X, S0 = H, R1 = R2 = 500 \Omega$		12		12	ns
t_{en}	$\overline{\text{OEDB}}\downarrow$	DB	$S1 = X, S0 = H, R1 = R2 = 500 \Omega$		12		12	ns
t_{dis}	$\overline{\text{OEDB}}\uparrow$	DB	$S1 = X, S0 = H, R1 = R2 = 500 \Omega$		12		12	ns

†All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

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LSI Devices

32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

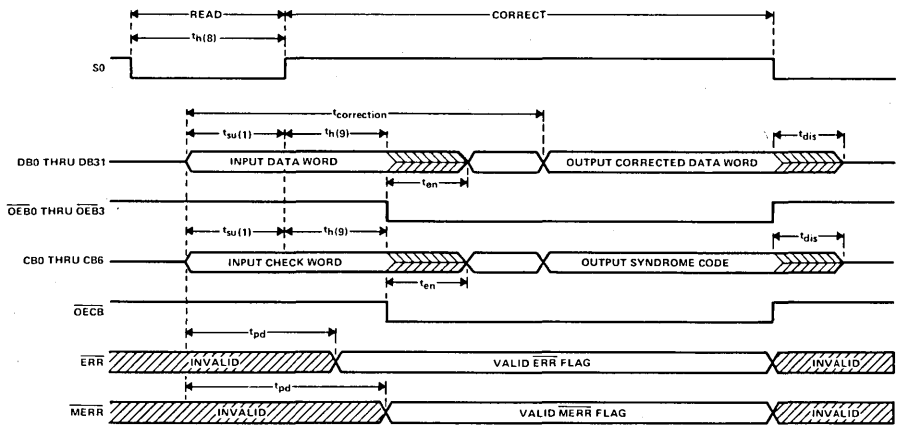


FIGURE 1. READ, FLAG, AND CORRECT MODE SWITCHING WAVEFORMS

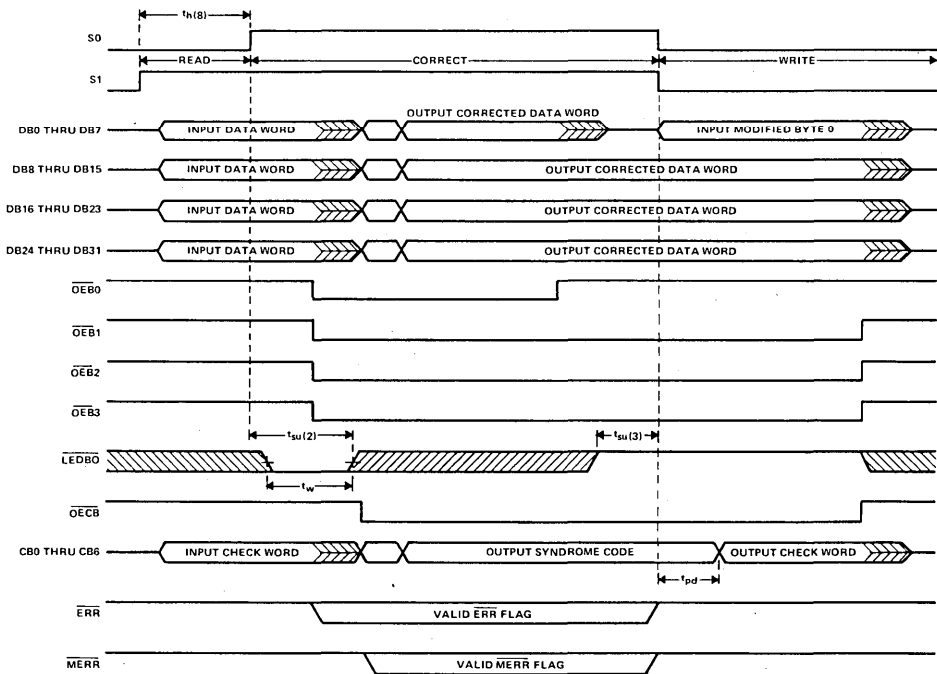


FIGURE 2. READ, CORRECT, MODIFY MODE SWITCHING WAVEFORMS

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LSI Devices

**SN54AS632, SN54AS634
 SN74AS632, SN74AS634
 32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS**

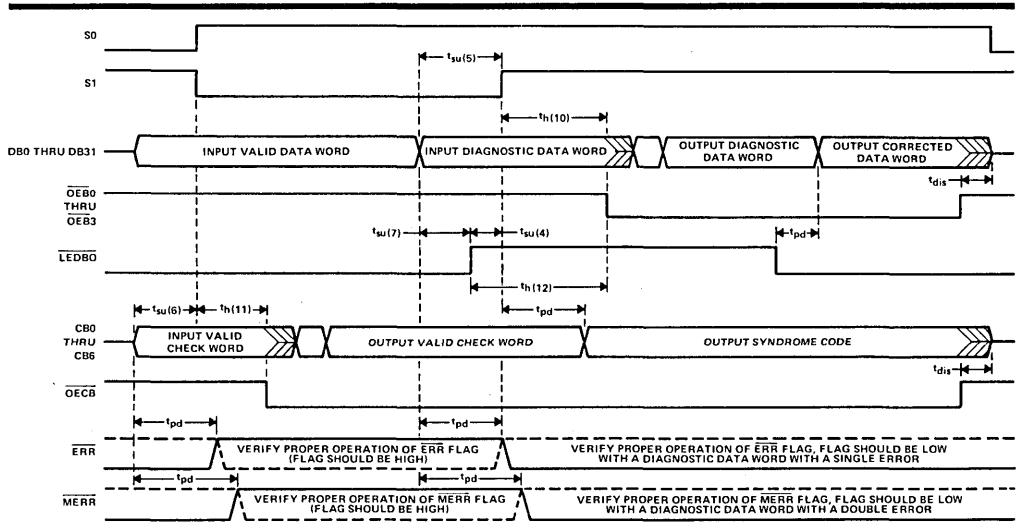


FIGURE 3. DIAGNOSTIC MODE SWITCHING WAVEFORM

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LSI Devices

SN54ALS646 THRU SN54ALS649, SN54AS646, SN54AS648 SN74ALS646 THRU SN74ALS649, SN74AS646, SN74AS648 OCTAL BUS TRANSCEIVERS AND REGISTERS

D2661, DECEMBER 1983—NOVEMBER 1985

- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True or Inverting Data Paths
- Choice of 3-State or Open-Collector Outputs
- Included Among the Package Options Are Compact 24-pin 300-mil Wide DIPs and Both 28-pin Plastic and Ceramic Chip Carriers
- Dependable Texas Instruments Quality and Reliability

DEVICE	OUTPUT	LOGIC
'ALS646, 'AS646	3-State	True
'ALS647	Open-Collector	True
'ALS648, 'AS648	3-State	Inverting
'ALS649	Open-Collector	Inverting

description

These devices consist of bus transceiver circuits, with 3-state or open-collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

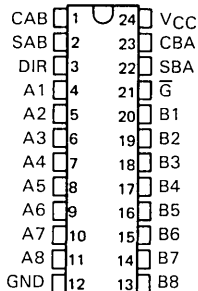
Enable (\bar{G}) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The circuitry used for select control will eliminate the typical decoding glitch which occurs in a multiplexer during the transition between stored and real-time data. The direction control determines which bus will receive data when enable \bar{G} is active (low). In the isolation mode (control \bar{G} high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

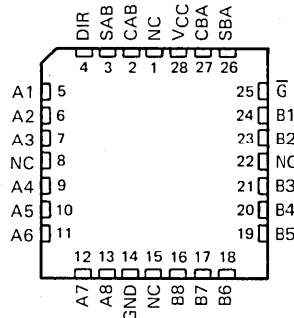
The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS' parts.

The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74' family is characterized for operation from 0°C to 70°C .

SN54ALS', SN54AS' . . . JT PACKAGE
SN74ALS', SN74AS' . . . DW OR NT PACKAGE
(TOP VIEW)

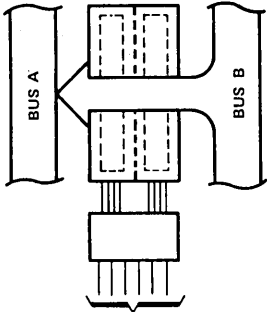


SN54ALS', SN54AS' . . . FK PACKAGE
SN74ALS', SN74AS' . . . FN PACKAGE
(TOP VIEW)



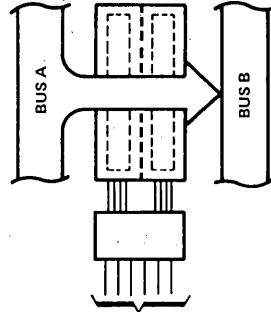
NC—No internal connection

**SN54ALS646 THRU SN54ALS649, SN54AS646, SN54AS648
 SN74ALS646 THRU SN74ALS649, SN74AS646, SN74AS648
 OCTAL BUS TRANSCEIVERS AND REGISTERS**



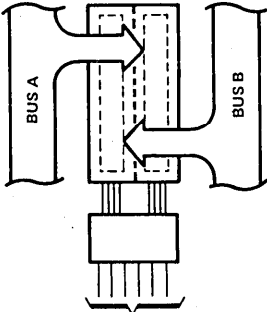
(21)	(3)	(1)	(23)	(2)	(22)
G	DIR	CAB	CBA	SAB	SBA
L	L	X	X	X	L

**REAL-TIME TRANSFER
 BUS B TO BUS A**



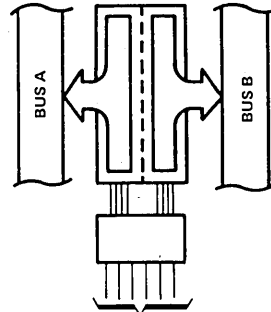
(21)	(3)	(1)	(23)	(2)	(22)
G	DIR	CAB	CBA	SAB	SBA
L	H	X	X	L	X

**REAL-TIME TRANSFER
 BUS A TO BUS B**



(21)	(3)	(1)	(23)	(2)	(22)
G	DIR	CAB	CBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

**STORAGE FROM
 A, B, OR A AND B**



(21)	(3)	(1)	(23)	(2)	(22)
G	DIR	CAB	CBA	SAB	SBA
L	L	X	HorL	X	H
L	H	HorL	X	H	X

**TRANSFER
 STORED DATA
 TO A OR B**

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LSI Devices

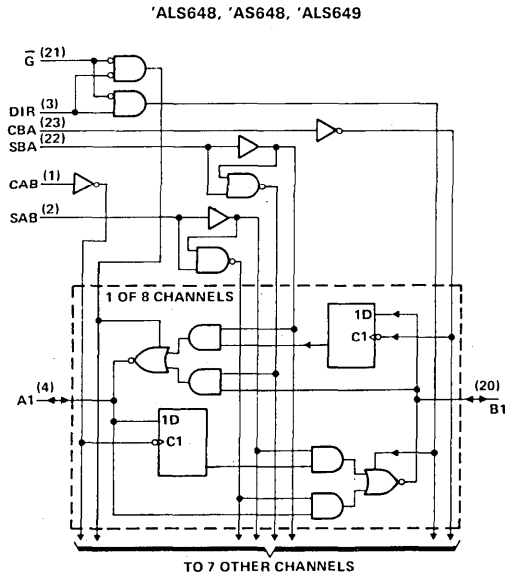
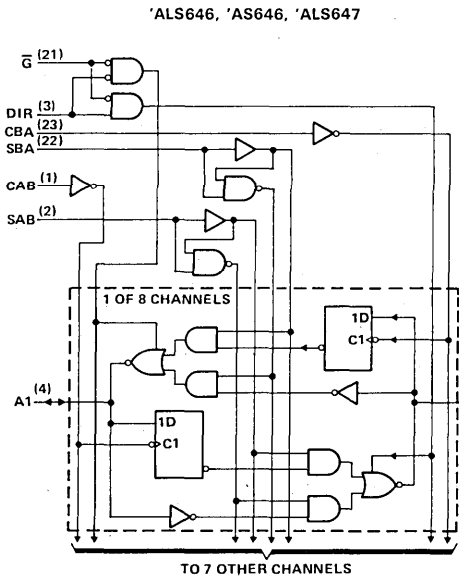
SN54ALS646 THRU SN54ALS649, SN54AS646, SN54AS648 SN74ALS646 THRU SN74ALS649, SN74AS646, SN74AS648 OCTAL BUS TRANSCEIVERS AND REGISTERS

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION	
G	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'ALS646, 'ALS647 'AS646	'ALS648, 'ALS649 'AS648
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time \bar{B} Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored B Data to A Bus	Stored \bar{B} Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time \bar{A} Data to B Bus
L	H	H or L	X	H	X	Input	Output	Stored A Data to B Bus	Store \bar{A} Data to B Bus

†The data output functions may be enabled or disabled by various signals at the \bar{G} and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

functional block diagrams (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

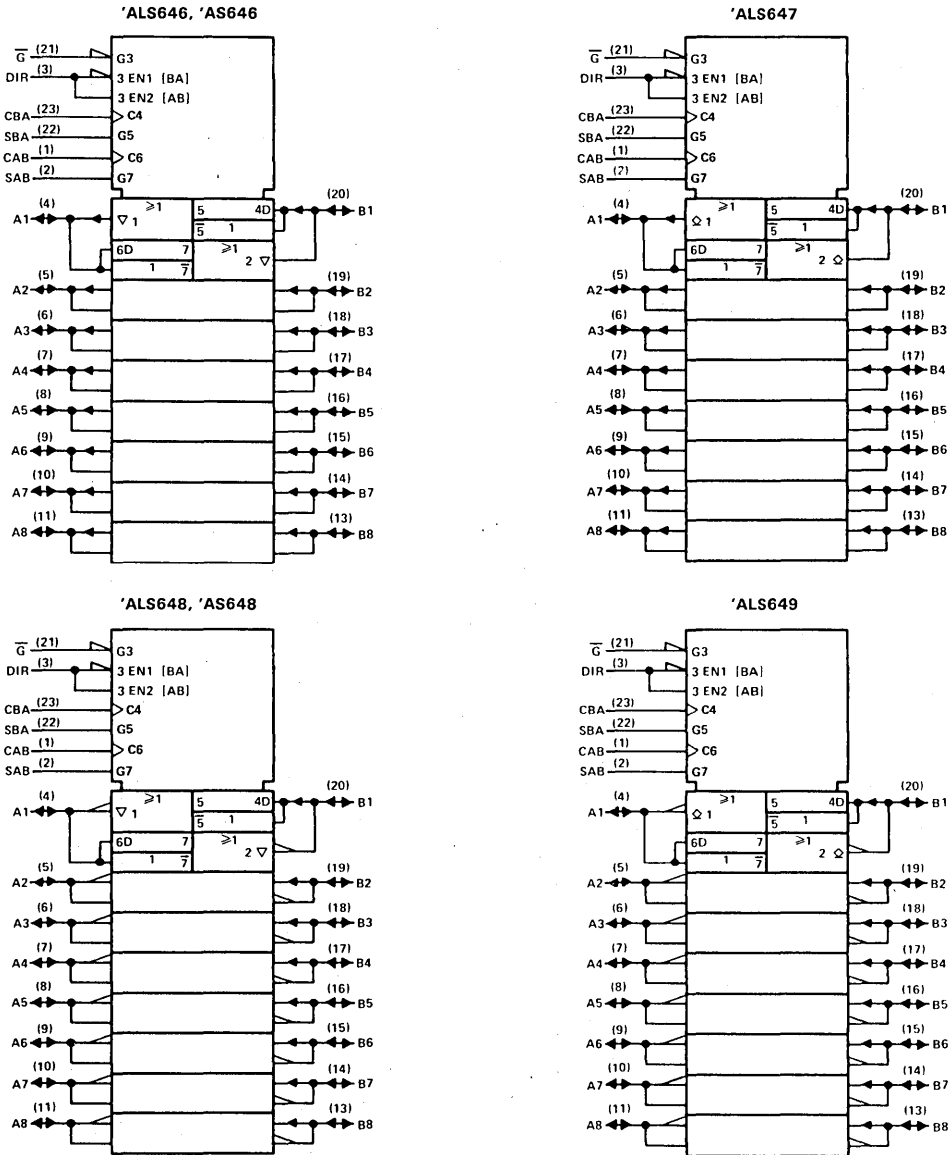
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LSI Devices

**SN54ALS646 THRU SN54ALS649, SN54AS646, SN54AS648
SN74ALS646 THRU SN74ALS649, SN74AS646, SN74AS648
OCTAL BUS TRANSCEIVERS AND REGISTERS**

logic symbols†

2 LSI Devices



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.

SN54ALS646, SN74ALS646

OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage: Control inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range: SN54ALS646	-55°C to 125°C
SN74ALS646	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54ALS646			SN74ALS646			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage				0.8			V
I_{OH}	High-level output current				-12			mA
I_{OL}	Low-level output current				12			mA
I_{OL}	Low-level output current				24			mA
I_{OL}	Low-level output current				48 [†]			mA
f_{clock}	Clock frequency	0			35			MHz
t_w	Pulse duration, clocks high or low	14.5			12.5			ns
t_{su}	Setup time, A before CAB [†] or B before CBA [†]	15			10			ns
t_h	Hold time, A after CAB [†] or B after CBA [†]	0			0			ns
T_A	Operating free-air temperature	-55			125			°C

[†]The extended condition applies if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48 mA limit applies for the SN74ALS646-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ALS646		SN74ALS646		UNIT
			MIN	TYP [‡]	MAX	MIN	
V_{IK}		$V_{CC} = 4.5\text{ V}, I_I = -18\text{ mA}$			-1.2		V
V_{OH}		$V_{CC} = 4.5\text{ V to } 5.5\text{ V}, I_{OH} = -0.4\text{ mA}$	$V_{CC}-2$		$V_{CC}-2$		V
		$V_{CC} = 4.5\text{ V}, I_{OH} = -3\text{ mA}$	2.4	3.2	2.4	3.2	
		$V_{CC} = 4.5\text{ V}, I_{OH} = -12\text{ mA}$	2				
		$V_{CC} = 4.5\text{ V}, I_{OH} = -15\text{ mA}$			2		
V_{OL}		$V_{CC} = 4.5\text{ V}, I_{OL} = 12\text{ mA}$	0.25	0.4	0.25	0.4	V
		$V_{CC} = 4.5\text{ V}, I_{OL} = 24\text{ mA}$ ($I_{OL} = 48\text{ mA}$ for -1 version)			0.35	0.5	
I_I	Control inputs A or B ports	$V_{CC} = 5.5\text{ V}, V_I = 7\text{ V}$			0.1		mA
		$V_{CC} = 5.5\text{ V}, V_I = 5.5\text{ V}$			0.1		
I_{IH}	Control inputs A or B ports [§]	$V_{CC} = 5.5\text{ V}, V_I = 2.7\text{ V}$	20		20		μA
			20		20		
I_{IL}	Control inputs A or B ports [§]	$V_{CC} = 5.5\text{ V}, V_I = 0.4\text{ V}$	-0.2		-0.2		mA
			-0.2		-0.2		
I_O^{\dagger}		$V_{CC} = 5.5\text{ V}, V_O = 2.25\text{ V}$	-30	-112	-30	-112	mA
I_{CC}		$V_{CC} = 5.5\text{ V}$	Outputs high		47 76		mA
			Outputs low		55 88		
			Outputs disabled		55 88		

[‡]All typical values are at $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$

[§]For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[†]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

2

LSI Devices

SN54ALS646, SN74ALS646
OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS

'ALS646 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX			UNIT	
			'ALS646			SN54ALS646		SN74ALS646		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
f _{max}			50			35	40		MHz	
t _{PLH}	CBA or CAB	A or B	20	25	10	35	10	30	ns	
t _{PHL}			11	15	5	20	5	17		
t _{PLH}	A or B	B or A	11	17	5	22	5	20	ns	
t _{PHL}			7.5	10	3	15	3	12		
t _{PLH}	SBA or SAB [†] (with A or B high)	A or B	24	32	15	40	15	35	ns	
t _{PHL}			13	17	5	23	5	20		
t _{PLH}	SBA or SAB [†] (with A or B low)	A or B	17	22	8	30	8	25	ns	
t _{PHL}			13	17	5	24	5	20		
t _{PZH}	\bar{G}	A or B	10	15	3	20	3	17	ns	
t _{PZL}			10	15	5	22	5	20		
t _{PHZ}	\bar{G}	A or B	6	8	1	12	1	10	ns	
t _{PLZ}			10	13	2	20	2	16		
t _{PZH}	DIR	A or B	22	28	10	38	10	30	ns	
t _{PZL}			14.5	20	5	30	5	25		
t _{PHZ}	DIR	A or B	6	8	1	12	1	10	ns	
t _{PLZ}			10	13	2	21	2	16		

[†] These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS647, SN74ALS647

OCTAL BUS TRANSCEIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Operating free-air temperature range: SN54ALS647	-55°C to 125°C
SN74ALS647	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54ALS647			SN74ALS647			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage				0.8			V
V_{OH}	High-level output voltage				5.5			V
I_{OL}	Low-level output current				12			mA
					24			
					48†			
f_{clock}	Clock frequency	0			25			MHz
t_w	Pulse duration, clocks high or low	20			16.5			ns
t_{su}	Setup time, A before CAB† or B before CBA†	15			10			ns
t_h	Hold time, A after CAB† or B after CBA†	0			0			ns
T_A	Operating free-air temperature	-55			125			°C

†The extended condition applies if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS647-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS647		SN74ALS647		UNIT
		MIN	TYP‡ MAX	MIN	TYP† MAX	
V_{IK}	$V_{CC} = 4.5$ V, $I_I = -18$ mA	-1.2		-1.2		V
I_{OH}	$V_{CC} = 4.5$ V, $V_{OH} = 5.5$ V	0.1		0.1		mA
V_{OL}	$V_{CC} = 4.5$ V, $I_{OL} = 12$ mA	0.25 0.4				V
	$V_{CC} = 4.5$ V, $I_{OL} = 24$ mA ($I_{OL} = 48$ mA for -1 versions)			0.35 0.5		
I_I	A or B ports	$V_{CC} = 5.5$ V, $V_I = 7$ V		0.1		mA
	Control inputs	$V_{CC} = 5.5$ V, $V_I = 7$ V		0.1		
I_{IH}	A or ports‡	$V_{CC} = 5.5$ V, $V_I = 2.7$ V		20		µA
	Control inputs			20		
I_{IL}	Control inputs	$V_{CC} = 5.5$ V, $V_I = 0.4$ V		-0.2		mA
	A or B ports‡			-0.2		
I_{CC}	$V_{CC} = 5.5$ V	Outputs high	35 60	35 60	60	mA
		Outputs low	40 65	40 65	65	

‡All typical values are at $V_{CC} = 5$ V, $T_A = 25$ °C

§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

2
LSI Devices

SN54ALS647, SN74ALS647
OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH OPEN-COLLECTOR OUTPUTS

ALS647 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R _L = 680 Ω, T _A = 25 °C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 680 Ω, T _A = MIN to MAX				UNIT
			'ALS647			SN54ALS647		SN74ALS647		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			40			25		30		MHz
t _{PLH}	CBA or CAB	A or B	38	50	19	72	19	58	ns	
t _{PHL}			12	20	6	24	6	22		
t _{PLH}	A or B	B or A	35	39	17	70	17	54	ns	
t _{PHL}			10	13	4	19	4	16		
t _{PLH}	SBA or SAB† (with A or B high)	A or B	40	51	20	72	20	60	ns	
t _{PHL}			12	17	6	26	6	22		
t _{PLH}	SBA or SAB† (with A or B low)	A or B	40	51	20	72	20	60	ns	
t _{PHL}			12	17	6	26	6	22		
t _{PLH}	\bar{G}	A or B	20	27	10	37	10	31	ns	
t _{PHL}			10	15	2	20	2	17		
t _{PLH}	DIR	A or B	20	25	9	34	9	29	ns	
t _{PHL}			13	17	2	22	2	19		

†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of *The TTL Data Book*, Volume 3, 1984.

2

LSI Devices

SN54ALS648, SN74ALS648 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage: Control inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range: SN54ALS648	-55°C to 125°C
SN74ALS648	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54ALS648			SN74ALS648			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-12			-15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
f_{clock}	Clock frequency	0		35	0		40	MHz
t_w	Pulse duration, clocks high or low	14.5			12.5			ns
t_{su}	Setup time, A before CAB† or B before CBA†	15			10			ns
t_h	Hold time, A after CAB† or B after CBA†	0			0			ns
T_A	Operating free-air temperature	-55		125	0		70	°C

†The extended condition applies if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS648-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ALS648		SN74ALS648		UNIT	
			MIN	TYP‡	MAX	MIN		TYP‡
V_{IK}		$V_{CC} = 4.5\text{ V}, I_I = -18\text{ mA}$			-1.2		-1.2	V
V_{OH}		$V_{CC} = 4.5\text{ V to } 5.5\text{ V}, I_{OH} = -0.4\text{ mA}$	$V_{CC}-2$			$V_{CC}-2$		V
		$V_{CC} = 4.5\text{ V}, I_{OH} = -3\text{ mA}$	2.4	3.2		2.4	3.2	
		$V_{CC} = 4.5\text{ V}, I_{OH} = -12\text{ mA}$	2					
		$V_{CC} = 4.5\text{ V}, I_{OH} = -15\text{ mA}$				2		
V_{OL}		$V_{CC} = 4.5\text{ V}, I_{OL} = 12\text{ mA}$	0.25	0.4		0.25	0.4	V
		$V_{CC} = 4.5\text{ V}, I_{OL} = 24\text{ mA}$				-0.35	0.5	
		($I_{OL} = 48\text{ mA}$ for -1 version)						
I_I	Control inputs	$V_{CC} = 5.5\text{ V}, V_I = 7\text{ V}$			0.1		0.1	mA
	A or B ports	$V_{CC} = 5.5\text{ V}, V_I = 5.5\text{ V}$			0.1		0.1	
I_{IH}	Control inputs	$V_{CC} = 5.5\text{ V}, V_I = 2.7\text{ V}$			20		20	μA
	A or B ports§				20		20	
I_{IL}	Control inputs	$V_{CC} = 5.5\text{ V}, V_I = 0.4\text{ V}$			-0.2		-0.2	mA
	A or B ports§				-0.2		-0.2	
I_O^\dagger		$V_{CC} = 5.5\text{ V}, V_O = 2.25\text{ V}$	-30		-112	-30		mA
I_{CC}		$V_{CC} = 5.5\text{ V}$	Outputs high	47	76	47	76	mA
			Outputs low	57	88	57	88	
			Outputs disabled	57	88	57	88	

‡All typical values are at $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$

§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

†The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

2

LSI Devices

SN54ALS648, SN74ALS648
OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS

ALS648 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX			UNIT			
			ALS648			SN54ALS648		SN74ALS648				
			MIN	TYP	MAX	MIN	MAX	MIN		MAX		
f _{max}			50			35		40		MHz		
t _{PLH}	CBA or CAB	A or B	21			8		39		33	ns	
t _{PHL}			13			5		23				
t _{PLH}	A or B	B or A	10			3		20		3	17	ns
t _{PHL}			6			2		12				
t _{PLH}	SBA or SAB† (with A or B high)	A or B	24			5		44		5	39	ns
t _{PHL}			15			4		26				
t _{PLH}	SBA or SAB† (with A or B low)	A or B	16			6		30		6	25	ns
t _{PHL}			14			6		25				
t _{PLH}	0	A or B	12			4		25		4	22	ns
t _{PHL}			12			4		25				
t _{PLH}	0	A or B	5			1		12		1	10	ns
t _{PHL}			7			2		21				
t _{PZH}	DIR	A or B	14			4		35		4	27	ns
t _{PZL}			10			3		25				
t _{PHZ}	DIR	A or B	7			1		17		1	14	ns
t _{PLZ}			7			2		22				

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
 NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS649, SN74ALS649

OCTAL BUS TRANSCEIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Operating free-air temperature range: SN54ALS649	-55°C to 125°C
SN74ALS649	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54ALS649			SN74ALS649			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage	0.8			0.8			V
V_{OH}	High-level output voltage	5.5			5.5			V
I_{OL}	Low-level output current	12			24			mA
					48†			
f_{clock}	Clock frequency	0			25			MHz
t_w	Pulse duration, clocks high or low	20			16.5			ns
t_{su}	Setup time, A before CAB† or B before CBA†	15			10			ns
t_h	Hold time, A after CAB† or B after CBA†	0			0			ns
T_A	Operating free-air temperature	-55			125			°C

†The extended condition applies if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS649-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ALS649		SN74ALS649		UNIT
			MIN	TYP‡	MAX	MIN	
V_{IK}		$V_{CC} = 4.5\text{ V}, I_I = -18\text{ mA}$	-1.2		-1.2		V
I_{OH}		$V_{CC} = 4.5\text{ V}, V_{OH} = 5.5\text{ V}$	0.1		0.1		mA
V_{OL}		$V_{CC} = 4.5\text{ V}, I_{OL} = 12\text{ mA}$	0.25		0.4		V
		$V_{CC} = 4.5\text{ V}, I_{OL} = 24\text{ mA}$ ($I_{OL} = 48\text{ mA}$ for -1 versions)			0.35		
I_I	A or B ports	$V_{CC} = 5.5\text{ V}, V_I = 7\text{ V}$	0.1		0.1		mA
	Control inputs	$V_{CC} = 5.5\text{ V}, V_I = 7\text{ V}$	0.1		0.1		
I_{IH}	A or ports§	$V_{CC} = 5.5\text{ V}, V_I = 2.7\text{ V}$	20		20		µA
	Control inputs		20		20		
I_{IL}	Control inputs	$V_{CC} = 5.5\text{ V}, V_I = 0.4\text{ V}$	-0.2		-0.2		mA
	A or B ports§		-0.2		-0.2		
I_{CC}		$V_{CC} = 5.5\text{ V}$	Outputs high		40 60		mA
			Outputs low		45 70		

‡All typical values are at $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$

§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

2

LSI Devices

SN54ALS649, SN74ALS649
OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH OPEN-COLLECTOR OUTPUTS

'ALS649 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R _L = 680 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 680 Ω, T _A = MIN to MAX			UNIT			
			'ALS649			SN54ALS649		SN74ALS649				
			MIN	TYP	MAX	MIN	MAX	MIN		MAX		
f _{max}			40			25		30		MHz		
t _{PLH}	CBA or CAB	A or B	40			52		19		77		ns
t _{PHL}			12			18		6		22		
t _{PLH}	A or B	B or A	30			41		13		65		ns
t _{PHL}			6			9		2		11		
t _{PLH}	SBA or SAB [†] (with A or B high)	A or B	35			46		20		72		ns
t _{PHL}			15			21		6		26		
t _{PLH}	SBA or SAB [†] (with A or B low)	A or B	35			46		20		72		ns
t _{PHL}			15			21		6		26		
t _{PLH}	\bar{G}	A or B	16			22		8		28		ns
t _{PHL}			13			18		2		23		
t _{PLH}	DIR	A or B	16			22		8		28		ns
t _{PHL}			13			17		2		23		

[†] These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
 NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

2 LSI Devices

SN54AS646, SN54AS648, SN74AS646, SN74AS648 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage: Control inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range: SN54AS646, SN54AS648	-55°C to 125°C
SN74AS646, SN74AS648	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54AS646			SN74AS646			UNIT
		SN54AS648			SN74AS648			
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-12			-15	mA
I_{OL}	Low-level output current			32			48	mA
f_{clock}	Clock frequency	0	75		0	90		MHz
t_w	Pulse duration	Clock high		6	5			ns
		Clock high		7	6			
t_{su}	Setup time, A before CAB† or B before CBA†	7			6			ns
t_h	Hold time, A after CAB† or B after CBA†	0			0			ns
T_A	Operating free-air temperature	-55	125		0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS646			SN74AS646			UNIT
		SN54AS648			SN74AS648			
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5 V, I_I = -18 mA$	-1.2			-1.2			V
V_{OH}	$V_{CC} = 4.5 V$ to $5.5 V, I_{OH} = -2 mA$	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5 V, I_{OH} = -3 mA$	2.4	3.2		2.4	3.2		
	$V_{CC} = 4.5 V, I_{OH} = -12 mA$	2						
	$V_{CC} = 4.5 V, I_{OH} = -15 mA$				2			
V_{OL}	$V_{CC} = 4.5 V, I_{OL} = 32 mA$	0.25	0.50					V
	$V_{CC} = 4.5 V, I_{OL} = 48 mA$				0.35	0.50		
I_I	Control inputs $V_{CC} = 5.5 V, V_I = 7 V$				0.1			mA
	A or B ports $V_{CC} = 5.5 V, V_I = 5.5 V$				0.1			
I_{IH}	Control inputs $V_{CC} = 5.5 V, V_I = 2.7 V$				20			μA
	A or B ports‡				70			
I_{IL}	Control inputs $V_{CC} = 5.5 V, V_I = 0.4 V$				-0.5			mA
	A or B ports§				-0.75			
$I_{O§}$	$V_{CC} = 5.5 V, V_O = 2.25 V$	-30	-112		-30	-112		mA
I_{CC}	'AS646	$V_{CC} = 5.5 V$	Outputs high	120	195	120	195	mA
			Outputs low	130	211	130	211	
			Outputs disabled	130	211	130	211	
			Outputs high	110	185	110	185	
			Outputs low	120	195	120	195	
			Outputs disabled	120	195	120	195	
'AS648	$V_{CC} = 5.5 V$	Outputs high	120	195	120	195	mA	
		Outputs low	130	211	130	211		
		Outputs disabled	130	211	130	211		
		Outputs high	110	185	110	185		
		Outputs low	120	195	120	195		
		Outputs disabled	120	195	120	195		

† All typical values are at $V_{CC} = 5 V, T_A = 25^\circ C$

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

LSI Devices

2

SN54AS646, SN54AS648, SN74AS646, SN74AS648
OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS

'AS646 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX				UNIT
			SN54AS646		SN74AS646		
			MIN	MAX	MIN	MAX	
f _{max}			75		90		MHz
t _{PLH}	CBA or CAB	A or B	2	9.5	2	8.5	ns
t _{PHL}			2	10	2	9	
t _{PLH}	A or B	B or A	2	11	2	9	ns
t _{PHL}			1	8	1	7	
t _{PLH}	SBA or SAB†	A or B	2	12	2	11	ns
t _{PHL}			2	10	2	9	
t _{PZH}	\bar{G}	A or B	2	10	2	9	ns
t _{PZL}			3	15	3	14	
t _{PHZ}	\bar{G}	A or B	2	11	2	9	ns
t _{PLZ}			2	11	2	9	
t _{PZH}	DIR	A or B	3	19	3	16	ns
t _{PZL}			3	21	3	18	
t _{PHZ}	DIR	A or B	2	12	2	10	ns
t _{PLZ}			2	12	2	10	

'AS648 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX				UNIT
			SN54AS648		SN74AS648		
			MIN	MAX	MIN	MAX	
f _{max}			75		90		MHz
t _{PLH}	CBA or CAB	A or B	2	9.5	2	8.5	ns
t _{PHL}			2	10	2	9	
t _{PLH}	A or B	B or A	2	9	2	8	ns
t _{PHL}			1	8	1	7	
t _{PLH}	SBA or SAB†	A or B	2	12	2	11	ns
t _{PHL}			2	10	2	9	
t _{PZH}	\bar{G}	A or B	2	10	2	9	ns
t _{PZL}			3	18	3	15	
t _{PHZ}	\bar{G}	A or B	2	11	2	9	ns
t _{PLZ}			2	11	2	9	
t _{PZH}	DIR	A or B	3	19	3	16	ns
t _{PZL}			3	21	3	18	
t _{PHZ}	DIR	A or B	2	12	2	10	ns
t _{PLZ}			2	12	2	10	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

2

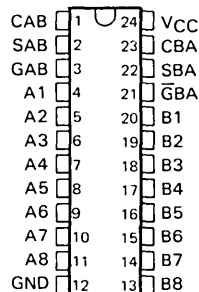
LSI Devices

SN54ALS651 THRU SN54ALS654, SN54AS651, SN54AS652 SN74ALS651 THRU SN74ALS654, SN74AS651, SN74AS652 OCTAL BUS TRANSCEIVERS AND REGISTERS

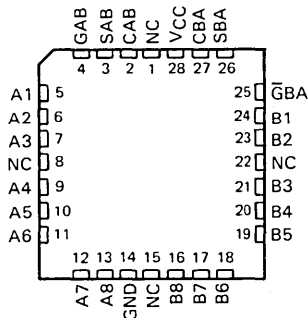
D2661, DECEMBER 1983 - REVISED NOVEMBER 1985

- Bus Transceivers/Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True and Inverting Data Paths
- Choice of 3-State or Open-Collector Outputs to A Bus
- Included Among the Package Options Are Compact 24-Pin 300-mil-Wide DIPs and Both 28-Pin Plastic and Ceramic Chip Carriers
- Dependable Texas Instruments Quality and Reliability

SN54ALS', SN54AS' . . . JT PACKAGE
SN74ALS', SN74AS' . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE
SN74ALS', SN74AS' . . . FN PACKAGE
(TOP VIEW)



NC - No internal connection

DEVICE	A OUTPUT	B OUTPUT	LOGIC
'ALS651, 'AS651	3-State	3-State	Inverting
'ALS652, 'AS652	3-State	3-State	True
'ALS653	Open-Collector	3-State	Inverting
'ALS654	Open-Collector	3-State	True

description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and $\bar{G}BA$ are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch which occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\bar{G}BA$. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The -1 versions of the SN74ALS651 through SN74ALS654 are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS651 through SN54ALS654.

The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74' family is characterized for operation from 0°C to 70°C .

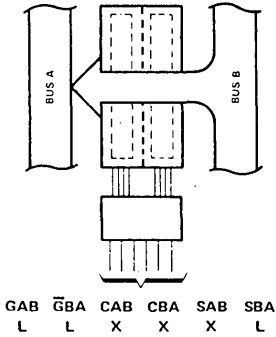
This document contains information on products in more than one phase of development. The status of each device is indicated on the page(s) specifying its electrical characteristics.

TEXAS
INSTRUMENTS

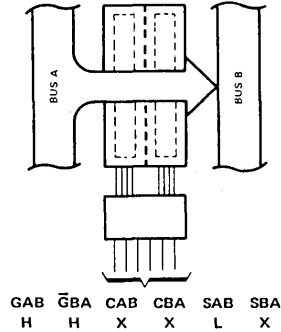
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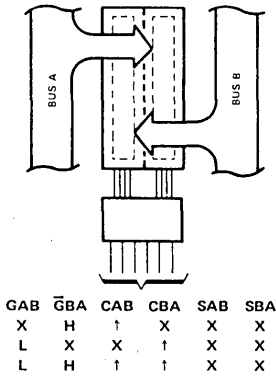
**SN54ALS651 THRU SN54ALS654, SN54AS651, SN54AS652
SN74ALS651 THRU SN74ALS654, SN74AS651, SN74AS652
OCTAL BUS TRANSCEIVERS AND REGISTERS**



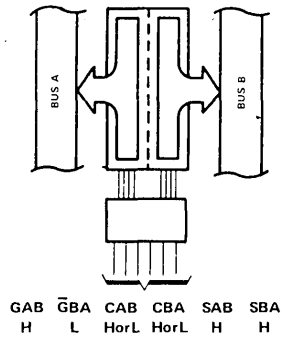
REAL-TIME TRANSFER
BUS B TO BUS A



REAL-TIME TRANSFER
BUS A TO BUS B



STORAGE FROM
A AND/OR B



TRANSFER
STORED DATA
TO A AND/OR B

2

LSI Devices

SN54ALS651 THRU SN54ALS654, SN54AS651, SN54AS652 SN74ALS651 THRU SN74ALS654, SN74AS651, SN74AS652 OCTAL BUS TRANSCEIVERS AND REGISTERS

FUNCTION TABLE

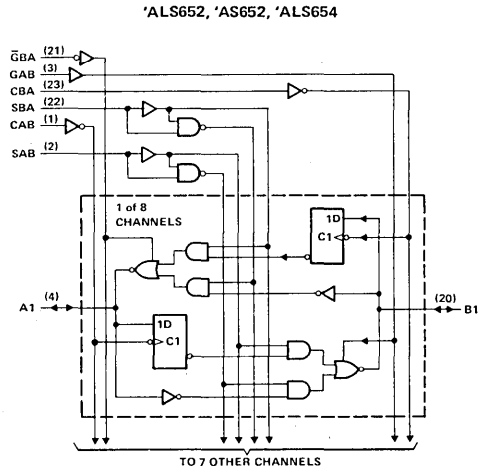
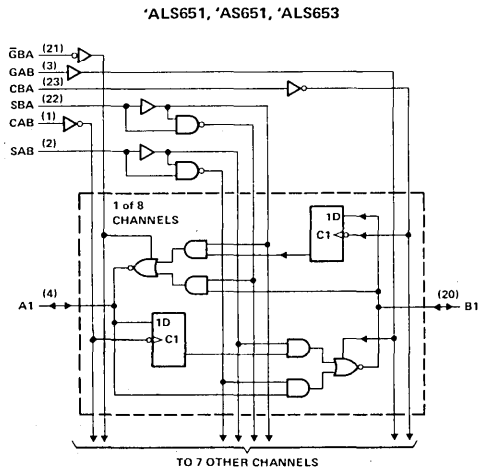
INPUTS						DATA I/O		OPERATION OR FUNCTION	
GAB	$\bar{G}BA$	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'ALS651, 'ALS653 'AS651	'ALS652, 'ALS654 'AS652
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	*	*	X	X	Input	Input	Store A and B Data	Store A and B Data
X	H	*	H or L	X	X	Input	Unspecified [†]	Store A, Hold B	Store A, Hold B
H	H	*	*	X [‡]	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	*	X	X	Unspecified [†]	Input	Hold A, Store B	Hold A, Store B
L	L	*	*	X	X [‡]	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time \bar{B} Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored \bar{B} Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time \bar{A} Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X	Input	Output	Stored \bar{A} Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored \bar{A} Data to B Bus and Stored \bar{B} Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

[†]The data output functions may be enabled or disabled by various signals at the GAB or $\bar{G}BA$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

[‡]Select control = L: clocks can occur simultaneously.

Select control = H: clocks must be staggered in order to load both registers.

logic diagrams (positive logic)



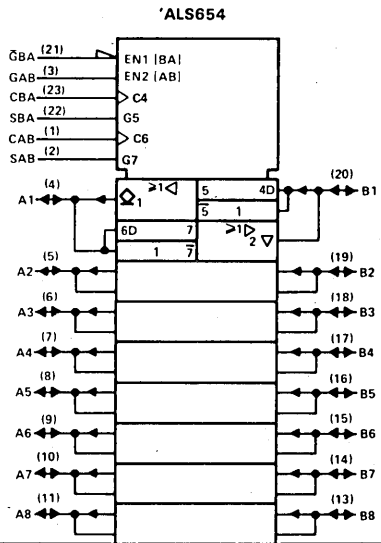
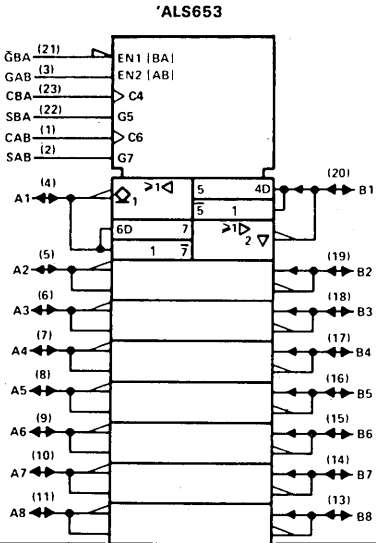
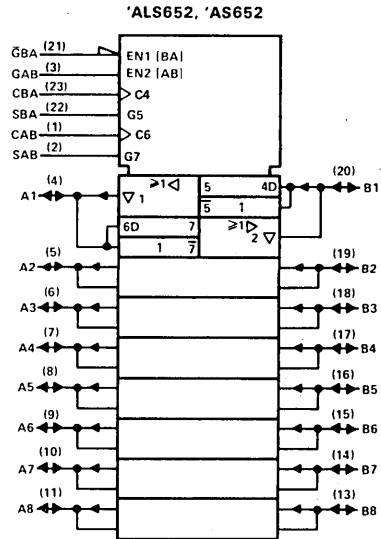
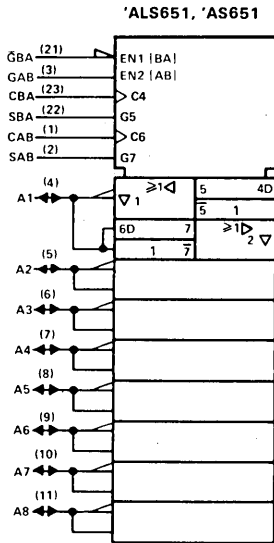
Pin numbers shown are for DW, JT, and NT packages.

2

LSI Devices

**SN54ALS651 THRU SN54ALS654, SN54AS651, SN54AS652
SN74ALS651 THRU SN74ALS654, SN74AS651, SN74AS652
OCTAL BUS TRANSCEIVERS AND REGISTERS**

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.

SN54ALS651, SN54ALS652, SN74ALS651, SN74ALS652 OCTAL BUS TRANSCEIVERS AND REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage: Control inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range: SN54ALS651, SN54ALS652	-55°C to 125°C
SN74ALS651, SN74ALS652	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54ALS651 SN54ALS652			SN74ALS651 SN74ALS652			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-12			-15	mA
I_{OL}	Low-level output current			12			24 48†	mA
f_{clock}	Clock frequency	0		35	0		40	MHz
t_w	Pulse duration	CBA or CAB high		14.5	12.5			ns
		CBA or CAB low		14.5	12.5			
t_{su}	Setup time before CAB† or CBA†	A or B		15	10			ns
t_h	Hold time after CAB† or CBA†	A or B		5	0			ns
T_A	Operating free-air temperature	-55		125	0		70	°C

† The extended condition applies if V_{CC} is maintained between 4.75 V and 5.25 V. The 48-mA limit applies for the SN74ALS651 - 1 and SN74ALS652 - 1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS651 SN54ALS652			SN74ALS651 SN74ALS652			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$	-1.2			-1.2			V
V_{OH}	$V_{CC} = 4.5 \text{ V}$ to 5.5 V , $I_{OH} = -0.4 \text{ mA}$	$V_{CC}-2$			$V_{CC}-2$			V
	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		
	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -12 \text{ mA}$	2						
	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -15 \text{ mA}$	2						
V_{OL}	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 12 \text{ mA}$	0.25	0.4		0.25	0.4	V	
	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 24 \text{ mA}$ ($I_{OL} = 48 \text{ mA}$ for -1 versions)	0.35 0.5						
I_I	Control inputs	$V_{CC} = 5.5 \text{ V}$, $V_I = 7 \text{ V}$			0.1			mA
	A or B ports	$V_{CC} = 5.5 \text{ V}$, $V_I = 5.5 \text{ V}$			0.1			
I_{IH}	Control inputs	$V_{CC} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$			20			μA
	A or B ports§	$V_{CC} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$			20			
I_{IL}	Control inputs	$V_{CC} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$			-0.2			mA
	A or B ports§	$V_{CC} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$			-0.2			
I_{O1}	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.25 \text{ V}$	-30		-112	-30		-112	mA
I_{CC}	'ALS651	$V_{CC} = 5.5 \text{ V}$	Outputs high	42	68	42	68	mA
			Outputs low	52	82	52	82	
			Outputs disabled	52	82	52	82	
			Outputs high	47	76	47	76	
			Outputs low	55	88	55	88	
			Outputs disabled	55	88	55	88	
I_{CC}	'ALS652	$V_{CC} = 5.5 \text{ V}$	Outputs high	42	68	42	68	mA
			Outputs low	52	82	52	82	
			Outputs disabled	52	82	52	82	
			Outputs high	47	76	47	76	
			Outputs low	55	88	55	88	
			Outputs disabled	55	88	55	88	

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

† The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

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2

LSI Devices

SN54ALS651, SN54ALS652, SN74ALS651, SN74ALS652

OCTAL BUS TRANSCEIVERS AND REGISTERS

ALS651 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX			UNIT							
			ALS651			SN54ALS651		SN74ALS651								
			MIN	TYP	MAX	MIN	MAX	MIN		MAX						
f _{max}			50			35		40		MHz						
t _{PLH}	CBA or CAB	A or B	20			27		10		38		10		32		ns
t _{PHL}			11			15		5		21		5		17		ns
t _{PLH}	A or B	B or A	9			13		4		20		4		18		ns
t _{PHL}			5			8		2		12		2		10		ns
t _{PLH}	SBA or SAB† (with A or B high)	A or B	24			31		13		45		13		38		ns
t _{PHL}			13			18		7		25		7		21		ns
t _{PLH}	SBA or SAB† (with A or B low)	A or B	15			20		8		30		8		25		ns
t _{PHL}			13			18		7		25		7		21		ns
t _{PZH}	G̅BA	A	12			16		5		22		5		20		ns
t _{PZL}			11			15		5		21		5		18		ns
t _{PHZ}	G̅BA	A	4			7		2		10		2		9		ns
t _{PLZ}			7			10		3		16		3		12		ns
t _{PZH}	GAB	B	14			19		7		25		7		22		ns
t _{PZL}			13			18		7		25		7		21		ns
t _{PHZ}	GAB	B	5			10		2		14		2		12		ns
t _{PLZ}			7			10		2		20		2		14		ns

ALS652 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX			UNIT							
			ALS652			SN54ALS652		SN74ALS652								
			MIN	TYP	MAX	MIN	MAX	MIN		MAX						
f _{max}			50			35		40		MHz						
t _{PLH}	CBA or CAB	A or B	20			25		10		35		10		30		ns
t _{PHL}			11			15		5		20		5		17		ns
t _{PLH}	A or B	B or A	11			15		5		20		5		18		ns
t _{PHL}			8			10		3		15		3		12		ns
t _{PLH}	SBA or SAB† (with A or B high)	A or B	24			32		15		40		15		35		ns
t _{PHL}			13			17		6		23		6		20		ns
t _{PLH}	SBA or SAB† (with A or B low)	A or B	17			22		8		30		8		25		ns
t _{PHL}			13			17		5		24		5		20		ns
t _{PZH}	G̅BA	A	10			15		3		20		3		17		ns
t _{PZL}			10			14		5		22		5		18		ns
t _{PHZ}	G̅BA	A	6			8		1		12		1		10		ns
t _{PLZ}			10			13		2		20		2		16		ns
t _{PZH}	GAB	B	15			20		8		25		8		22		ns
t _{PZL}			12			16		6		21		6		18		ns
t _{PHZ}	GAB	B	6			8		1		12		1		10		ns
t _{PLZ}			10			13		2		21		2		16		ns

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage: All inputs and A I/O ports	7 V
B I/O ports	5.5 V
Operating free-air temperature range: SN54ALS653, SN54ALS654	-55 °C to 125 °C
SN74ALS653, SN74ALS654	0 °C to 70 °C
Storage temperature range	-65 °C to 150 °C

recommended operating conditions

		SN54ALS653			SN74ALS653			UNIT		
		SN54ALS654			SN74ALS654					
		MIN	NOM	MAX	MIN	NOM	MAX			
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V		
V_{IH}	High-level input voltage	2			2			V		
V_{IL}	Low-level input voltage	0.8			0.8			V		
V_{OH}	High-level output voltage	5.5			5.5			V		
I_{OH}	High-level output current	-12			-15			mA		
I_{OL}	Low-level output current	12			24			mA		
					48 [†]					
f_{clock}	Clock frequency							MHz		
t_w	Pulse duration	CBA or CAB high						ns		
		CBA or CAB low								
t_{su}	Setup time before CAB [†] or CBA [†]	A or B						ns		
t_h	Hold time after CAB [†] or CBA [†]	A or B						ns		
T_A	Operating free-air temperature	-55			125			0	70	°C

[†] The extended condition applies if V_{CC} is maintained between 4.75 V and 5.25 V. The 48-mA limit applies for the SN74ALS653 - 1 and SN74ALS654 - 1 only.

2
LSI Devices

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ALS653 SN54ALS654			SN74ALS653 SN74ALS654			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$	-1.5			-1.5			V
V_{OH}	B ports	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $I_{OH} = -0.4 \text{ mA}$	$V_{CC}-2$			$V_{CC}-2$			V
		$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		
		$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -12 \text{ mA}$	2						
		$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -15 \text{ mA}$				2			
I_{OH}	A ports	$V_{CC} = 4.5 \text{ V}$, $V_{OH} = 5.5 \text{ V}$	0.1			0.1			mA
V_{OL}		$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 12 \text{ mA}$	0.25	0.4		0.25	0.4	V	
		$V_{CC} = 4.75 \text{ V}$, $I_{OL} = 24 \text{ mA}$				0.35	0.5		
		$(I_{OL} = 48 \text{ mA for } -1 \text{ versions})$							
I_I	Control inputs	$V_{CC} = 5.5 \text{ V}$, $V_I = 7 \text{ V}$	0.1			0.1			mA
	A or B ports	$V_{CC} = 5.5 \text{ V}$, $V_I = 5.5 \text{ V}$	0.1			0.1			
I_{IH}	Control inputs	$V_{CC} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$	20			20			μA
	A or B ports‡		20			20			
I_{IL}	Control inputs	$V_{CC} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$	-0.1			-0.1			mA
	A or B ports‡		-0.2			-0.2			
I_O^{\S}	B ports	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.25 \text{ V}$	-30	-112		-30	-112	mA	
I_{CC}	'ALS653	$V_{CC} = 5.5 \text{ V}$	Outputs high		52	52		mA	
			Outputs low		57	57			
			Outputs disabled		58	58			
			Outputs high		60	60			
			Outputs low		68	68			
			Outputs disabled		68	68			
	'ALS654	$V_{CC} = 5.5 \text{ V}$	Outputs high		52	52		mA	
			Outputs low		57	57			
			Outputs disabled		58	58			
			Outputs high		60	60			
			Outputs low		68	68			
			Outputs disabled		68	68			

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For I/P ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

2

LSI Devices



'ALS653 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ $C_L = 50 \text{ pF}$ $R_L = 680 \Omega$, (A outputs) $R_1 = R_2 = 500 \Omega$, (B outputs) $T_A = \text{MIN to MAX}$						UNIT
			SN54ALS653			SN74ALS653			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}									MHz
t_{PLH}	CBA	A	24			24			ns
t_{PHL}			15			15			
t_{PLH}	CAB	B	11			11			ns
t_{PHL}			13			13			
t_{PLH}	A	B	10			10			ns
t_{PHL}			12			12			
t_{PLH}	B	A	24			24			ns
t_{PHL}			10			10			
t_{PLH}	SBA‡ (with B high)	A	26			26			ns
t_{PHL}			15			15			
t_{PLH}	SBA‡ (with B low)	A	26			26			ns
t_{PHL}			15			15			
t_{PLH}	SAB‡ (with A high)	B	16			16			ns
t_{PHL}			16			16			
t_{PLH}	SAB‡ (with A low)	B	15			15			ns
t_{PHL}			15			15			
t_{PLH}	\bar{G} BA	A	24			24			ns
t_{PHL}			17			17			
t_{PZH}	GAB	B	19			19			ns
t_{PZL}			22			22			
t_{PHZ}	GAB	B	12			12			ns
t_{PLZ}			14			14			

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

Additional information on these products can be obtained from the factory as it becomes available.

2

LSI Devices

SN54ALS654, SN74ALS654
OCTAL BUS TRANSCEIVERS AND REGISTERS

**PRODUCT
 PREVIEW**

ALS654 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 680 Ω, (A outputs) R ₁ = R ₂ = 500 Ω, (B outputs) T _A = MIN to MAX						UNIT
			SN54ALS654			SN74ALS654			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f _{max}									MHz
t _{PLH}	CBA	A	24			24			ns
t _{PHL}			15			15			
t _{PLH}	CAB	B	11			11			ns
t _{PHL}			13			13			
t _{PLH}	A	B	8			8			ns
t _{PHL}			8			8			
t _{PLH}	B	A	24			24			ns
t _{PHL}			10			10			
t _{PLH}	SBA‡ (with B high)	A	26			26			ns
t _{PHL}			15			15			
t _{PLH}	SBA‡ (with B low)	A	26			26			ns
t _{PHL}			15			15			
t _{PLH}	SBA‡ (with A high)	B	16			16			ns
t _{PHL}			16			16			
t _{PLH}	SAB‡ (with A low)	B	15			15			ns
t _{PHL}			12			12			
t _{PLH}	G̅BA	A	24			24			ns
t _{PHL}			17			17			
t _{PZH}	GAB	B	19			19			ns
t _{PZL}			22			22			
t _{PHZ}	GAB	B	12			12			ns
t _{PLZ}			14			14			

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

Additional information on these products can be obtained from the factory as it becomes available.

2 LSI Devices

SN54AS651, SN54AS652, SN74AS651, SN74AS652 OCTAL BUS TRANSCEIVERS AND REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage: Control inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range: SN54AS651, SN54AS652	-55 °C to 125 °C
SN74AS651, SN74AS652	0 °C to 70 °C
Storage temperature range	-65 °C to 150 °C

recommended operating conditions

		SN54AS651 SN54AS652			SN74AS651 SN74AS652			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-12			-15	mA
I_{OL}	Low-level output current			32			48	mA
f_{clock}		0		75	0		90	MHz
t_w	Pulse duration	CBA or CAB high		6	5			ns
		CBA or CAB low		7	6			
t_{su}	Setup time before $CAB\uparrow$ or $CBA\uparrow$	A or B		7	6			ns
t_h	Hold time after $CAB\uparrow$ or $CBA\uparrow$	A or B		0	0			ns
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS651 SN54AS652			SN74AS651 SN74AS652			UNIT
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
V_{IK}		$V_{CC} = 4.5 V$,	$I_I = -18 mA$			-1.2			-1.2	V
V_{OH}		$V_{CC} = 4.5 V$ to $5.5 V$,	$I_{OH} = -2 mA$	$V_{CC}-2$		$V_{CC}-2$				
		$V_{CC} = 4.5 V$,	$I_{OH} = -3 mA$	2.4	3.2	2.4	3.2		V	
		$V_{CC} = 4.5 V$,	$I_{OH} = -12 mA$	2						
		$V_{CC} = 4.5 V$,	$I_{OH} = -15 mA$			2				
V_{OL}		$V_{CC} = 4.5 V$,	$I_{OL} = 32 mA$	0.25	0.50					
		$V_{CC} = 4.5 V$,	$I_{OL} = 48 mA$			0.35	0.50		V	
I_I	Control inputs	$V_{CC} = 5.5 V$,	$V_I = 7 V$			0.1		0.1	mA	
	A or B ports	$V_{CC} = 5.5 V$,	$V_I = 5.5 V$			0.1		0.1		
I_{IH}	Control inputs	$V_{CC} = 5.5 V$,	$V_I = 2.7 V$			20		20	μA	
	A or B ports [‡]					70		70		
I_{IL}	Control inputs	$V_{CC} = 5.5 V$,	$V_I = 0.4 V$			-0.5		-0.5	mA	
	A or B ports [‡]					-0.75		-0.75		
I_O^{\S}		$V_{CC} = 5.5 V$,	$V_O = 2.25 V$	-30		-112		-30	-112	mA
I_{CC}	'AS651	$V_{CC} = 5.5 V$	Outputs high	110	185	110	185	mA		
			Outputs low	120	195	120	195			
			Outputs disabled	130	195	130	195			
	'AS652		Outputs high	120	195	120	195			
			Outputs low	130	211	130	211			
			Outputs disabled	130	211	130	211			

[†]All typical values are at $V_{CC} = 5 V$, $T_A = 25^\circ C$.

[‡]For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

SN54AS651, SN54AS654, SN74AS651, SN74AS652 OCTAL BUS TRANSCEIVERS AND REGISTERS

'AS651 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $R_1 = 500 \Omega$, $R_2 = 500 \Omega$, $T_A = \text{MIN to MAX}$				UNIT
			SN54AS651		SN74AS651		
			MIN	MAX	MIN	MAX	
f_{max}			75		90		MHz
t_{PLH}	CBA or CAB	A or B	2	9.5	2	8.5	ns
t_{PHL}			2	10	2	9	
t_{PLH}	A or B	B or A	2	9	2	8	ns
t_{PHL}			1	8	1	7	
t_{PLH}	SBA or SAB [†]	A or B	2	12	2	11	ns
t_{PHL}			2	10	2	9	
t_{PZH}	\bar{G} BA	A	2	11	2	10	ns
t_{PZL}			3	18	3	16	
t_{PHZ}	\bar{G} BA	A	2	10	2	9	ns
t_{PLZ}			2	10	2	9	
t_{PZH}	GAB	B	3	12	3	11	ns
t_{PZL}			3	20	3	16	
t_{PHZ}	GAB	B	2	11	2	10	ns
t_{PLZ}			2	12	2	11	

'AS652 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $R_1 = 500 \Omega$, $R_2 = 500 \Omega$, $T_A = \text{MIN to MAX}$				UNIT
			SN54AS652		SN74AS652		
			MIN	MAX	MIN	MAX	
f_{max}			75		90		MHz
t_{PLH}	CBA or CAB	A or B	2	9.5	2	8.5	ns
t_{PHL}			2	10	2	9	
t_{PLH}	A or B	B or A	2	11	2	9	ns
t_{PHL}			1	8	1	7	
t_{PLH}	SBA or SAB [†]	A or B	2	12	2	11	ns
t_{PHL}			2	10	2	9	
t_{PZH}	\bar{G} BA	A	2	11	2	10	ns
t_{PZL}			3	18	3	16	
t_{PHZ}	\bar{G} BA	A	2	10	2	9	ns
t_{PLZ}			2	10	2	9	
t_{PZH}	GAB	B	3	12	3	11	ns
t_{PZL}			3	20	3	16	
t_{PHZ}	GAB	B	2	11	2	10	ns
t_{PLZ}			2	12	2	11	

[†]These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS666, SN54ALS667, SN74ALS666, SN74ALS667 8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES WITH 3-STATE OUTPUTS

D2855, JUNE 1984—REVISED DECEMBER 1985

- 3-State I/O-Type Read-Back Inputs
- Bus-Structured Pinout
- Choice of True or Inverting Logic
 - 'ALS666 . . . True Outputs
 - 'ALS667 . . . Inverting Outputs
- Preset and Clear Inputs
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramics DIPs
- Dependable Texas Instruments Quality and Reliability

description

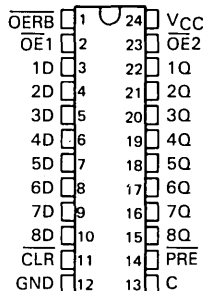
These 8-bit latches are designed specifically for storing the contents of the input data bus plus providing the capability of reading-back the stored data onto the input data bus. In addition, they provide a 3-state buffer type output and are easily utilized in bus-structured applications.

The eight latches of the 'ALS666 and 'ALS667 are transparent D-type. While the enable (C) is high, the Q outputs of the 'ALS666 will follow the data (D) inputs. On the 'ALS667, the \bar{Q} outputs will provide the inverse of what is applied to its data (D) inputs. On both devices, the Q or \bar{Q} output will be in the high-impedance state if either output control, $\bar{OE}1$ or $\bar{OE}2$, is at a high logic level.

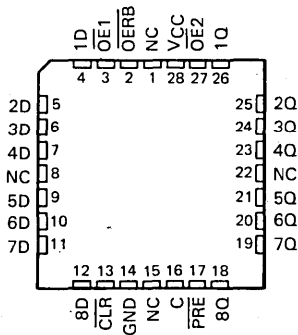
Read-back is provided thru the read-back control input (\bar{OERB}). When \bar{OERB} is taken low, the data present at the output of the data latches will be allowed to pass back onto the input data bus. When it is taken high, the output of the data latches will be isolated from the data (D) inputs. The read-back control does not affect the internal operation of the latches; however, caution should be exercised not to create a bus-conflict situation.

The SN54ALS666 and SN54ALS667 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS666 and SN75ALS667 are characterized for operation from 0°C to 70°C .

SN54ALS666 . . . JT PACKAGE
SN74ALS666 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS666 . . . FK PACKAGE
SN74ALS666 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection.

2

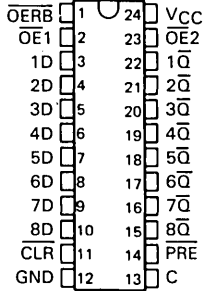
LSI Devices

SN54ALS666, SN54ALS667, SN74ALS666, SN74ALS667

8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES WITH 3-STATE OUTPUTS

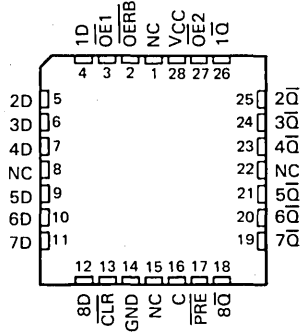
SN54ALS667 . . . JT PACKAGE
SN74ALS667 . . . DW OR NT PACKAGE

(TOP VIEW)



SN54ALS667 . . . FK PACKAGE
SN74ALS667 . . . FN PACKAGE

(TOP VIEW)

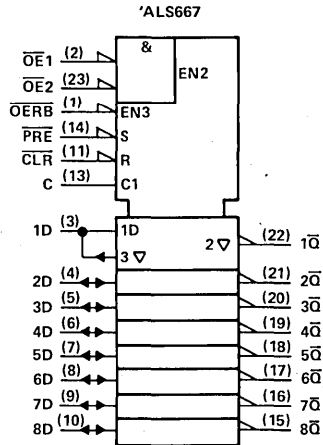
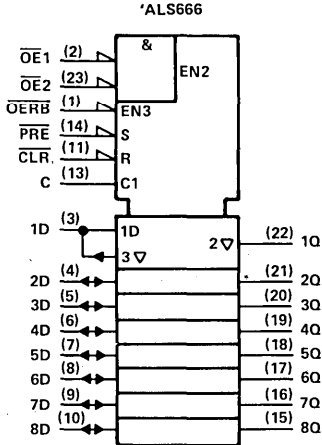


NC—No internal connection.

2

logic symbols†

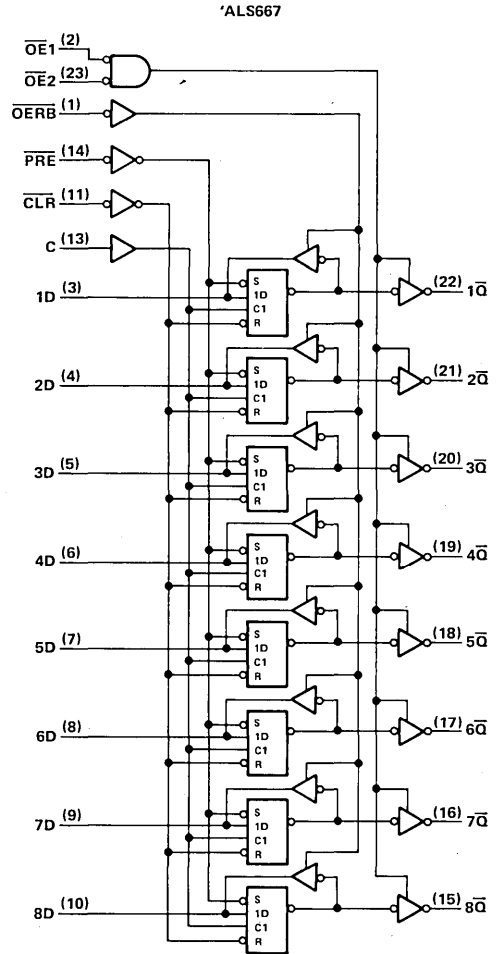
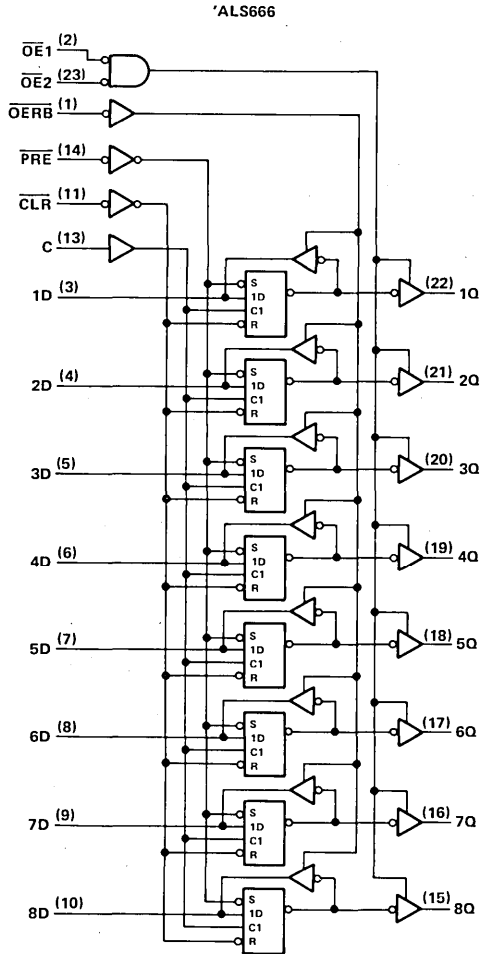
LSI Devices



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.

SN54ALS666, SN54ALS667, SN74ALS666, SN74ALS667
8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES
WITH 3-STATE OUTPUTS

logic diagrams (positive logic)

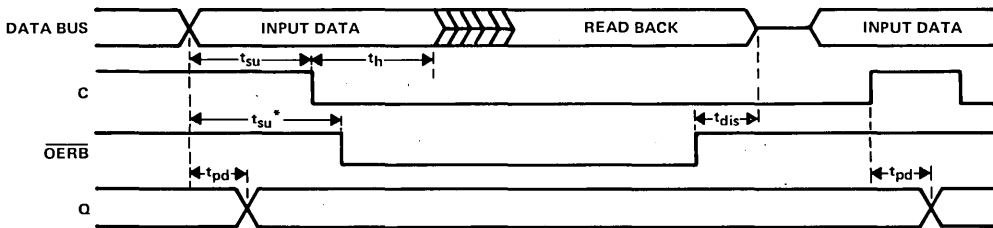


Pin numbers shown are for DW, JT, and NT packages.

2
LSI Devices

SN54ALS666, SN54ALS667, SN74ALS666, SN74ALS667
8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES
WITH 3-STATE OUTPUTS

timing diagram



$\overline{\text{CLR}} = \text{H}, \overline{\text{PRE}} = \text{H}, \overline{\text{OE1}} = \text{L}, \overline{\text{OE2}} = \text{L}$

*This setup time ensures the readback circuit will not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage (all inputs except D input)	7 V
Voltage applied to D inputs and to disabled 3-state outputs	5.5 V
Operating free-air temperature range: SN54ALS666, SN54ALS667	-55°C to 125°C
SN74ALS666, SN74ALS667	0°C to 70°C
Storage temperature range	-65°C to 150°C

2

LSI Devices

recommended operating conditions

		SN54ALS666 SN54ALS667			SN74ALS666 SN74ALS667			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX		
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
V_{IH}	High-level input voltage	2			2			V	
V_{IL}	Low-level input voltage			0.8			0.8	V	
I_{OH}	High-level output current	Q		-1	D		-2.6	mA	
		D		-0.4	Q		-0.4		
I_{OL}	Load-level output current	Q		12	D		24	mA	
		D		4	Q		8		
t_w	Pulse duration	Enable C high		15	CLR low		10	ns	
		$\overline{\text{CLR}}$ low		10	PRE low		10		
		PRE low		10					
t_{su}	Setup time	Data before $\text{C}\downarrow$		15	Data before $\overline{\text{OERB}}\downarrow$		10	ns	
		Data before $\overline{\text{OERB}}\downarrow$		15					
t_h	Hold time	Data after $\text{C}\downarrow$		10			5	ns	
T_A	Operating free-air temperature			-55	125		0	70	°C

SN54ALS666, SN54ALS667, SN74ALS666, SN74ALS667

8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS666 SN54ALS667		SN74ALS666 SN74ALS667		UNIT		
		MIN	TYP† MAX	MIN	TYP† MAX			
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA	-1.2		-1.2		V		
V _{OH}	All outputs	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA		V _{CC} -2		V		
	Q or \bar{Q}	V _{CC} = 4.5 V, I _{OH} = -1 mA	2.4	3.3	V _{CC} -2			
		V _{CC} = 4.5 V, I _{OH} = -2.6 mA			2.4		3.2	
V _{OL}	D	V _{CC} = 4.5 V, I _{OL} = 4 mA	0.25	0.4	0.25	0.4	V	
		V _{CC} = 4.5 V, I _{OL} = 8 mA			0.35	0.5		
	Q or \bar{Q}	V _{CC} = 4.5 V, I _{OL} = 12 mA	0.25	0.4	0.25	0.4		
		V _{CC} = 4.5 V, I _{OL} = 24 mA			0.35	0.5		
						0.35		0.5
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V	20		20		μA		
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.4 V	-20		-20				
I _I	D inputs	V _{CC} = 5.5 V, V _I = 5.5 V	0.1		0.1		mA	
	All others	V _{CC} = 5.5 V, V = 7 V	0.1		0.1			
I _{IH}	D inputs‡	V _{CC} = 5.5 V, V = 2.7 V	20		20		μA	
	All others		20		20			
I _{IL}	D inputs‡	V _{CC} = 5.5 V, V _I = 0.4 V	-0.1		-0.1		mA	
	All others		-0.1		-0.1			
I _O [§]	V _{CC} = 5.5 V, V _O = 2.25 V	-30	-112	-30	-112	mA		
I _{CC}	'ALS666	V _{CC} = 5.5 V, $\bar{O}ERB$ high	Q outputs high	25	50	25	50	mA
			Q outputs low	40	73	40	73	
			Q outputs disabled	30	55	30	55	
			\bar{Q} outputs high	25	50	25	50	
			\bar{Q} outputs low	45	79	45	79	
			\bar{Q} outputs disabled	30	60	30	60	
	'ALS667							

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit output currents, I_{OS}.

2

LSI Devices

SN54ALS666, SN54ALS667, SN74ALS666, SN74ALS667
8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES
WITH 3-STATE OUTPUTS

***ALS666 switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, T _A = 25 °C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, T _A = MIN to MAX				UNIT
			*ALS666			SN54ALS666		SN74ALS666		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	D	Q		7	10	3	18	3	14	ns
t _{PHL}			11	15	4	22	4	18		
t _{PLH}	C	Q		12	16	6	25	6	21	ns
t _{PHL}			16	21	8	32	8	27		
t _{PHL}	CLR	Q		17	22	9	32	9	29	ns
t _{PHL}		D		17	24	11	36	11	32	
t _{PLH}	PRE	Q		13	18	7	28	7	22	ns
t _{PHL}		D		17	22	9	35	9	28	
t _{en}	OERB	D		11	17	4	25	4	21	ns
t _{dis}				6	11	1	18	1	14	
t _{en}	OE1, OE2	Q		11	17	4	25	4	21	ns
t _{dis}				6	11	1	18	1	14	

***ALS667 switching characteristics (see Figure 1)**

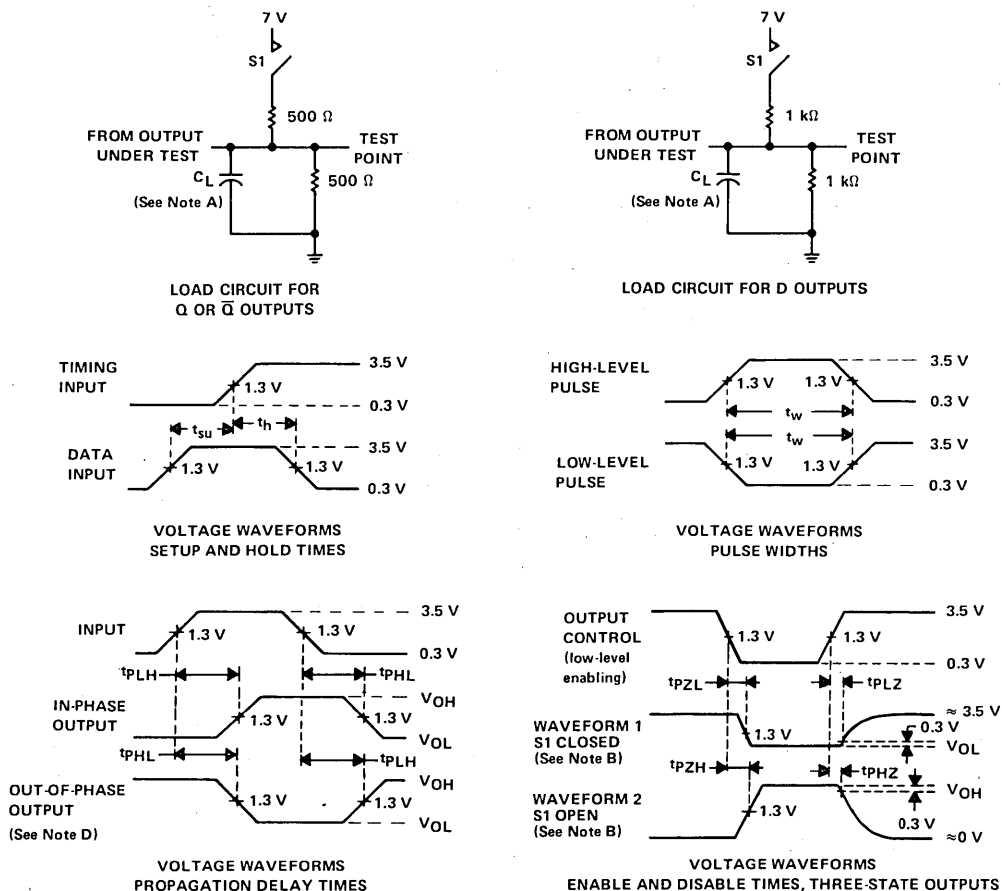
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, T _A = 25 °C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, T _A = MIN to MAX				UNIT
			*ALS667			SN54ALS667		SN74ALS667		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	D	Q̄		13	17	6	24	6	20	ns
t _{PHL}			9	13	4	18	4	15		
t _{PLH}	C	Q̄		18	23	9	35	9	28	ns
t _{PHL}			14	19	7	27	7	22		
t _{PLH}	CLR	Q̄		14	19	7	28	7	24	ns
t _{PHL}		D		17	23	8	30	8	26	
t _{PHL}	PRE	Q̄		17	23	8	30	8	25	ns
t _{PLH}		D		18	25	9	35	9	28	
t _{en}	OERB	D		11	17	4	25	4	21	ns
t _{dis}				6	11	1	20	1	14	
t _{en}	OE1, OE2	Q̄		11	17	4	25	4	21	ns
t _{dis}				6	11	1	20	1	14	

t_{en} = t_{PZH} or t_{PZL}
t_{dis} = t_{PHZ} or t_{PLZ}

SN54ALS666, SN54ALS667, SN74ALS666, SN74ALS667

8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES WITH 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses have the following characteristics: $PRR \leq 1 \text{ MHz}$, $t_r = t_f = 2 \text{ ns}$, duty cycle = 50%.
 D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

FIGURE 1

2
LSI Devices

2

LSI Devices

SN54AS821, SN54AS822, SN74AS821, SN74AS822 10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

D2825, DECEMBER 1983—REVISED JANUARY 1986

- Functionally Equivalent to AMD's AM29821 and AM29822
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- Outputs Have Undershoot Protection Circuitry
- Power-Up High-Impedance State
- Package Options Include Both Plastic and Ceramic Carriers in Addition to Plastic and Ceramic DIPs
- Buffered Control Inputs to Reduce DC Loading Effects
- Dependable Texas Instruments Quality and Reliability

description

These 10-bit flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

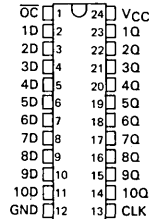
The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock the Q outputs on the 'AS821 will be true, and on the 'AS822 will be complementary to the data input.

A buffered output-control input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control (OC) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AS' family is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AS' family is characterized for operation from 0°C to 70°C .

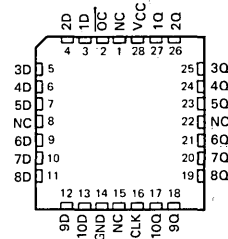
SN54AS821 . . . JT PACKAGE
SN74AS821 . . . DW OR NT PACKAGE

(TOP VIEW)



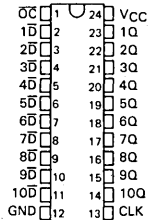
SN54AS821 . . . FK PACKAGE
SN74AS821 . . . FN PACKAGE

(TOP VIEW)



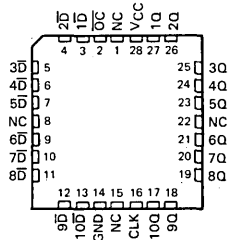
SN54AS822 . . . JT PACKAGE
SN74AS822 . . . DW OR NT PACKAGE

(TOP VIEW)



SN54AS822 . . . FK PACKAGE
SN74AS822 . . . FN PACKAGE

(TOP VIEW)



NC—No internal connection

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LSI Devices

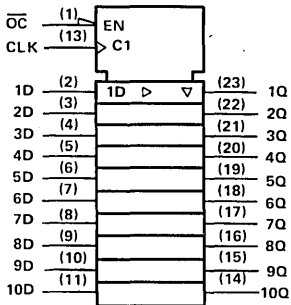
SN54AS821, SN74AS821

10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

'AS821 FUNCTION TABLE (EACH FLIP-FLOP)

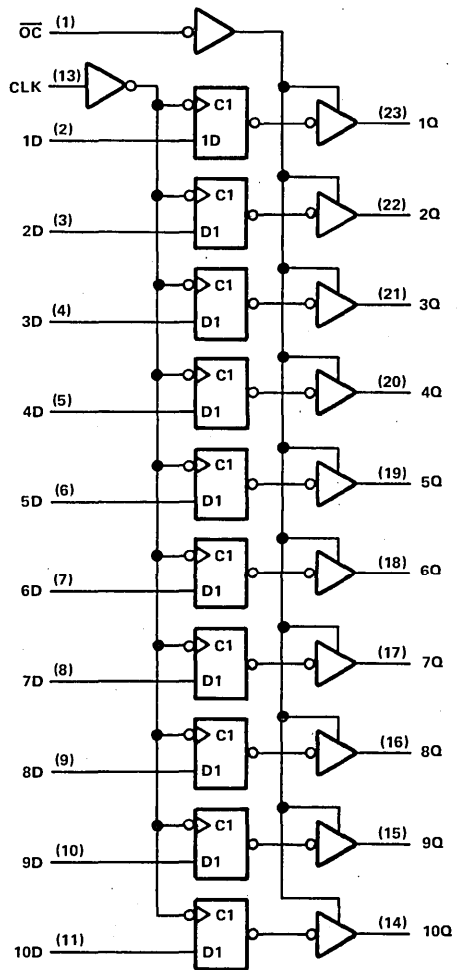
INPUTS			OUTPUT
\overline{OC}	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

'AS821 logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'AS821 logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

2

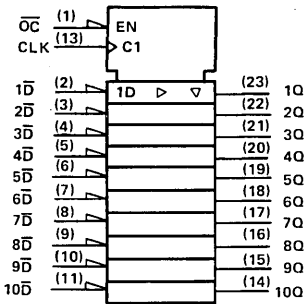
LSI Devices

SN54AS822, SN74AS822 10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

'AS822 FUNCTION TABLE (EACH FLIP-FLOP)

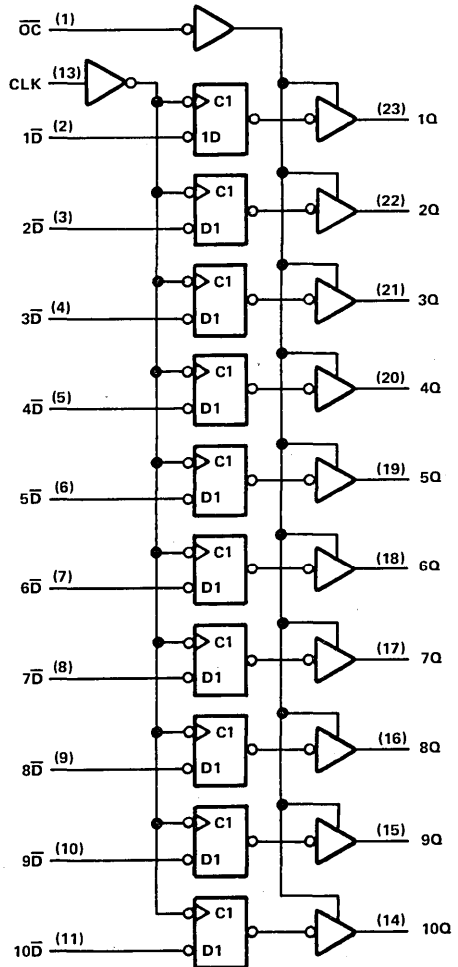
INPUTS			OUTPUT
\overline{OC}	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

'AS822 logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'AS822 logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

2
LSI Devices

SN54AS821, SN54AS822, SN74AS821, SN74AS822

10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range: SN54AS821, SN54AS822	-55°C to 125°C
SN74AS821, SN74AS822	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54AS821 SN54AS822			SN74AS821 SN74AS822			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-24			-24	mA
I_{OL}	Low-level output current			32			48	mA
t_w	Pulse duration, CLK high or low	9			8			ns
t_{su}	Setup time, data before CLK↑	7			6			ns
t_h	Hold time, data after CLK↑	0			0			ns
T_A	Operating free-air temperature	-55	125	-	0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS821 SN54AS822			SN74AS821 SN74AS822			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5 V, I_I = -18 mA$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 4.5 V \text{ to } 5.5 V, I_{OH} = -2 mA$	$V_{CC}-2$			$V_{CC}-2$			V
	$V_{CC} = 4.5 V, I_{OH} = -15 mA$	2.4	3.2		2.4	3.2		
	$V_{CC} = 4.5 V, I_{OH} = -24 mA$	2			2			
V_{OL}	$V_{CC} = 4.5 V, I_{OL} = 32 mA$	0.25	0.5					V
	$V_{CC} = 4.5 V, I_{OL} = 48 mA$				0.35	0.5		
I_{OZH}	$V_{CC} = 5.5 V, V_O = 2.7 V$			50			50	μA
I_{OZL}	$V_{CC} = 5.5 V, V_O = 0.4 V$			-50			-50	μA
I_I	$V_{CC} = 5.5 V, V_I = 7 V$			0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5 V, V_I = 2.7 V$			20			20	μA
I_{IL}	$V_{CC} = 5.5 V, V_I = 0.4 V$			-0.5			-0.5	mA
I_O^{\ddagger}	$V_{CC} = 5.5 V, V_O = 2.25 V$	-30		-112	-30		-112	mA
I_{CC}	$V_{CC} = 5.5 V$		Outputs high	55	88	55	88	mA
			Outputs low	68	109	68	109	
			Outputs disabled	70	113	70	113	
			Outputs high	55	88	55	88	
			Outputs low	68	109	68	109	
			Outputs disabled	70	113	70	113	

†All typical values are at $V_{CC} = 5 V, T_A = 25^\circ C$.

‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

2

LSI Devices

SN54AS821, SN54AS822, SN74AS821, SN74AS822

10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_1 = 500 \Omega,$ $R_2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54AS821 SN54AS822		SN74AS821 SN74AS822		
			MIN	MAX	MIN	MAX	
t_{PLH}	CLK	Any Q	3.5	9	3.5	7.5	ns
t_{PHL}			3.5	11.5	3.5	10.5	
t_{PZH}	\overline{OC}	Any Q	4	12	4	11	ns
t_{PZL}			4	13	4	12	
t_{PHZ}	\overline{OC}	Any Q	2	10	2	8	ns
t_{PZL}			2	10	2	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

2

LSI Devices

2

LSI Devices

SN54AS823, SN54AS824 SN74AS823, SN74AS824 9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

D2825, JUNE 1984—REVISED JANUARY 1986

- Functionally Equivalent to AMD's AM29823 and AM29824
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- Outputs Have Undershoot Protection Circuitry
- Power-Up High-Impedance State
- Buffered Control Inputs to Reduce DC Loading Effects
- Package Options Include both Plastic and Ceramic Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

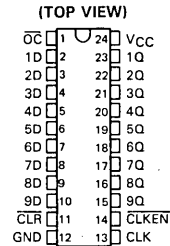
description

These 9-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing and working registers.

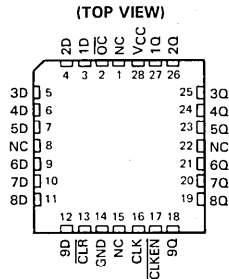
With the clock enable ($\overline{\text{CLKEN}}$) low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{\text{CLKEN}}$ high will disable the clock buffer, thus latching the outputs. The 'AS823 has noninverting D inputs and the 'AS824 has inverting D inputs. Taking the $\overline{\text{CLR}}$ input low causes the nine Q outputs to go low independently of the clock.

A buffered output-control input ($\overline{\text{OC}}$) can be used to place the nine outputs in either normal logic state (high or low level) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

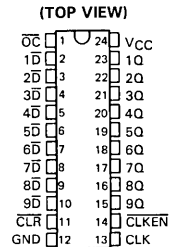
SN54AS823 . . . JT PACKAGE
SN74AS823 . . . DW OR NT PACKAGE



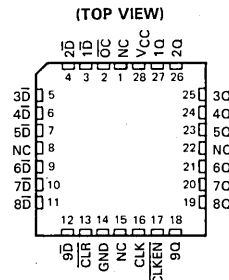
SN54AS823 . . . FK PACKAGE
SN74AS823 . . . FN PACKAGE



SN54AS824 . . . JT PACKAGE
SN74AS824 . . . DW OR NT PACKAGE



SN54AS824 . . . FK PACKAGE
SN74AS824 . . . FN PACKAGE



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SN54AS823, SN54AS824, SN74AS823, SN74AS824

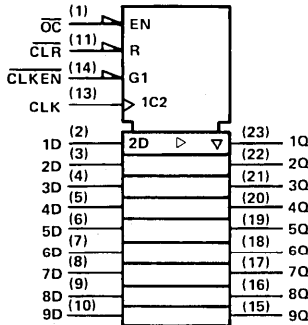
9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

The SN54AS' family is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AS' family is characterized for operation from 0°C to 70°C .

'AS823 FUNCTION TABLE

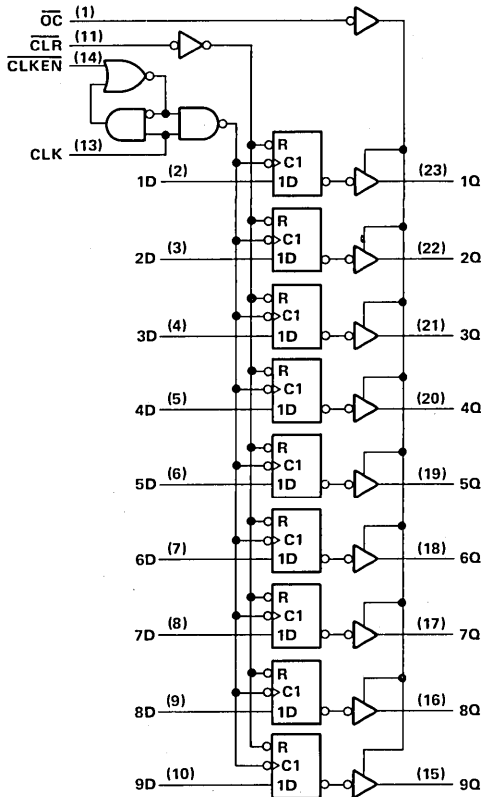
INPUTS					OUTPUT
$\overline{\text{OC}}$	$\overline{\text{CLR}}$	$\overline{\text{CLKEN}}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

'AS823 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

'AS823 logic diagram (positive logic)



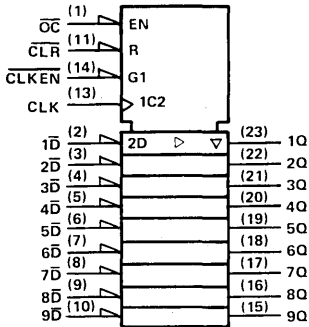
Pin numbers shown are for DW, JT, and NT packages.

SN54AS824, SN74AS824 9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

'AS824 FUNCTION TABLE

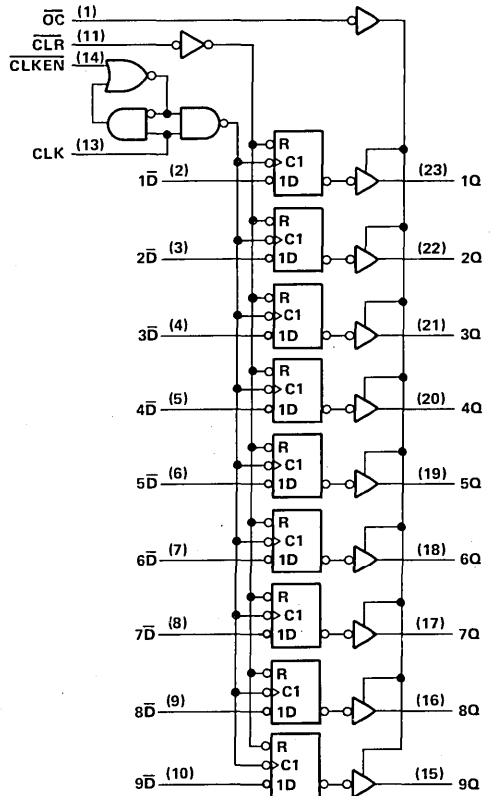
INPUTS					OUTPUT
\overline{OC}	\overline{CLR}	\overline{CLKEN}	CLK	\overline{D}	Q
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	Q_0
H	X	X	X	X	Z

'AS824 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'AS824 logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

2

LSI Devices

SN54AS823, SN54AS824, SN74AS823, SN74AS824

9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range: SN54AS823, SN54AS824	-55°C to 125°C
SN74AS823, SN74AS824	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

	SN54AS823 SN54AS824			SN74AS823 SN74AS824			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			-24			-24	mA
I_{OL} Low-level output current			32			48	mA
t_w Pulse duration	CLR low	5		4			ns
	CLK high or low	9		8			
t_{su} Setup time before CLK†	CLR inactive	8		8			ns
	Data	7		6			
	CLKEN high or low	7		6			
t_h Hold time, \overline{CLKEN} or data after CLK†		0		0			ns
T_A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS823 SN54AS824			SN74AS823 SN74AS824			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5$ V, $I_I = -18$ mA			-1.2			-1.2	V
V_{OH}	$V_{CC} = 4.5$ V to 5.5 V, $I_{OH} = -2$ mA	$V_{CC}-2$			$V_{CC}-2$			V
	$V_{CC} = 4.5$ V, $I_{OH} = -15$ mA	2.4	3.2		2.4	3.2		
	$V_{CC} = 4.5$ V, $I_{OH} = -24$ mA	2			2			
V_{OL}	$V_{CC} = 4.5$ V, $I_{OL} = 32$ mA		0.3	0.5				V
	$V_{CC} = 4.5$ V, $I_{OL} = 48$ mA				0.35	0.5		
I_{OZH}	$V_{CC} = 5.5$ V, $V_O = 2.7$ V			50			50	μA
I_{OZL}	$V_{CC} = 5.5$ V, $V_O = 0.4$ V			-50			-50	μA
I_I	$V_{CC} = 5.5$ V, $V_I = 7$ V			0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5$ V, $V_I = 2.7$ V			20			20	μA
I_{IL}	$V_{CC} = 5.5$ V, $V_I = 0.4$ V			-0.5			-0.5	mA
I_O^{\ddagger}	$V_{CC} = 5.5$ V, $V_O = 2.25$ V	-30		-112	-30		-112	mA
I_{CC}	'AS823	$V_{CC} = 5.5$ V	Outputs high	49	80	49	80	mA
			Outputs low	61	100	61	100	
			Outputs disabled	64	103	64	103	
	'AS824	$V_{CC} = 5.5$ V	Outputs high	49	80	49	80	mA
			Outputs low	61	100	61	100	
			Outputs disabled	64	103	64	103	

† All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

SN54AS823, SN54AS824, SN74AS823, SN74AS824

9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$ $C_L = 50 \text{ pF,}$ $R_1 = 500 \Omega,$ $R_2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54AS823 SN54AS824		SN74AS823 SN74AS824		
			MIN	MAX	MIN	MAX	
t_{PLH}	CLK	Any Q	3.5	9	3.5	7.5	ns
t_{PHL}			3.5	12	3.5	11	
t_{PHL}	$\overline{\text{CLR}}$	Any Q	3.5	14	3.5	13	ns
t_{PZH}	$\overline{\text{OC}}$	Any Q	4	12	4	11	ns
t_{PZL}			4	13	4	12	
t_{PHZ}	$\overline{\text{OC}}$	Any Q	2	10	2	8	ns
t_{PLZ}			2	10	2	8	

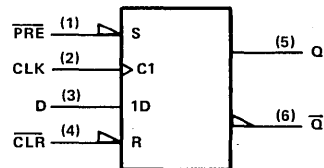
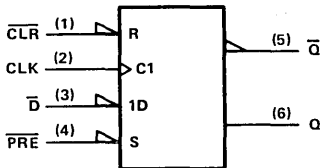
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D flip-flop signal conventions

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called \overline{Q} . An input that causes a Q output to go high or a \overline{Q} output to go low is called Preset; an input that causes a Q output to go high or a \overline{Q} output to go low is called Clear. Bars are used over these pin names (PRE and CLR) if they are active-low.

The devices on this data sheet are second-source designs and the pin-name convention used by the original manufacturer has been retained. That makes it necessary to designate the inputs and outputs of the inverting circuit D and \overline{Q} . In some applications it may be advantageous to redesignate the inputs and outputs as D and Q. In that case, outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.

Notice that Q and \overline{Q} exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (∇) on PRE and CLR remain since these inputs are still active-low, but that the presence or absence of the polarity changes at D, Q, and \overline{Q} . Of course pin 5 (Q) is still in phase with the data input D, but now both are considered active high.



2

LSI Devices

SN54AS825, SN54AS826 SN74AS825, SN74AS826 8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

D2825, JUNE 1984—REVISED JANUARY 1986

- Functionally Equivalent to AMD's AM29825 and AM29826
- Improved IOH Specifications
- Multiple Output Enables Allow Multiuser Control of the Interface
- Outputs Have Undershoot Protection Circuitry
- Power-Up High-Impedance State
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Buffered Control Inputs to Reduce DC Loading Effect
- Dependable Texas Instruments Quality and Reliability

description

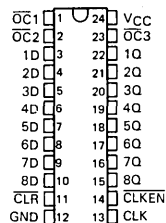
These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing multiuser registers, I/O ports, bidirectional bus drivers, and working registers.

With the clock enable ($\overline{\text{CLKEN}}$) low, the eight D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{\text{CLKEN}}$ high will disable the clock buffer, thus latching the outputs. The 'AS825 has non-inverting D inputs and the 'AS826 has inverting D inputs. Taking the $\overline{\text{CLR}}$ input low causes the eight Q outputs to go low independently of the clock.

Multiuser buffered output-control inputs ($\overline{\text{OC1}}$, $\overline{\text{OC2}}$, and $\overline{\text{OC3}}$) can be used to place the eight outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

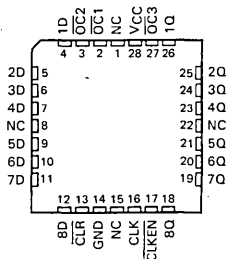
SN54AS825 . . . JT PACKAGE
SN74AS825 . . . DW OR NT PACKAGE

(TOP VIEW)



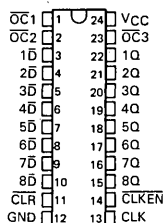
SN54AS825 . . . FK PACKAGE
SN74AS825 . . . FN PACKAGE

(TOP VIEW)



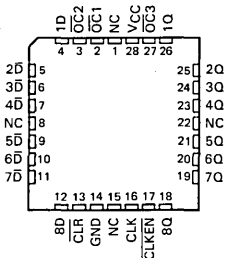
SN54AS826 . . . JT PACKAGE
SN74AS826 . . . DW OR NT PACKAGE

(TOP VIEW)



SN54AS826 . . . FK PACKAGE
SN74AS826 . . . FN PACKAGE

(TOP VIEW)



NC—No internal connection

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2
LSI Devices

SN54AS825, SN54AS826, SN74AS825, SN74AS826

8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

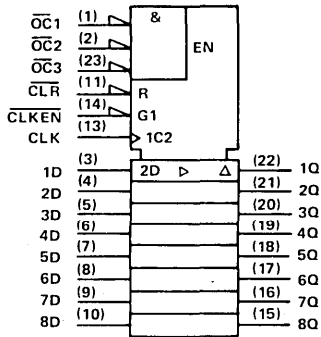
The SN54AS' family is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AS' family is characterized for operation from 0°C to 70°C .

'AS825 FUNCTION TABLE

INPUTS					OUTPUT
$\overline{\text{OC}}^*$	CLR	CLKEN	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

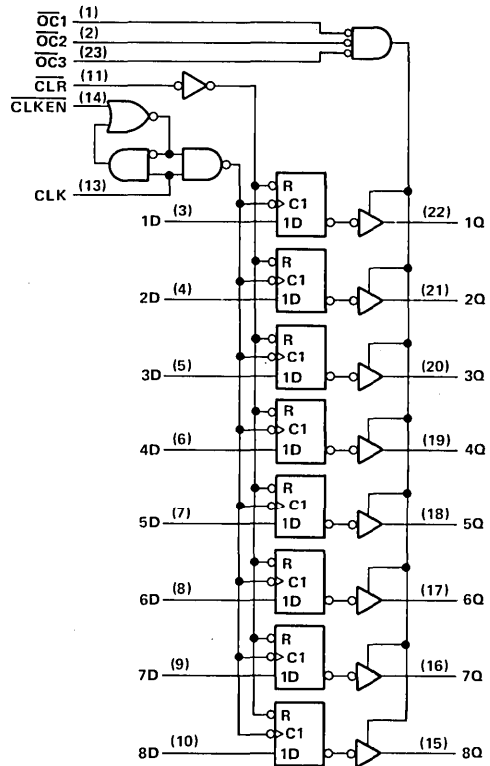
$\overline{\text{OC}}^* = \text{H}$ if any of $\overline{\text{OC}}1$, $\overline{\text{OC}}2$, or $\overline{\text{OC}}3$ are high.
 $\overline{\text{OC}}^* = \text{L}$ if all of $\overline{\text{OC}}1$, $\overline{\text{OC}}2$, and $\overline{\text{OC}}3$ are low.

'AS825 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'AS825 logic diagram (positive logic)



Pin numbers are for DW, JT, and NT packages.

SN54AS826, SN74AS826 8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

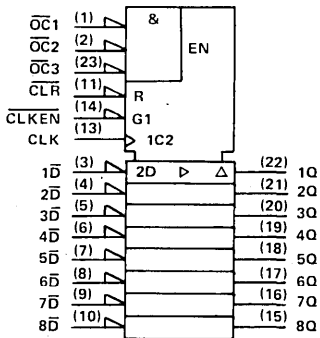
*AS826 FUNCTION TABLE

INPUTS					OUTPUT
\overline{OC}^*	CLR	CLKEN	CLK	\overline{D}	Q
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	Q_0
H	X	X	X	X	Z

$\overline{OC}^* = H$ if any of $\overline{OC}1$, $\overline{OC}2$, or $\overline{OC}3$ are high.

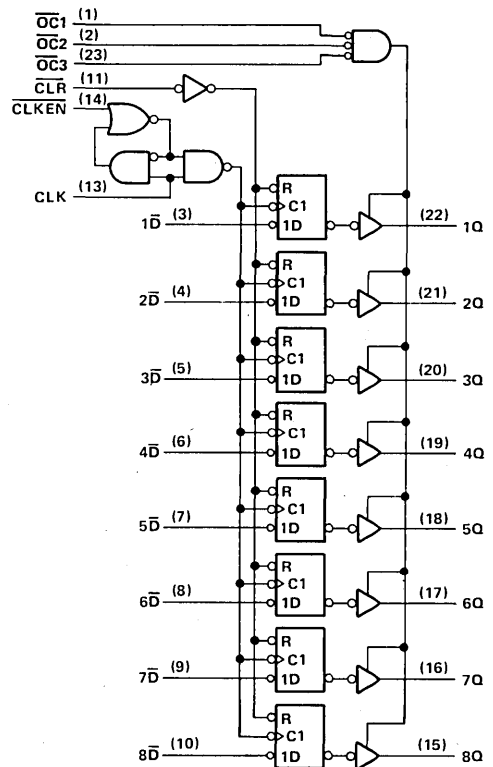
$\overline{OC}^* = L$ if all of $\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$ are low.

*AS826 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

*AS826 logic diagram (positive logic)



2

LSI Devices

Pin numbers shown are for DW, JT, and NT packages.

SN54AS825, SN54AS826, SN74AS825, SN74AS826

8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range:	
SN54AS825, SN54AS826	-55°C to 125°C
SN74AS825, SN74AS826	0°C to 70°C
Storage temperature range	-65 to 150°C

recommended operating conditions

		SN54AS825 SN54AS826			SN74AS825 SN74AS826			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-24			-24	mA
I_{OL}	Low-level output current			32			48	mA
t_w	Pulse duration	CLR low	5		4			ns
		CLK high or low	9		8			
t_{su}	Setup time before CLK†	CLR inactive	8		8			ns
		Data	7		6			
		CLKEN high or low	7		6			
t_h	Hold time, CLKEN or data after CLK†	0			0			ns
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS825 SN54AS826			SN74AS825 SN74AS826			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5 V, I_I = -18 mA$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 4.5 V$ to 5.5 V, $I_{OH} = -2 mA$	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5 V, I_{OH} = -15 mA$	2.4	3.2		2.4	3.2		
	$V_{CC} = 4.5 V, I_{OH} = -24 mA$	2			2			
V_{OL}	$V_{CC} = 4.5 V, I_{OL} = 32 mA$		0.3	0.5				V
	$V_{CC} = 4.5 V, I_{OL} = 48 mA$				0.35	0.5		
I_{OZH}	$V_{CC} = 5.5 V, V_O = 2.7 V$			50			50	µA
I_{OZL}	$V_{CC} = 5.5 V, V_O = 0.4 V$			-50			-50	µA
I_I	$V_{CC} = 5.5 V, V_I = 7 V$			0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5 V, V_I = 2.7 V$			20			20	µA
I_{IL}	$V_{CC} = 5.5 V, V_I = 0.4 V$			-0.5			-0.5	mA
I_O^\ddagger	$V_{CC} = 5.5 V, V_O = 2.25 V$	-30		-112	-30		-112	mA
I_{CC}	'AS825	$V_{CC} = 5.5 V$	Outputs high	45	73	45	73	mA
			Outputs low	56	90	56	90	
			Outputs disabled	59	95	59	95	
	'AS826	$V_{CC} = 5.5 V$	Outputs high	45	73	45	73	mA
			Outputs low	56	90	56	90	
			Outputs disabled	59	95	59	95	

† All typical values are at $V_{CC} = 5 V, T_A = 25^\circ C$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

SN54AS825, SN54AS826, SN74AS825, SN74AS826

8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$ $C_L = 50 \text{ pF,}$ $R_1 = 500 \Omega,$ $R_2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54AS825		SN74AS825		
			MIN	MAX	MIN	MAX	
t_{PLH}	CLK	Any Q	3.5	9	3.5	7.5	ns
t_{PHL}			3.5	11.5	3.5	11	
t_{PHL}	$\overline{\text{CLR}}$	Any Q	3.5	14	3.5	13	ns
t_{PZH}	$\overline{\text{OC}}$	Any Q	4	12	4	11	ns
t_{PZL}			4	13	4	12	
t_{PHZ}	$\overline{\text{OC}}$	Any Q	2	10	2	8	ns
t_{PLZ}			2	10	2	8	

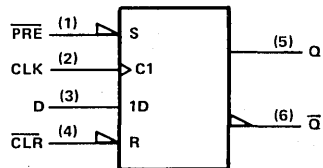
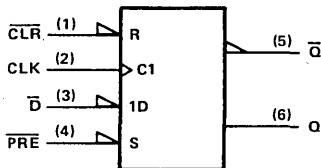
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D flip-flop signal conventions

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called \overline{Q} . An input that causes a Q output to go high or a \overline{Q} output to go low is called Preset; an input that causes a \overline{Q} output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{\text{PRE}}$ and $\overline{\text{CLR}}$) if they are active-low.

The devices on this data sheet are second-source designs and the pin-name convention used by the original manufacturer has been retained. That makes it necessary to designate the inputs and outputs of the inverting circuit \overline{D} and Q. In some applications it may be advantageous to redesignate the inputs and outputs as D and \overline{Q} . In that case, outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.

Notice that Q and \overline{Q} exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (∇) on $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at \overline{D} , Q, and \overline{Q} . Of course pin 5 (Q) is still in phase with the data input D, but now both are considered active high.



2
LSI Devices

2

LSI Devices

SN54ALS841, SN54AS841, SN54ALS842, SN54AS842 SN74ALS841, SN74AS841, SN74ALS842, SN74AS842 10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

D2910, DECEMBER 1983—REVISED OCTOBER 1985

- 3-State Buffer-Type Outputs Drive Bus-Lines Directly
- Bus-Structured Pinout
- Provide Extra Bus Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity
- Buffered Control Inputs to Reduce DC Loading
- Power-Up High-Impedance State
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 10-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The ten latches are transparent D-type. The 'ALS841 and 'AS841 have noninverting data (D) inputs. The 'ALS842 and 'AS842 have inverting D inputs.

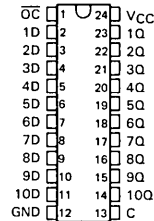
A buffered output control (\overline{OC}) input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

The -1 versions of the SN74ALS841 and SN74ALS842 parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS841 and SN54ALS842.

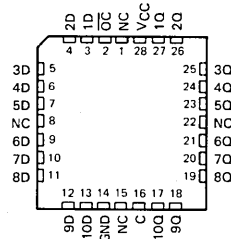
SN54ALS841, SN54AS841 . . . JT PACKAGE
SN74ALS841, SN74AS841 . . . DW OR NT PACKAGE

(TOP VIEW)



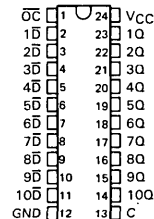
SN54ALS842, SN54AS842 . . . FK PACKAGE
SN74ALS842, SN74AS842 . . . FN PACKAGE

(TOP VIEW)



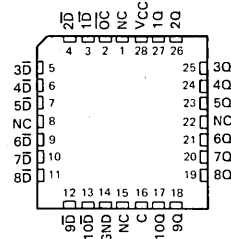
SN54ALS842, SN54AS842 . . . JT PACKAGE
SN74ALS842, SN74AS842 . . . DW OR NT PACKAGE

(TOP VIEW)



SN54ALS842, SN54AS842 . . . FK PACKAGE
SN74ALS842, SN74AS842 . . . FN PACKAGE

(TOP VIEW)



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SN54ALS841, SN54AS841, SN54ALS842, SN54AS842 SN74ALS841, SN74AS841, SN74ALS842, SN74AS842 10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

The SN54ALS841, SN54AS841, SN54ALS842, and SN54AS842 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS841, SN74AS841, SN74ALS842, and SN74AS842 are characterized for operation from 0°C to 70°C .

FUNCTION TABLES

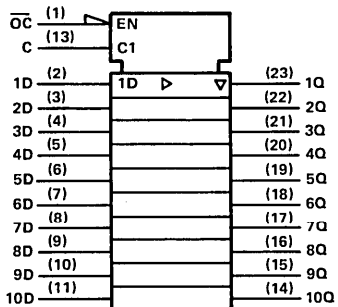
'ALS841, 'AS841

INPUTS			OUTPUT
$\overline{\text{OC}}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

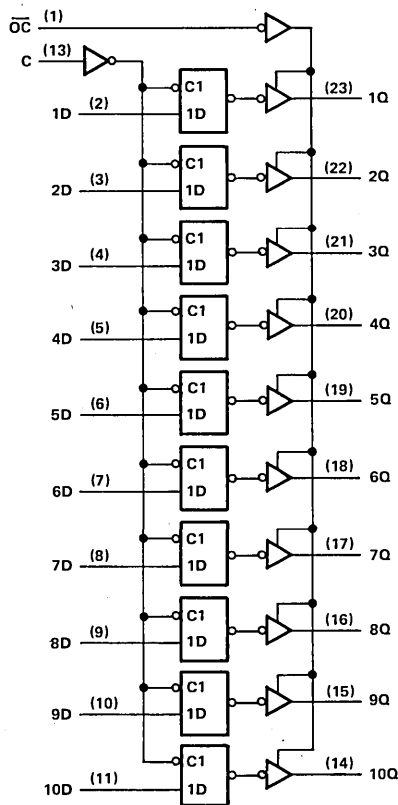
'ALS842, 'AS842

INPUTS			OUTPUT
$\overline{\text{OC}}$	C	$\overline{\text{D}}$	Q
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

'ALS841, 'AS841 logic symbol†



'ALS841, 'AS841 logic diagram (positive logic)

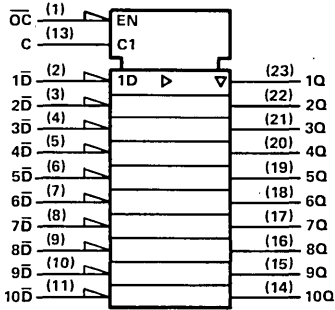


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

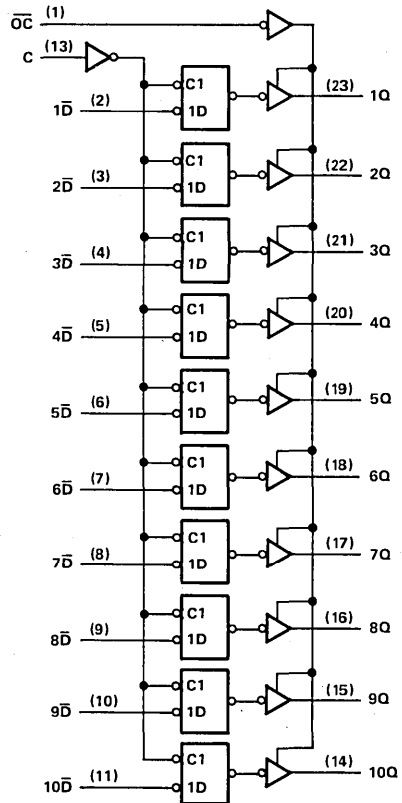
Pin numbers shown are for DW, JT, and NT packages.

**SN54ALS841, SN54AS841, SN54ALS842, SN54AS842
SN74ALS841, SN74AS841, SN74ALS842, SN74AS842
10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS**

'ALS842, 'AS842 logic symbol†



'ALS842, 'AS842 logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range:	
SN54ALS841, SN54AS841, SN54ALS842, SN54AS842	-55°C to 125°C
SN74ALS841, SN74AS841, SN74ALS842, SN74AS842	0°C to 70°C
Storage temperature range	-65°C to 150°C

SN54ALS841, SN74ALS841

10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

recommended operating conditions

		SN54ALS841			SN74ALS841			UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX			
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V		
V _{IH}	High-level input voltage	2			2			V		
V _{IL}	Low-level input voltage	0.8			0.8			V		
I _{OH}	High-level output current	-1			-2.6			mA		
I _{OL}	Low-level output current	12			24			mA		
					48 [†]					
t _w	Pulse duration, enable C high	25			20			ns		
t _{su}	Setup time, data before enable C↓	16			10			ns		
t _h	Hold time, data after enable C↓	7			5			ns		
T _A	Operating free-air temperature	-55			125			0	70	°C

[†] The extended limit applies only if V_{CC} is maintained between 4.75 V and 5.25 V. The 48 mA limit applies for SN74ALS841-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS841			SN74ALS841			UNIT	
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX		
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA	-1.2			-1.2			V	
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA	V _{CC} - 2			V _{CC} - 2			V	
	V _{CC} = 4.5 V, I _{OH} = -1 mA	2.4	3.3						
	V _{CC} = 4.5 V, I _{OH} = -2.6 mA				2.4	3.2			
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 12 mA	0.25			0.25			V	
	V _{CC} = 4.5 V, I _{OL} = 24 mA (I _{OL} = 48 mA for -1 versions)				0.35				
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V	20			20			μA	
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.4	-20			-20			μA	
I _I	V _{CC} = 5.5 V, V _I = 7 V	0.1			0.1			mA	
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V	20			20			μA	
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V	-0.1			-0.1			mA	
I _O [§]	V _{CC} = 5.5 V, V _O = 2.25 V	-30	-112		-30	-112		mA	
I _{CC}	V _{CC} = 5.5 V	Outputs high			19			30	mA
		Outputs low			38			62	
		Outputs disabled			23			40	

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54ALS841, SN74ALS841
10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

'ALS841 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX						UNIT
			SN54/74ALS841			SN54ALS841		SN74ALS841				
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	D	Q		8.5	11	2	15	2	13	ns		
t _{PHL}				8.5	11	2	15	2	13			
t _{PLH}	C	Q		14	18	7	25	7	21	ns		
t _{PHL}				17	23	8	30	8	26			
t _{PZH}	\overline{OC}	Q		7.5	10	2	14	2	12	ns		
t _{PZL}				7.5	10	2	14	2	12			
t _{PHZ}	\overline{OC}	Q		6	8	2	12	2	10	ns		
t _{PLZ}				7	9	2	14	2	12			

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS842, SN74ALS842

10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

recommended operating conditions

		SN54ALS842			SN74ALS842			UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX			
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V		
V _{IH}	High-level input voltage	2			2			V		
V _{IL}	Low-level input voltage				0.8			V		
I _{OH}	High-level output current				-1			-2.6	mA	
I _{OL}	Low-level output current				12			24	mA	
								48 [†]		
t _w	Pulse duration, enable C high	25			20			ns		
t _{su}	Setup time, data before enable C↓	16			10			ns		
t _h	Hold time, data after enable C↓	7			5			ns		
T _A	Operating free-air temperature	-55			125			0	70	°C

[†] The extended limit applies only if V_{CC} is maintained between 4.75 V and 5.25 V. The 48 mA limit applies for SN74ALS841-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS842			SN74ALS842			UNIT	
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX		
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA	-1.2			-1.2			V	
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA	V _{CC} - 2			V _{CC} - 2			V	
	V _{CC} = 4.5 V, I _{OH} = -1 mA	2.4	3.3						
	V _{CC} = 4.5 V, I _{OH} = -2.6 mA				2.4	3.2			
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 12 mA	0.25			0.4			V	
	V _{CC} = 4.5 V, I _{OL} = 24 mA (I _{OL} = 48 mA for -1 versions)				0.35				
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V				20			μA	
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.4				-20			μA	
I _I	V _{CC} = 5.5 V, V _I = 7 V				0.1			mA	
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V				20			μA	
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V				-0.1			mA	
I _{O[§]}	V _{CC} = 5.5 V, V _O = 2.25 V	-30	-112		-30	-112		mA	
I _{CC}	V _{CC} = 5.5 V	Outputs high		20	35		20	35	mA
		Outputs low		48	74		48	74	
		Outputs disabled		27	44		27	44	

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{O[§]}.

SN54ALS842, SN74ALS842
10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

'ALS842 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX			UNIT	
			'ALS842			SN54ALS842		SN74ALS842		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
t _{PLH}	D̄	Q	11	15	4	22	4	18	ns	
t _{PHL}			8	11	3	17	3	13		
t _{PLH}	C	Q	17	23	8	31	8	27	ns	
t _{PHL}			13	18	6	24	6	20		
t _{PZH}	OC̄	Q	8	10	2	14	2	12	ns	
t _{PZL}			8	11	2	14	2	12		
t _{PHZ}	OC̄	Q	6	8	1	12	1	10	ns	
t _{PLZ}			7	9	2	14	2	12		

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54AS841, SN54AS842
SN74AS841, SN74AS842
10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

recommended operating conditions

		SN54AS841 SN54AS842			SN74AS841 SN74AS842			UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX			
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V		
V _{IH}	High-level input voltage	2			2			V		
V _{IL}	Low-level input voltage	0.8			0.8			V		
I _{OH}	High-level output current	-24			-24			mA		
I _{OL}	Low-level output current	32			48			mA		
t _w	Pulse duration, enable C high	5			4			ns		
t _{su}	Setup time, data before enable C↑	3.5			2.5			ns		
t _h	Hold time, data after enable C↓	3.5			2.5			ns		
T _A	Operating free-air temperature	-55			125			0	70	°C

electrical characteristics over recommended operating free-air temperature range
(unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS841 SN54AS842			SN74AS841 SN74AS842			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA	-1.2			-1.2			V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -2 mA	V _{CC} -2			V _{CC} -2			V
	V _{CC} = 4.5 V, I _{OH} = -15 mA	2.4	3.2		2.4	3.2		
	V _{CC} = 4.5 V, I _{OH} = -24 mA	2			2			
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 32 mA	0.25			0.5			V
	V _{CC} = 4.5 V, I _{OL} = 48 mA				0.35			
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V	50			50			μA
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.4 V	-50			-50			μA
I _I	V _{CC} = 5.5 V, V _I = 7 V	0.1			0.1			mA
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V	20			20			μA
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V	-0.5			-0.5			mA
I _O ‡	V _{CC} = 5.5 V, V _O = 2.25 V	-30		-112	-30		-112	mA
I _{CC}	V _{CC} = 5.5 V	Outputs high	36	60	36	60	mA	
		Outputs low	58	94	58	94		
		Outputs disabled	56	92	56	92		
		Outputs high	38	62	38	62		
		Outputs low	60	97	60	97		
		Outputs disabled	58	95	58	95		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

'AS841 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$ $C_L = 50 \text{ pF,}$ $R_1 = 500 \Omega,$ $R_2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54AS841		SN74AS841		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1	8.5	1	6.5	ns
t_{PHL}			1	10	1	9	
t_{PLH}	C	Q	2	13	2	12	ns
t_{PHL}			2	13	2	12	
t_{PZH}	\overline{OC}	Q	2	13.5	2	10.5	ns
t_{PZL}			2	15	2	13.5	
t_{PHZ}	\overline{OC}	Q	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

'AS842 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$ $C_L = 50 \text{ pF,}$ $R_1 = 500 \Omega,$ $R_2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54AS842		SN74AS842		
			MIN	MAX	MIN	MAX	
t_{PLH}	\overline{D}	Q	1	11	1	8.5	ns
t_{PHL}			1	10	1	9	
t_{PLH}	C	Q	2	13	2	12	ns
t_{PHL}			2	13	2	12	
t_{PZH}	\overline{OC}	Q	2	14.5	2	12	ns
t_{PZL}			2	15	2	12.5	
t_{PHZ}	\overline{OC}	Q	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS843, SN54AS843, SN54ALS844, SN54AS844 SN74ALS843, SN74AS843, SN74ALS844, SN74AS844 9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

D2910, DECEMBER 1983—REVISED DECEMBER 1985

- 3-State Buffer-Type Outputs Drive Bus-Lines Directly
- Bus-Structured Pinout
- Provide Extra Bus Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity
- Buffered Control Inputs to Reduce DC Loading
- Power-Up High Impedance
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 9-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

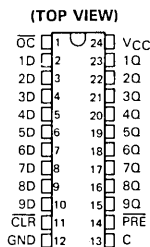
The nine latches are transparent D-type. The 'ALS843 and 'AS843 have noninverting data (D) inputs. The 'ALS844 and 'AS844 have inverting D inputs.

A buffered output control (\overline{OC}) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

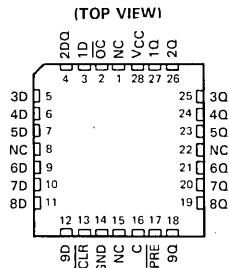
The output control (\overline{OC}) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The -1 versions of the SN74ALS843 and SN74ALS844 parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS843 and SN54ALS844.

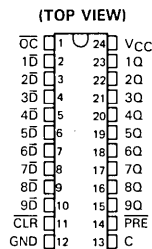
SN54ALS843, SN54AS843 . . . JT PACKAGE
SN74ALS843, SN74AS843 . . . DW OR NT PACKAGE



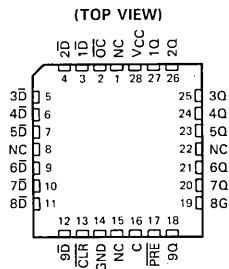
SN54ALS843, SN54AS843 . . . FK PACKAGE
SN74ALS843, SN74AS843 . . . FN PACKAGE



SN54ALS844, SN54AS844 . . . JT PACKAGE
SN74ALS844, SN74AS844 . . . DW OR NT PACKAGE



SN54ALS844, SN54AS844 . . . FK PACKAGE
SN74ALS844, SN74AS844 . . . FN PACKAGE



NC—No internal connection

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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2-173

2
LSI Devices

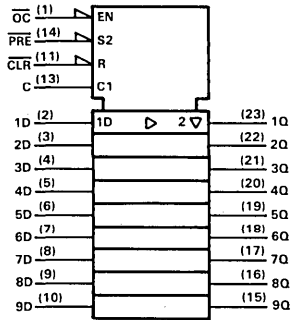
**SN54ALS843, SN54AS843, SN54ALS844, SN54AS844
SN74ALS843, SN74AS843, SN74ALS844, SN74AS844
9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS**

The SN54ALS843, SN54AS843, SN54ALS844, and SN54AS844 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS843, SN74AS843, SN74ALS844, and SN74AS844 are characterized for operation from 0°C to 70°C .

'ALS843, 'AS843 FUNCTION TABLE

INPUTS					OUTPUT
PRE	CLR	OC	C	D	Q
L	X	L	X	X	H [†]
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q _O
X	X	H	X	X	Z

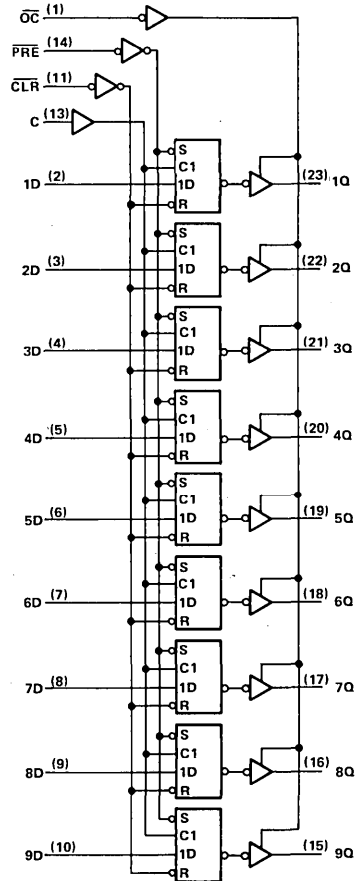
'ALS843, 'AS843 logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

'ALS843, 'AS843 logic diagram (positive logic)

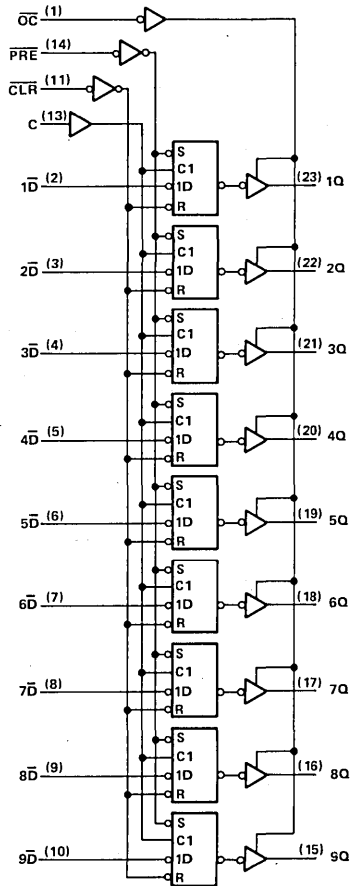


**SN54ALS843, SN54AS843, SN54ALS844, SN54AS844
SN74ALS843, SN74AS843, SN74ALS844, SN74AS844
9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS**

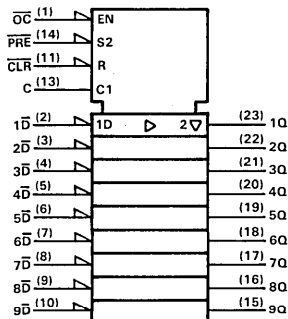
'ALS844, 'AS844 FUNCTION TABLE

INPUTS					OUTPUT
PRE	CLR	OC	C	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	H
H	H	L	H	H	L
H	H	L	L	X	Q _O
X	X	H	X	X	Z

'ALS844, 'AS844 logic diagram (positive logic)



'ALS844, 'AS844 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC}	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range: SN54ALS', SN54AS'	-55°C to 125°C
SN74ALS', SN74AS'	0°C to 70°C
Storage temperature range	-65°C to 150°C

2
LSI Devices

SN54ALS843, SN54ALS844
SN74ALS843, SN74ALS844
9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

recommended operating conditions

			SN54ALS843 SN54ALS844			SN74ALS843 SN74ALS844			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage		0.8			0.8			V
I _{OH}	High-level output current		-1			-2.6			mA
I _{OL}	Low-level output current		12			24			mA
						48 [†]			
t _w	Pulse duration	CLR or PRE low	40			35			ns
		C high	25			20			
t _{su}	Setup time, data before enable C _I		16			10			ns
t _h	Hold time, data after enable C _I		7			5			ns
T _A	Operating free-air temperature		-55			125			°C

[†]The 48-mA limit applies for SN74ALS843-1 and SN74ALS844-1 only and only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ALS843 SN54ALS844		SN74ALS843 SN74ALS844		UNIT
			MIN	TYP [‡]	MAX	MIN	
V _{IK}		V _{CC} = 4.5 V, I _I = -18 mA	-1.2		-1.2		V
V _{OH}		V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA	V _{CC} -2		V _{CC} -2		V
		V _{CC} = 4.5 V, I _{OH} = -1 mA	2.4	3.3			
		V _{CC} = 4.5 V, I _{OH} = -2.6 mA			2.4	3.2	
V _{OL}		V _{CC} = 4.5 V, I _{OL} = 12 mA	0.25	0.4	0.25	0.4	V
		V _{CC} = 4.5 V, I _{OL} = 24 mA					
		(I _{OL} = 48 mA for -1 versions)			0.35	0.5	
I _{OZH}		V _{CC} = 5.5 V, V _O = 2.7 V	20		20		μA
I _{OZL}		V _{CC} = 5.5 V, V _O = 0.4 V	-20		-20		μA
I _I		V _{CC} = 5.5 V, V _I = 7 V	0.1		0.1		mA
I _{IH}		V _{CC} = 5.5 V, V _I = 2.7 V	20		20		μA
I _{IL}		V _{CC} = 5.5 V, V _I = 0.4 V	-0.1		-0.1		mA
I _O [§]		V _{CC} = 5.5 V, V _O = 2.25 V	-30	-112	-30	-112	mA
I _{CC}	'ALS843	Outputs high	21	36	21	36	mA
		Outputs low	41	67	41	67	
		Outputs disabled	25	42	25	42	
	'ALS844	Outputs high	21	36	21	36	
		Outputs low	41	72	41	72	
		Outputs disabled	28	48	28	48	

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54ALS843, SN54ALS844
SN74ALS843, SN74ALS844

9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

'ALS843 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX				UNIT
			'ALS843			SN54ALS843		SN74ALS843		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	D	Q	7	11	2	15	2	13	ns	
t _{PHL}			11	15	4	20	4	18		
t _{PLH}	C	Q	12	18	5	25	5	21	ns	
t _{PHL}			16	23	8	30	8	26		
t _{PLH}	PRE	Q	13	19	5	25	5	22	ns	
t _{PHL}			19	26	4	35	6	30		
t _{PLH}	CLR	Q	19	26	4	35	6	30	ns	
t _{PHL}			14	21	6	27	6	23		
t _{PZH}	OC	Q	7	10	2	14	2	12	ns	
t _{PZL}			9	12	4	16	4	14		
t _{PHZ}	OC	Q	6	9	2	12	2	10	ns	
t _{PLZ}			7	10	2	14	2	12		

'ALS844 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX				UNIT
			'ALS844			SN54ALS844		SN74ALS844		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	D	Q	11	16	4	22	4	20	ns	
t _{PHL}			9	13	3	17	3	15		
t _{PLH}	C	Q	17	24	8	32	8	29	ns	
t _{PHL}			14	19	6	26	6	22		
t _{PLH}	PRE	Q	13	19	5	25	5	22	ns	
t _{PHL}			19	26	4	35	6	30		
t _{PLH}	CLR	Q	19	26	4	35	6	30	ns	
t _{PHL}			16	23	8	29	8	25		
t _{PZH}	OC	Q	10	15	2	19	4	17	ns	
t _{PZL}			12	18	3	22	5	20		
t _{PHZ}	OC	Q	7	10	1	12	1	11	ns	
t _{PLZ}			5	9	1	14	1	12		

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

2
LSI Devices

SN54AS843, SN54AS844
SN74AS843, SN74AS844
9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

recommended operating conditions

		SN54AS843 SN54AS844			SN74AS843 SN74AS844			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage [§]	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage	0.8			0.8			V
I _{OH}	High-level output current	-24			-24			mA
I _{OL}	Low-level output current	32			48			mA
t _w	Pulse duration, enable C high	CLR or PRE low		4			ns	
		C high		4				
t _{SU}	Setup time, data before enable C↓	3.5			2.5			ns
t _H	Hold time, data after enable C↓	3.5			2.5			ns
t _r	Recovery time	PRE		15			ns	
		CLR		14				
T _A	Operating free-air temperature	-55		125		0 70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS843 SN54AS844			SN74AS843 SN74AS844			UNIT
			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
V _{IK}	V _{CC} = 4.5 V,	I _I = -18 mA	-1.2			-1.2			V
V _{OH}	V _{CC} = 4.5 V,	I _{OH} = -2 mA	V _{CC} -2			V _{CC} -2			V
	V _{CC} = 4.5 V,	I _{OH} = -15 mA	2.4	3.2		2.4	3.2		
	V _{CC} = 4.5 V,	I _{OH} = -24 mA	2			2			
V _{OL}	V _{CC} = 4.5 V,	I _{OL} = 32 mA	0.25		0.5				V
	V _{CC} = 4.5 V,	I _{OL} = 48 mA				0.35	0.5		
I _{OZH}	V _{CC} = 5.5 V,	V _O = 2.7 V	50			50			μA
I _{OZL}	V _{CC} = 5.5 V,	V _O = 0.4 V	-50			-50			μA
I _I	V _{CC} = 5.5 V,	V _I = 7 V	0.1			0.1			mA
I _{IH}	V _{CC} = 5.5 V,	V _I = 2.7 V	20			20			μA
I _{IL}	V _{CC} = 5.5 V,	V _I = 0.4 V	-0.5			-0.5			mA
I _O [‡]	V _{CC} = 5.5 V,	V _O = 2.25 V	-30		-112	-30		-112	mA
I _{CC}	'AS843	V _{CC} = 5.5 V,	Outputs high		37	62	37	62	mA
			Outputs low		56	92	56	92	
			Outputs disabled		56	92	56	92	
	'AS844		Outputs high		39	64	39	64	
			Outputs low		58	95	58	95	
			Outputs disabled		58	95	58	95	

[†]All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54AS843, SN54AS844
SN74AS843, SN74AS844

9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

'AS843 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $R_1 = 500 \Omega$, $R_2 = 500 \Omega$, $T_A = \text{MIN to MAX}$				UNIT
			SN54AS843		SN74AS843		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1	8.5	1	6.5	ns
t_{PHL}			1	10	1	9	
t_{PLH}	C	O	2	13	2	12	ns
t_{PHL}			2	13	2	12	
t_{PLH}	$\overline{\text{PRE}}$	Q	2	12	2	10	ns
t_{PHL}	$\overline{\text{CLR}}$	Q	2	14	2	13	ns
t_{PZH}	$\overline{\text{OC}}$	Q	2	13.5	2	10.5	ns
t_{PZL}			2	15	2	13.5	
t_{PHZ}	$\overline{\text{OC}}$	Q	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

'AS844 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $R_1 = 500 \Omega$, $R_2 = 500 \Omega$, $T_A = \text{MIN to MAX}$				UNIT
			SN54AS844		SN74AS844		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1	11	1	8.5	ns
t_{PHL}			1	11	1	10	
t_{PLH}	C	O	2	14	2	12.5	ns
t_{PHL}			2	14	2	13	
t_{PLH}	$\overline{\text{PRE}}$	Q	2	12	2	10	ns
t_{PHL}	$\overline{\text{CLR}}$	Q	2	14.5	2	13.5	ns
t_{PZH}	$\overline{\text{OC}}$	Q	2	14.5	2	12	ns
t_{PZL}			2	15	2	13.5	
t_{PHZ}	$\overline{\text{OC}}$	Q	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

2
LSI Devices

**SN54ALS843, SN54AS843, SN54ALS844, SN54AS844
 SN74ALS843, SN74AS843, SN74ALS844, SN74AS844
 9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS**

D latch signal conventions

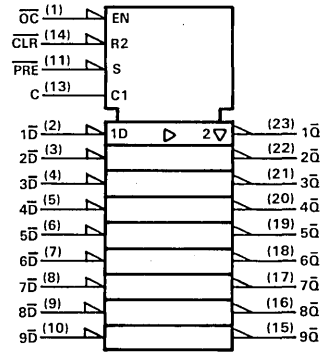
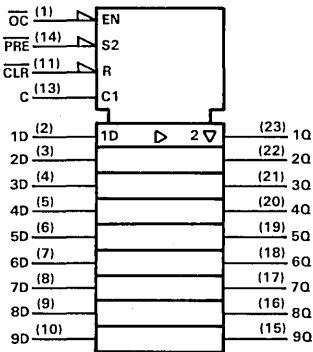
It is normal TI practice to name the outputs and other inputs of a D-type latch and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called \bar{Q} . An input that causes a Q output to go high or a \bar{Q} output to go low is called Preset; an input that causes a \bar{Q} output to go high or a Q output to go low is called Clear. Bars are used over these pin names (\overline{PRE} and \overline{CLR}) if they are active low. The devices on this data sheet are second-source designs and the pin-name conventions used by the original manufacturer have been retained. That makes it necessary to designate the data inputs and outputs of the inverting circuit \bar{D} and \bar{Q} .

In some applications it may be advantageous to redesignate the inputs and outputs \bar{D} and \bar{Q} for the noninverting circuits or D and \bar{Q} for the inverting circuits. In that case signal names should change as shown below. Also shown are corresponding changes in the logic symbols.

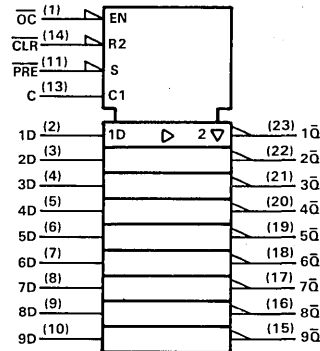
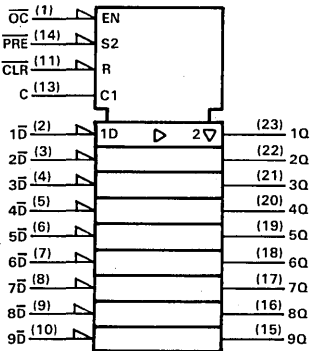
Notice that Q becoming \bar{Q} causes \overline{PRE} and \overline{CLR} to exchange their names and their S and R function labels. The presence or absence of polarity indicators (∇) changes at the data inputs and outputs, but not at \overline{PRE} , \overline{CLR} , and \overline{OC} since these inputs are still active-low.

2
LSI Devices

'ALS843, 'AS843



'ALS844, 'AS844



SN54ALS845, SN54AS845, SN54ALS846, SN54AS846 SN74ALS845, SN74AS845, SN74ALS846, SN74AS846 8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

D2825, DECEMBER 1983—REVISED JANUARY 1986

- 3-State Buffer-Type Outputs Drive Bus-Lines Directly
- Bus-Structured Pinout
- Provides Extra Bus Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity
- Buffered Control Inputs to Reduce DC Loading
- Power-Up High-Impedance State
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

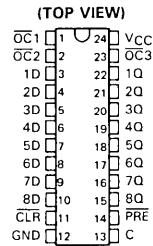
description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

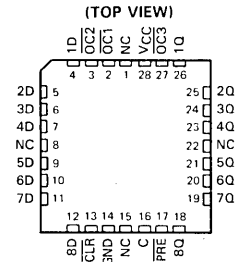
The eight latches are transparent D-type. The 'ALS845 and 'AS845 have noninverting data (D) inputs. The 'ALS846 and 'AS846 have inverting D inputs. Since CLR and PRE are independent of the clock, taking the CLR input low will cause the eight Q outputs to go low. Taking the PRE input low will cause the eight Q outputs to go high. When both PRE and CLR are taken low, the outputs will follow the preset condition.

The buffered output control inputs ($\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$) can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

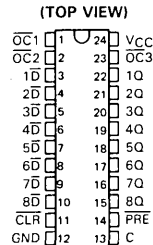
SN54ALS845, SN54AS845 . . . JT PACKAGE
SN74ALS845, SN74AS845 . . . DW OR NT PACKAGE



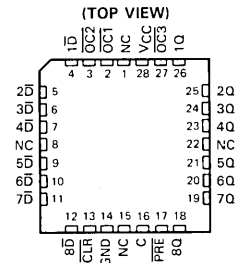
SN54ALS846, SN54AS846 . . . FK PACKAGE
SN74ALS846, SN74AS846 . . . FN PACKAGE



SN54ALS846, SN54AS846 . . . JT PACKAGE
SN74ALS846, SN74AS846 . . . DW OR NT PACKAGE



SN54ALS846, SN54AS846 . . . FK PACKAGE
SN74ALS846, SN74AS846 . . . FN PACKAGE



NC—No internal connection

This document contains information on products in more than one phase of development. The status of each device is indicated on the page(s) specifying its electrical characteristics.

SN54ALS845, SN54AS845, SN54ALS846, SN54AS846 SN74ALS845, SN74AS845, SN74ALS846, SN74AS846 8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

The -1 versions of the SN74ALS845 and SN74ALS846 parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS845 and SN54ALS846.

The SN54ALS845, SN54AS845, SN54ALS846, and SN54AS846 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS845, SN74AS845, SN74ALS846, and SN74AS846 are characterized for operation from 0°C to 70°C .

FUNCTION TABLES

'ALS845, 'AS845

INPUTS								OUTPUT
PRE	CLR	OC1	OC2	OC3	C	D	Q	
L	H	L	L	L	X	X	H	
H	L	L	L	L	X	X	L	
L	L	L	L	L	X	X	H	
H	H	L	L	L	H	L	L	
H	H	L	L	L	H	H	H	
H	H	L	L	L	L	X	Q_0	
X	X	X	X	H	X	X	Z	
X	X	X	H	X	X	X	Z	
X	X	H	X	X	X	X	Z	

'ALS846, 'AS846

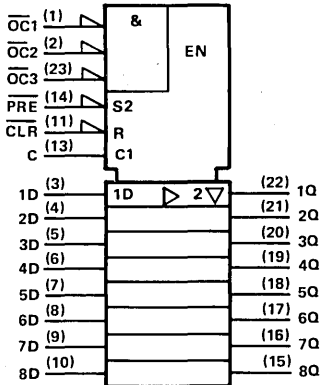
INPUTS								OUTPUT
PRE	CLR	OC1	OC2	OC3	C	D	Q	
L	H	L	L	L	X	X	H	
H	L	L	L	L	X	X	L	
L	L	L	L	L	X	X	H	
H	H	L	L	L	H	L	H	
H	H	L	L	L	H	H	L	
H	H	L	L	L	L	X	Q_0	
X	X	X	X	H	X	X	Z	
X	X	X	H	X	X	X	Z	
X	X	H	X	X	X	X	Z	

2

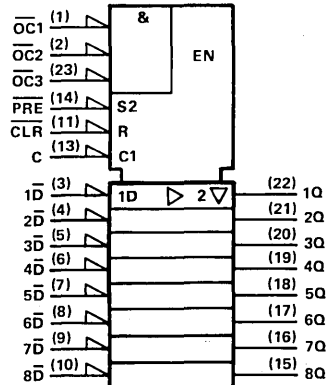
LSI Devices

logic symbols†

'ALS845, 'AS845



'ALS846, 'AS846



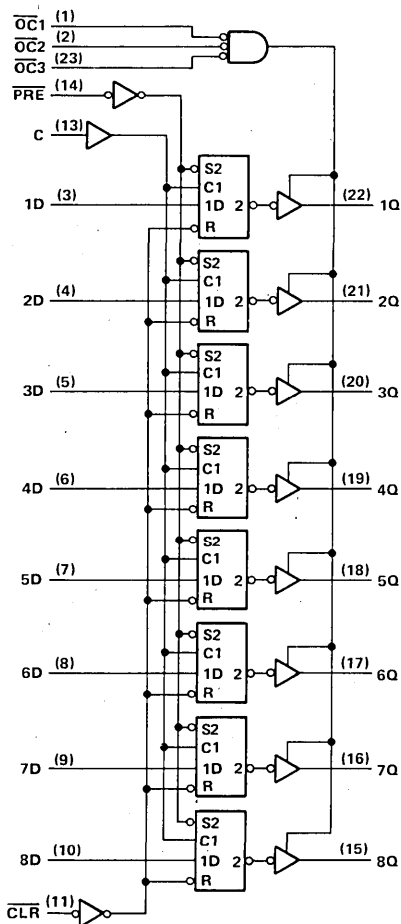
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

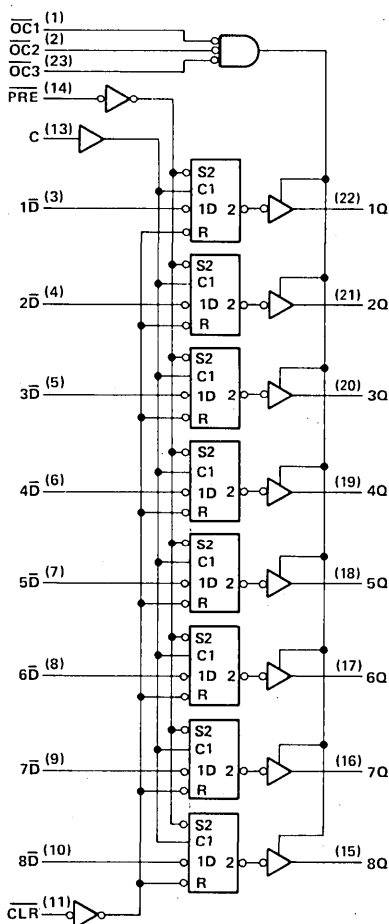
SN54ALS845, SN54AS845, SN54ALS846, SN54AS846 SN74ALS845, SN74AS845, SN74ALS846, SN74AS846 8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

logic diagrams (positive logic)

'ALS845, 'AS845



'ALS846, 'AS846



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range:	
SN54ALS845, SN54AS845, SN54ALS846, SN54AS846	-55°C to 125°C
SN74ALS845, SN74AS845, SN74ALS846, SN74AS846	-0°C to 70°C
Storage temperature range	-65°C to 150°C

SN54ALS845, SN74ALS845

8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

recommended operating conditions

	SN54ALS845			SN74ALS845			UNIT		
	MIN	NOM	MAX	MIN	NOM	MAX			
V _{CC} Supply voltage	4.5	5	5.5	4.5	5	5.5	V		
V _{IH} High-level input voltage	2			2			V		
V _{IL} Low-level input voltage	0.8			0.8			V		
I _{OH} High-level output current	-1			-2.6			mA		
I _{OL} Low-level output current	12			48†			mA		
t _w Pulse duration	CLR or PRE low			35			ns		
	C high			20					
t _{su} Setup time, data before enable C↓	16			10			ns		
t _h Hold time, data after enable C↓	7			5			ns		
T _A Operating free-air temperature	-55			125			0	70	°C

†The extended limit applies only if V_{CC} is maintained between 4.75 V and 5.25 V. The 48 mA limit applies for SN74ALS845-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS845		SN74ALS845		UNIT
		MIN	TYP‡	MAX	MIN	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2		V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA	V _{CC} - 2		V _{CC} - 2		V
	V _{CC} = 4.5 V, I _{OH} = -1 mA	2.4	3.3			
	V _{CC} = 4.5 V, I _{OH} = -2.6 mA			2.4	3.2	
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 12 mA	0.25		0.4		V
	V _{CC} = 4.5 V, I _{OL} = 24 mA			0.35		
	(I _{OL} = 48 mA for -1 versions)			0.5		
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V	20		20		μA
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.4 V	-20		-20		μA
I _I	V _{CC} = 5.5 V, V _I = 7 V	0.1		0.1		mA
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V	20		20		μA
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V	-0.1		-0.1		mA
I _O [§]	V _{CC} = 5.5 V, V _O = 2.25 V	-30	-112	-30	-112	mA
I _{CC}	V _{CC} = 5.5 V	Outputs high		21	36	mA
		Outputs low		41	67	
		Outputs disabled		25	42	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_O.

SN54ALS845, SN74ALS845 8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX			UNIT	
			ALS845			SN54ALS845		SN74ALS845		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
t _{PLH}	D	Q	7	11	2	15	2	13	ns	
t _{PHL}			11	15	4	20	4	18		
t _{PLH}	C	Q	12	18	5	25	5	21	ns	
t _{PHL}			16	23	8	30	8	26		
t _{PLH}	$\overline{\text{PRE}}$	Q	13	19	5	25	6	22	ns	
t _{PHL}			19	26	4	35	6	30		
t _{PLH}	$\overline{\text{CLR}}$	Q	19	26	4	35	6	30	ns	
t _{PHL}			16	22	6	28	6	24		
t _{PZH}	$\overline{\text{OC}}$	Q	9	14	2	18	3	16	ns	
t _{PZL}			12	17	4	20	5	18		
t _{PHZ}	$\overline{\text{OC}}$	Q	4	9	1	12	1	11	ns	
t _{PLZ}			6	11	2	14	2	12		

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

2

LSI Devices

PRODUCTION DATA documents contain information current as of publication date. Products conform to these specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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recommended operating conditions

		SN54ALS846			SN74ALS846			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage	0.8			0.8			V
I _{OH}	High-level output current	-1			-2.6			mA
I _{OL}	Low-level output current	12			24			mA
					48 [†]			
t _w	Pulse duration	CLR or PRE low						ns
		C high						
t _{su}	Setup time, data before enable C _I							ns
t _h	Hold time, data after enable C _I							ns
T _A	Operating free-air temperature	-55		125		0 70		°C

[†] The extended limit applies only if V_{CC} is maintained between 4.75 V and 5.25 V. The 48 mA limit applies for SN74ALS846-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

2 LSI Devices

PARAMETER	TEST CONDITIONS	SN54ALS846		SN74ALS846		UNIT
		MIN	TYP [‡] MAX	MIN	TYP [‡] MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA	-1.2		-1.2		V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA	V _{CC} -2		V _{CC} -2		V
	V _{CC} = 4.5 V, I _{OH} = -1 mA	2.4	3.3			
	V _{CC} = 4.5 V, I _{OH} = -2.6 mA			2.4	3.2	
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 12 mA	0.25 0.4				V
	V _{CC} = 4.5 V, I _{OL} = 24 mA					
	(I _{OL} = 48 mA for -1 versions)			0.35	0.5	
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V	20		20		μA
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.4 V	-20		-20		μA
I _I	V _{CC} = 5.5 V, V _I = 7 V	0.1		0.1		mA
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V	20		20		μA
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V	-0.1		-0.1		mA
I _O [§]	V _{CC} = 5.5 V, V _O = 2.25 V	-30	-112	-30	-112	mA
I _{CC}	V _{CC} = 5.5 V	Outputs high				mA
		Outputs low				
		Outputs disabled				

[‡] All typical values are at V_{CC} = 5 V, T_A = 25 °C.

[§] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = 25 °C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX			UNIT	
			'ALS846			SN54ALS846		SN74ALS846		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
t _{PLH}	D	Q							ns	
t _{PHL}										
t _{PLH}	C	Q							ns	
t _{PHL}										
t _{PLH}	PRE	Q							ns	
t _{PHL}										
t _{PLH}	CLR	Q							ns	
t _{PHL}										
t _{PZH}	OC	Q							ns	
t _{PZL}										
t _{PHZ}	OC	Q							ns	
t _{PLZ}										

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

Additional information on these products can be obtained from the factory as it becomes available.

SN54AS845, SN54AS846
SN74AS845, SN74AS846
8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

recommended operating conditions

		SN54AS845 SN54AS846			SN74AS845 SN74AS846			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage	0.8			0.8			V
I _{OH}	High-level output current	-24			-24			mA
I _{OL}	Low-level output current	32			48			mA
t _w	Pulse duration	CLR or PRE low		5	4		ns	
		C high		5	4			
t _{su}	Setup time, data before enable C↓	3.5			2.5			ns
t _h	Hold time, data after enable C↓	3.5			2.5			ns
t _r	Recovery time	PRE		17	15		ns	
		CLR		16	14			
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

2

LSI Devices

PARAMETER	TEST CONDITIONS		SN54AS845 SN54AS846			SN74AS845 SN74AS846			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA		-1.2			-1.2			V
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -2 mA		V _{CC} - 2			V _{CC} - 2			V
	V _{CC} = 4.5 V, I _{OH} = -15 mA		2.4	3.2		2.4	3.2		
	V _{CC} = 4.5 V, I _{OH} = -24 mA		2			2			
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 32 mA		0.25			0.5			V
	V _{CC} = 4.5 V, I _{OL} = 48 mA					0.35			
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V		50			50			μA
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.4 V		-50			-50			μA
I _I	V _{CC} = 5.5 V, V _I = 7 V		0.1			0.1			mA
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V		20			20			μA
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V		-0.5			-0.5			mA
I _O ‡	V _{CC} = 5.5 V, V _O = 2.25 V		-30			-112			mA
I _{CC}	'AS845	V _{CC} = 5.5 V	Outputs high		35	58	35	58	mA
			Outputs low		52	85	52	85	
	Outputs disabled		52	85	52	85			
	Outputs high		36	59	36	59			
	Outputs low		53	87	53	87			
	Outputs disabled		53	87	53	87			

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{O5}.

SN54AS845, SN54AS846
SN74AS845, SN74AS846

8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

'AS845 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V,}$ $C_L = 50\text{ pF,}$ $R_1 = 500\ \Omega,$ $R_2 = 500\ \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54AS845		SN74AS845		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1	8.5	1	6.5	ns
t_{PHL}			1	10	1	9	
t_{PLH}	C	Q	2	13	2	12	ns
t_{PHL}			2	13	2	12	
t_{PLH}	PRE	Q	2	12	2	10	ns
t_{PHL}	CLR	Q	2	14	2	13	ns
t_{PHL}	\overline{OC}	Q	2	13.5	2	10.5	ns
t_{PZL}			2	15	2	13.5	
t_{PHZ}	\overline{OC}	Q	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

'AS846 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V,}$ $C_L = 50\text{ pF,}$ $R_1 = 500\ \Omega,$ $R_2 = 500\ \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54AS846		SN74AS846		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1	11	1	8.5	ns
t_{PHL}			1	11	1	10	
t_{PLH}	C	Q	2	14	2	12.5	ns
t_{PHL}			2	14	2	13	
t_{PLH}	PRE	Q	2	12	2	10	ns
t_{PHL}	CLR	Q	2	14.5	2	13.5	ns
t_{PHL}	\overline{OC}	Q	2	14.5	2	12	ns
t_{PZL}			2	15	2	13.5	
t_{PHZ}	\overline{OC}	Q	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

2
LSI Devices

SN54ALS845, SN54AS845, SN54ALS846, SN54AS846
SN74ALS845, SN74AS845, SN74ALS846, SN74AS846
8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

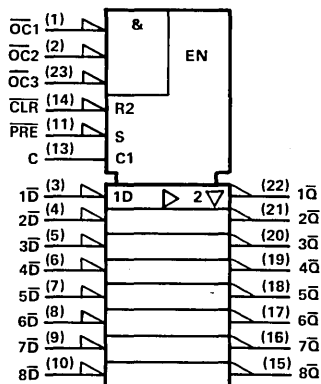
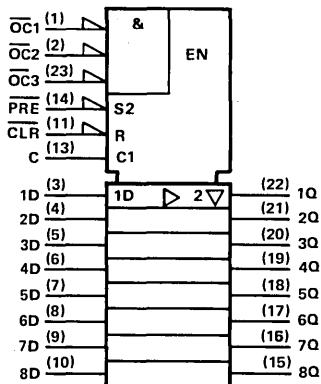
D latch signal conventions

It is normal TI practice to name the outputs and other inputs of a D-type latch and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called \bar{Q} . An input that causes a Q output to go high or a \bar{Q} output to go low is called Preset; and input that causes a \bar{Q} output to go high or a Q output to go low is called Clear. Bars are used over these pin names (PRE and CLR) if they are active low. The devices on this data sheet are second-source designs and the pin-name conventions used by the original manufacturer have been retained. That makes it necessary to designate the data inputs and outputs of the inverting circuit \bar{D} and Q.

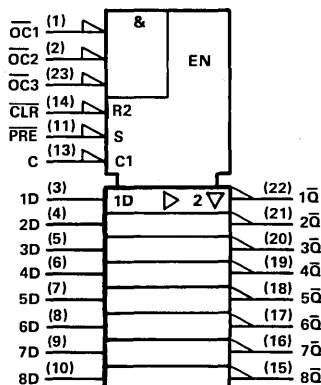
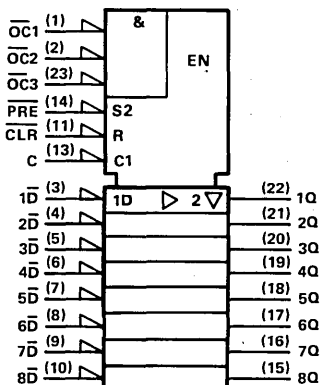
In some applications it may be advantageous to redesignate the inputs and outputs \bar{D} and \bar{Q} for the noninverting circuits or D and \bar{Q} for the inverting circuits. In that case signal names should change as shown below. Also shown are corresponding changes in the logic symbols.

Notice that Q becoming \bar{Q} causes \overline{PRE} and \overline{CLR} to exchange their names and their S and R function labels. The presence or absence of polarity indicators ($\bar{\square}$) changes at the data inputs and outputs, but not at CLR/PRE, OC1, OC2, and OC3 since these inputs are still active-low.

'ALS845, 'AS845



'ALS846, 'AS846



2

LSI Devices

- 4-Line to 1-Line Data Selectors/Multiplexers That Can Select 1 of 16 Data Inputs.

Typical Applications:

Boolean Function Generators
Parallel-to-Serial Converters
Data Source Selectors

- Cascadable to n-Bits
- 3-State Bus Driver Outputs
- 'AS850 Offers Clocked Selects; 'AS851 Offers Enable-Controlled Selects
- Has a Master Output Control (\bar{G}) for Cascading and Individual Output Controls ($\bar{G}\bar{Y}$, GW) for Each Output
- Package Options Include both Plastic and Ceramic Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

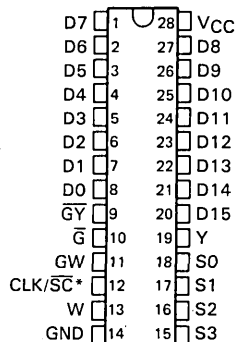
These four-line to one-line data selectors/multiplexers provide full binary decoding to select one-of-sixteen data sources with complementary Y and W outputs. The 'AS850 has a clock-controlled select register allowing for a symmetrical presentation of the select inputs to the decoder while the 'AS851 has an enable-controlled select register allowing the user to select and hold one particular data line.

A buffered group of output controls (\bar{G} , $\bar{G}\bar{Y}$, GW) can be used to place the two-outputs in either a normal logic (high or low logic level) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without the need for interface or pull-up components.

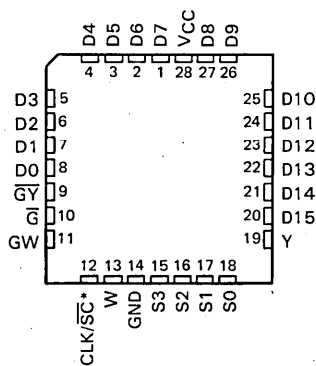
The output controls do not affect the internal operations of the data selector/multiplexer. New data can be setup while the outputs are in the high-impedance state.

The SN74AS850 and SN74AS851 are characterized for operation from 0°C to 70°C.

SN74AS850, SN74AS851 . . . N PACKAGE
(TOP VIEW)



SN74AS850, SN74AS851 . . . FN PACKAGE
(TOP VIEW)



*CLK for 'AS850 or SC for 'AS851

SN74AS850, SN74AS851

1 OF 16 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

INPUT SELECTION TABLE

SELECT INPUTS				'AS850	'AS851	INPUT SELECTED
S3	S2	S1	S0	CLK	\overline{SC}	
L	L	L	L	↑	L	D0
L	L	L	H	↑	L	D1
L	L	H	L	↑	L	D2
L	L	H	H	↑	L	D3
L	H	L	L	↑	L	D4
L	H	L	H	↑	L	D5
L	H	H	L	↑	L	D6
L	H	H	H	↑	L	D7
H	L	L	L	↑	L	D8
H	L	L	H	↑	L	D9
H	L	H	L	↑	L	D10
H	L	H	H	↑	L	D11
H	H	L	L	↑	L	D12
H	H	L	H	↑	L	D13
H	H	H	L	↑	L	D14
H	H	H	H	↑	L	D15
X	X	X	X	H or L	H	Dn

OUTPUT FUNCTION TABLE

\overline{G}	\overline{GY}	GW	OUTPUTS	
			Y	W
H	X	X	Z	Z
L	H	L	Z	Z
L	L	L	D	Z
L	H	H	Z	\overline{D}
L	L	H	D	\overline{D}

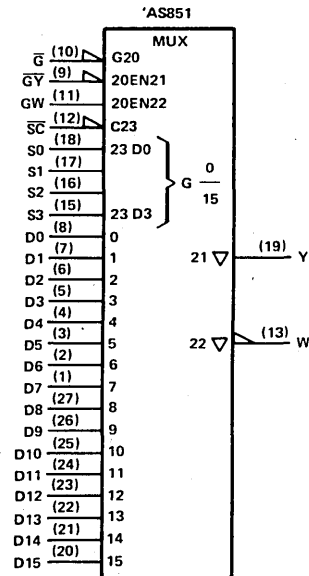
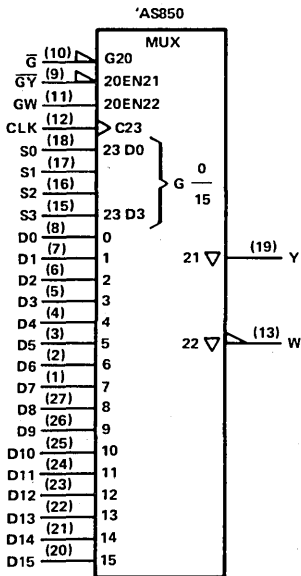
D = level of selected input D0—D15

2

LSI Devices

Dn = the input selected before the most-recent low-to-high transition of CLK or \overline{SC} .

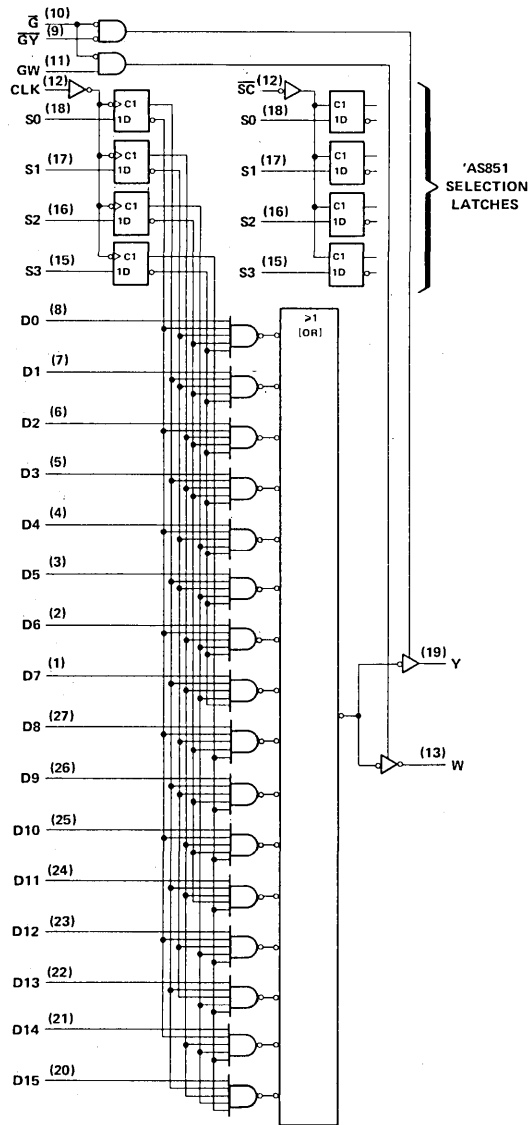
logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74AS850, SN74AS851
 1 OF 16 DATA SELECTORS/MULTIPLEXERS
 WITH 3-STATE OUTPUTS

'AS850 logic diagrams (positive logic) (see inset for 'AS851)



2
 LSI Devices

SN74AS850, SN74AS851

1 OF 16 DATA SELECTORS/MULTIPLEXERS

WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

SN74AS850 recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			48	mA
f_{clock}	Clock frequency	0		60	MHz
t_w	Pulse duration	CLK high	8		ns
		CLK low	8		
t_{su}	Setup time, select inputs before CLK↑	10			ns
t_h	Hold time, select inputs after CLK↑	0			ns
T_A	Operating free-air temperature	0		70	°C

2

LSI Devices

SN74AS850 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
V_{IK}	$V_{CC} = 4.5 V, I_I = -18 mA$				-1.2	V	
V_{OH}	$V_{CC} = 4.5 V \text{ to } 5.5 V, I_{OH} = -2 mA$		$V_{CC} - 2$			V	
	$V_{CC} = 4.5 V, I_{OH} = -15 mA$		2	3.3			
V_{OL}	$V_{CC} = 4.5 V, I_{OL} = 48 mA$			0.35	0.5	V	
I_{OZH}	$V_{CC} = 5.5 V, V_O = 2.7 V$				50	μA	
I_{OZL}	$V_{CC} = 5.5 V, V_O = 0.4 V$				-50	μA	
I_I	$V_{CC} = 5.5 V, V_I = 7 V$				0.1	mA	
I_{IH}	$V_{CC} = 5.5 V, V_I = 2.7 V$				20	μA	
I_{IL}	D, \bar{G}	$V_{CC} = 5.5 V, V_I = 0.4 V$			-1	mA	
	All others				-0.5		
I_O^\ddagger	$V_{CC} = 5.5 V, V_O = 2.25 V$		-30		-112	mA	
I_{CC}	$V_{CC} = 5.5 V$		Outputs active		50	81	mA
			Outputs disabled		52	85	

† All typical values are at $V_{CC} = 5 V, T_A = 25^\circ C$.

‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS} .

SN74AS850
1 OF 16 DATA SELECTORS/MULTIPLEXERS
WITH 3-STATE OUTPUTS

SN74AS850 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = 0°C to 70°C		UNIT
			MIN	MAX	
f _{max}			60		MHz
t _{PLH}	Any D	Y	3	10.5	ns
t _{PHL}			3	11	
t _{PLH}	Any D	W	3	8	ns
t _{PHL}			1	6	
t _{PLH}	CLK	Y	3	14.5	ns
t _{PHL}			3	17.5	
t _{PLH}	CLK	W	3	15	ns
t _{PHL}			3.5	13	
t _{PZH}	$\bar{0}$	Y	2	8	ns
t _{PZL}			3	11	
t _{PHZ}	$\bar{0}$	Y	1	6	ns
t _{PLZ}			2	8	
t _{PZH}	$\bar{0}$	W	2	8	ns
t _{PZL}			3	21	
t _{PHZ}	$\bar{0}$	W	1	6	ns
t _{PLZ}			2	8	
t _{PZH}	$\bar{0}\bar{Y}$	Y	2	8	ns
t _{PZL}			3	11	
t _{PHZ}	$\bar{0}\bar{Y}$	Y	1	6	ns
t _{PLZ}			2	8	
t _{PZH}	GW	W	2	10	ns
t _{PZL}			3	25	
t _{PHZ}	GW	W	1	6	ns
t _{PLZ}			2	11	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

2

LSI Devices

SN74AS851
1 OF 16 DATA SELECTORS/MULTIPLEXERS
WITH 3-STATE OUTPUTS

SN74AS851 recommended operating conditions

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			V
V _{IL}	Low-level input voltage			0.8	V
I _{OH}	High-level output current			-15	mA
I _{OL}	Low-level output current			48	mA
t _w	Pulse duration, \overline{SC} low	10			ns
t _{su}	Setup time, select inputs before \overline{SC} †	4.5			ns
t _h	Hold time, select inputs after \overline{SC} †	0			ns
T _A	Operating free-air temperature	0		70	°C

SN74AS851 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA				-1.2	C
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -2 mA		V _{CC} - 2			V
	V _{CC} = 4.5 V, I _{OH} = -15 mA		2	3.3		
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 48 mA		0.35	0.5		V
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V				50	μA
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.4 V				-50	μA
I _I	V _{CC} = 5.5 V, V _I = 7 V				0.1	mA
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V				20	μA
I _{IL}	D, \overline{G}	V _{CC} = 5.5 V, V _I = 0.4 V			-1	mA
	All others				-0.5	
I _O ‡	V _{CC} = 5.5 V, V _O = 2.25 V		-30		-112	mA
I _{CC}	V _{CC} = 5.5 V					mA
			Outputs active		50 81	
			Outputs disabled		52 85	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

2
LSI Devices

SN74AS851
1 OF 16 DATA SELECTORS/MULTIPLEXERS
WITH 3-STATE OUTPUTS

SN74AS851 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = 0°C to 70°C		UNIT
			MIN	MAX	
t _{PLH}	Any D	Y	3	10.5	ns
t _{PHL}			3	11	
t _{PLH}	Any D	W	3	8	ns
t _{PHL}			1	6	
t _{PLH}	S0, S1, S2, S3	Y	3	18	ns
t _{PHL}			3	19	
t _{PLH}	S0, S1, S2, S3	W	3	16	ns
t _{PHL}			3	15	
t _{PLH}	\overline{SC}	Y	3	18	ns
t _{PHL}			3	20	
t _{PLH}	\overline{SC}	W	3	16	ns
t _{PHL}			3	15	
t _{PZH}	\overline{G}	Y	2	8	ns
t _{PZL}			3	11	
t _{PHZ}	\overline{G}	Y	1	6	ns
t _{PLZ}			2	8	
t _{PZH}	\overline{G}	W	2	8	ns
t _{PZL}			3	21	
t _{PHZ}	\overline{G}	W	1	6	ns
t _{PLZ}			2	8	
t _{PZH}	\overline{GY}	Y	2	8	ns
t _{PZL}			3	11	
t _{PHZ}	\overline{GY}	Y	1	6	ns
t _{PLL}			2	8	
t _{PZH}	GW	W	2	10	ns
t _{PZL}			3	25	
t _{PHZ}	GW	W	1	6	ns
t _{PLZ}			2	11	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

2

LSI Devices

SN74AS850, SN74AS851
1 OF 16 DATA SELECTORS/MULTIPLEXERS
WITH 3-STATE OUTPUTS

TYPICAL APPLICATION DATA

The 'AS850 or 'AS851 can be used as a 1-of-16 Boolean function generator. Figure 1 shows the 'AS850 in one example.

2

LSI Devices

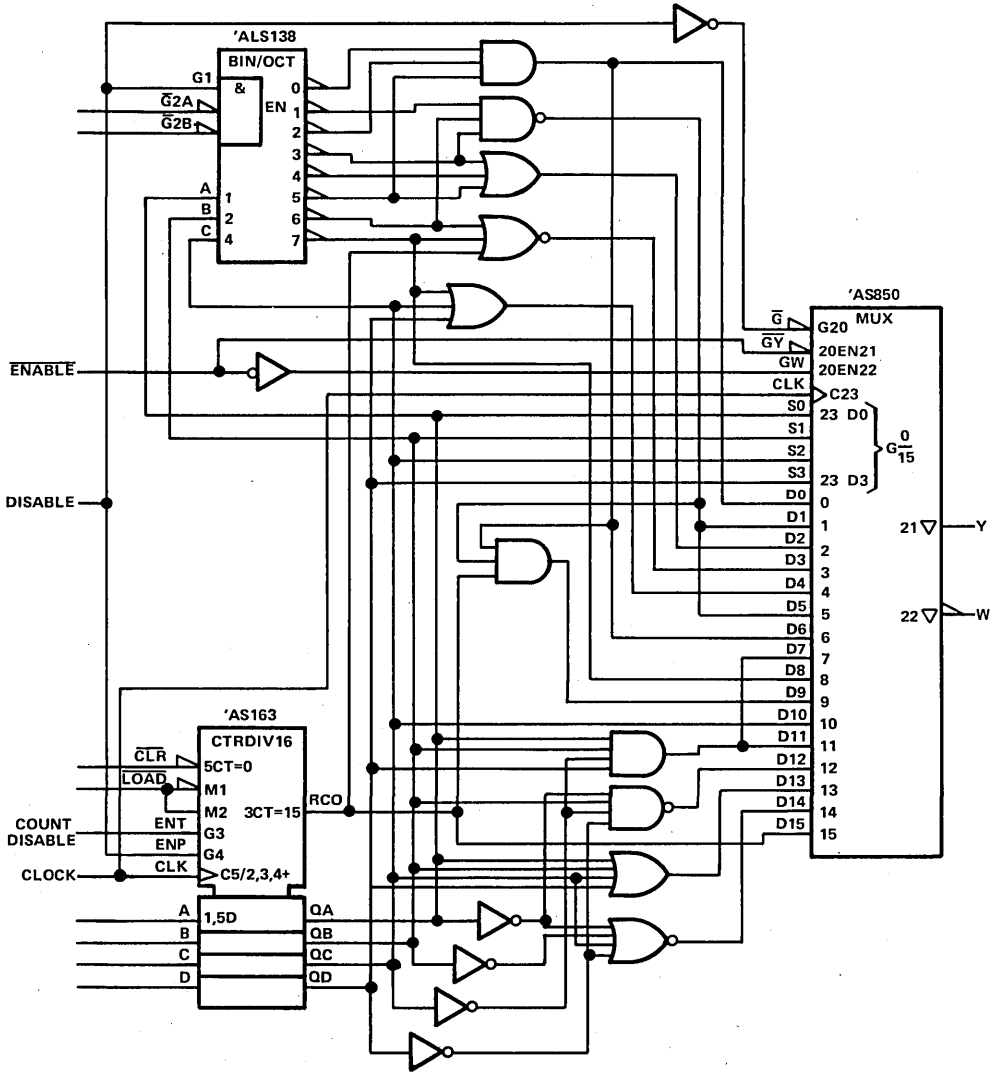


FIGURE 1. 1-of-16 BOOLEAN FUNCTION GENERATOR

SN74AS850
 1 OF 16 DATA SELECTORS/MULTIPLEXERS
 WITH 3-STATE OUTPUTS

TYPICAL APPLICATION DATA

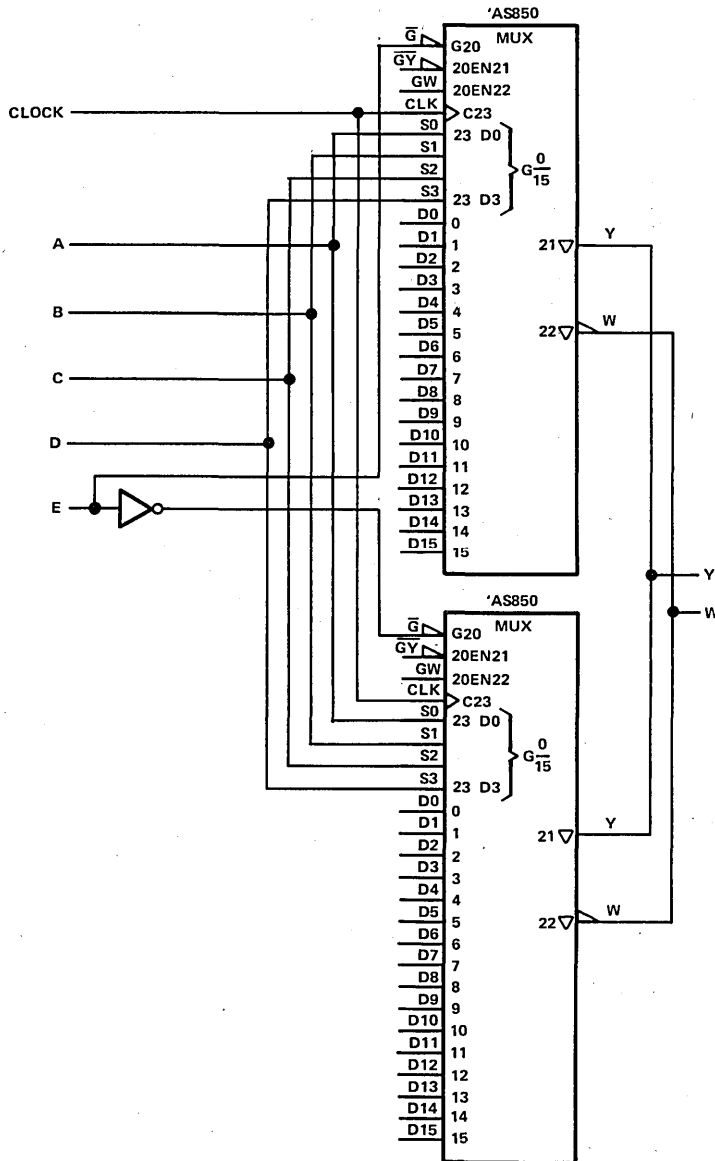


FIGURE 2. 1-of-32 DATA SELECTOR/MULTIPLEXER

2
 LSI Devices

SN74AS850
1 OF 16 DATA SELECTORS/MULTIPLEXERS
WITH 3-STATE OUTPUTS

TYPICAL APPLICATION DATA

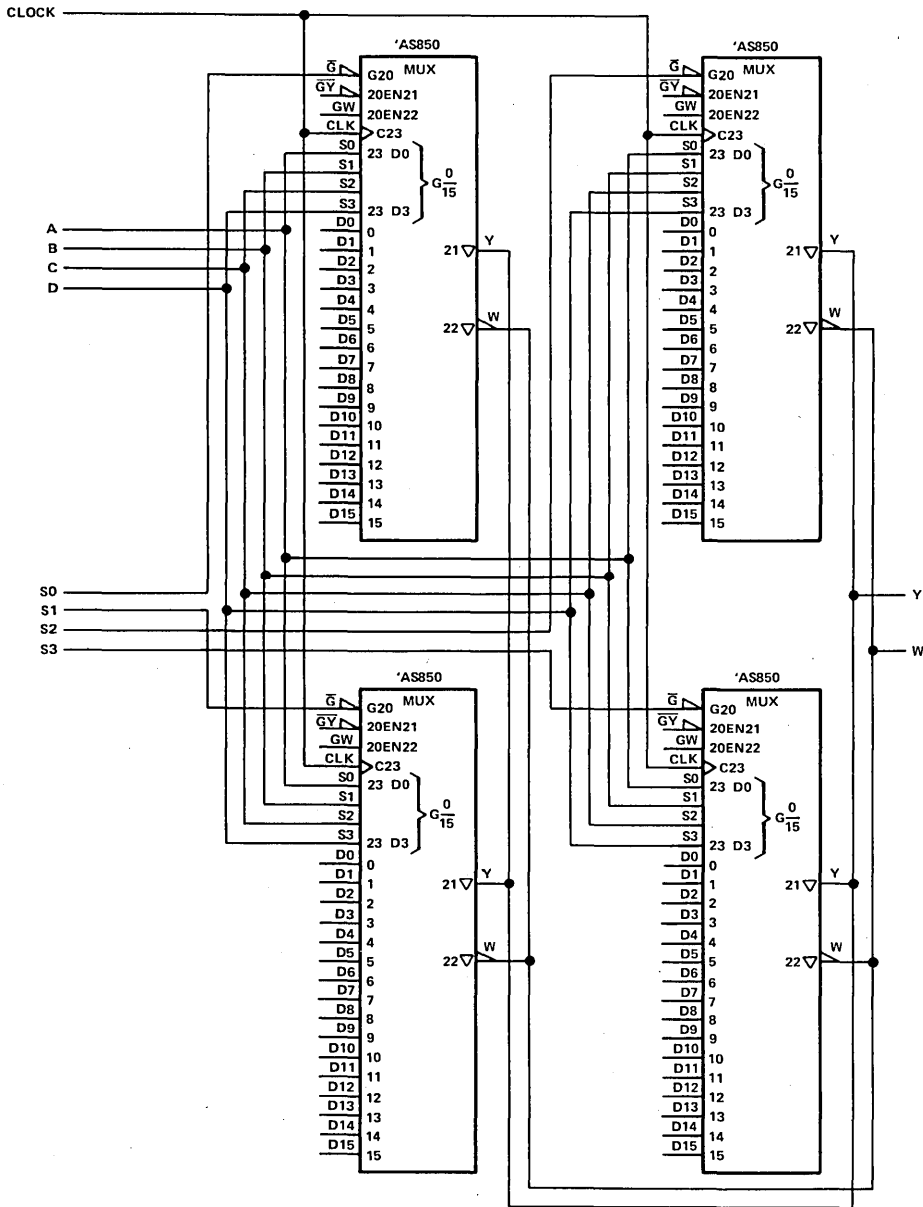


FIGURE 3. 1-of-64 DATA SELECTOR/MULTIPLEXER

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LSI Devices

SN54AS852, SN74AS852 8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

D2810, JUNE 1984—REVISED JANUARY 1986

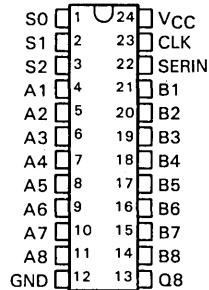
- Included among the Package Options are Compact, 24-Pin, 300-mil-Wide DIPs and Both 28-Pin Plastic and Ceramic Chip Carriers
- Buffered 3-State Outputs Drive Bus Lines Directly
- Cascadable to n-Bits
- Eight Selectable Transceiver/Port Functions:
 - A to B or B to A
 - Register to A or B
 - Shifted to A from B or Shifted to B from A
 - Off-Line Shifts (A and B Ports Transceiving or in High-Impedance State)
 - Register Clear
- Particularly Suitable for Use in Diagnostics Circuitry
- Serial Register Provides:
 - Parallel Storage of Either A or B Input Data
 - Serial Transmission of Data from Either A or B Port
- Dependable Texas Instruments Quality and Reliability

description

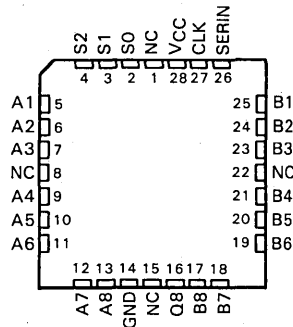
The 'AS852 features two 8-bit I/O ports (A1-A8 and B1-B8), and 8-bit parallel-load, serial-in, parallel-out shift register, and control logic. With these features, this device is capable of performing eight selectable transceiver or port functions, depending on the state of the three select lines S0, S1, and S2. These functions include: transferring data from port A to port B or vice versa (i.e., the transceiver function), transferring data from the register to either port, serial shifting data to either port from the opposite port, performing off-line shifts (with A and B ports in high-impedance state), and clearing the register. The 'AS852 can simultaneously transfer data from A to B or B to A and perform an off-line serial shift of data in the register. Synchronous parallel loading of the internal register can be accomplished from either port on the positive transition of the clock while serially shifting data in via the SERIN input. The 'AS852 is ideally suited for applications implementing diagnostic circuitry to enhance system verification and/or fault analysis. All serial data is shifted right. All outputs are buffer-type outputs designed specifically to drive bus lines directly and all are 3-state except for Q8, which is a totem-pole output.

The SN54AS852 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74AS852 is characterized for operation from 0°C to 70°C.

SN54AS852 . . . JT PACKAGE
SN74AS852 . . . DW or NT PACKAGE
(TOP VIEW)



SN54AS852 . . . FK PACKAGE
SN74AS852 . . . FN PACKAGE
(TOP VIEW)



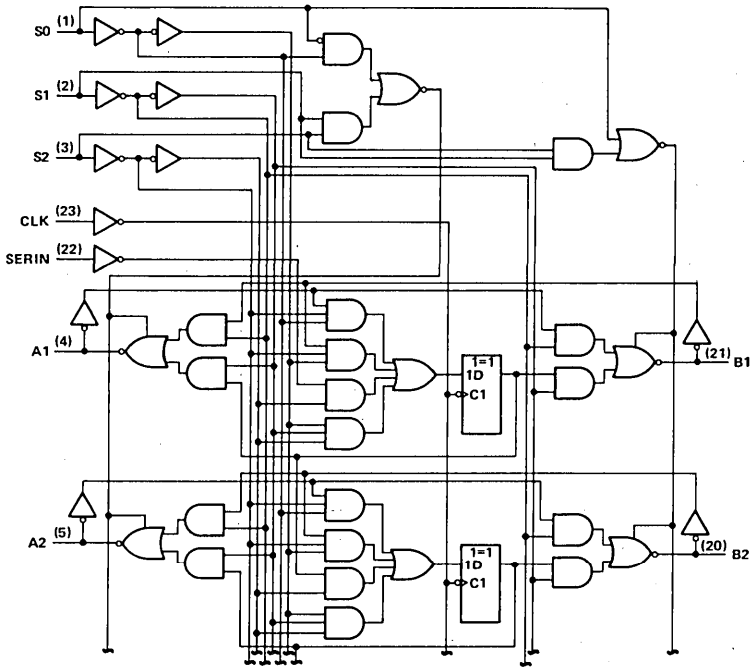
NC—No internal connection

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LSI Devices

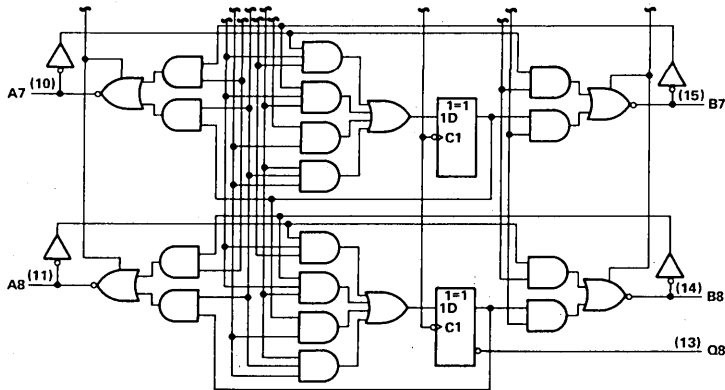
SN54AS852, SN74AS852
8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

logic diagram (positive logic)



FOUR IDENTICAL CHANNELS NOT SHOWN
 INPUTS/OUTPUTS NOT SHOWN:

- | | |
|--------|---------|
| (6) A3 | (19) B3 |
| (7) A4 | (18) B4 |
| (8) A5 | (17) B5 |
| (9) A6 | (16) B6 |



Pin numbers shown are for DW, JT, and NT packages.

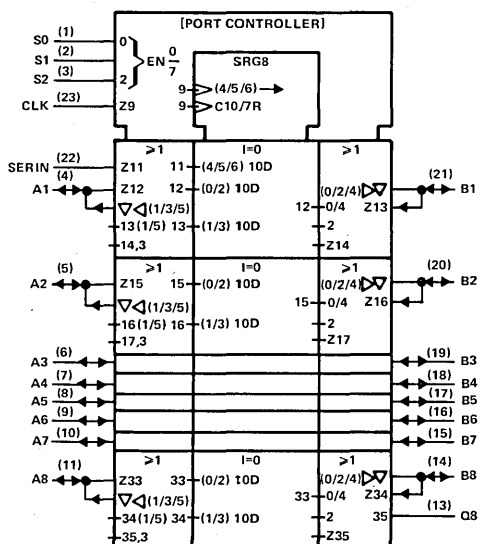
SN54AS852, SN74AS852 8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

FUNCTION TABLE

MODE S2 S1 S0	CLOCK	SERIN	A1 Q1 B1	A2 Q2 B2	A3 Q3 B3	A4 Q4 B4	A5 Q5 B5	A6 Q6 B6	A7 Q7 B7	A8 Q8 B8	PORT FUNCTION
L L L	H or L	X	Z Q _n A1	Z Q _n A2	Z Q _n A3	Z Q _n A4	Z Q _n A5	Z Q _n A6	Z Q _n A7	Z Q _n A8	A TO B
L L L	↑	X	Z A1 A1	Z A2 A2	A A3 A3	Z A4 A4	Z A5 A5	Z A6 A6	Z A7 A7	Z A8 A8	
L L H	H or L	X	B1 Q _n Z	B2 Q _n Z	B3 Q _n Z	B4 Q _n Z	B5 Q _n Z	B6 Q _n Z	B7 Q _n Z	B8 Q _n Z	B TO A
L L H	↑	X	B1 B1 Z	B2 B2 Z	B3 B3 Z	B4 B4 Z	B5 B5 Z	B6 B6 Z	B7 B7 Z	B8 B8 Z	
L H L	H or L	X	X Q _n Q1	X Q _n Q2	X Q _n Q3	X Q _n Q4	X Q _n Q5	X Q _n Q6	X Q _n Q7	X Q _n Q8	Q _n TO B _n
L H L	↑	X	Z A1 A1	Z A2 A2	Z A3 A3	Z A4 A4	Z A5 A5	Z A6 A6	Z A7 A7	Z A8 A8	
L H H	H or L	X	Q1 Q _n X	Q2 Q _n X	Q3 Q _n X	Q4 Q _n X	Q5 Q _n X	Q6 Q _n X	Q7 Q _n X	Q8 Q _n X	Q _n TO A _n
L H H	↑	X	B1 B1 Z	B2 B2 Z	B3 B3 Z	B4 B4 Z	B5 B5 Z	B6 B6 Z	B7 B7 Z	B8 B8 Z	
H L L	H or L	X	Z Q _n A1	Z Q _n A2	Z Q _n A3	Z Q _n A4	Z Q _n A5	Z Q _n A6	Z Q _n A7	Z Q _n A8	SHIFT
H L L	↑	H	Z H A1	Z Q1 A2	Z Q2 A3	Z Q3 A4	Z Q4 A5	Z Q5 A6	Z Q6 A7	Z Q7 A8	AND
H L L	↑	L	Z L A1	Z Q1 A2	Z Q2 A3	Z Q3 A4	Z Q4 A5	Z Q5 A6	Z Q6 A7	Z Q7 A8	A TO B
H L H	H or L	X	B1 Q _n Z	B2 Q _n Z	B3 Q _n Z	B4 Q _n Z	B5 Q _n Z	B6 Q _n Z	B7 Q _n Z	B8 Q _n Z	SHIFT
H L H	↑	H	B1 H Z	B2 Q1 Z	B3 Q2 Z	B4 Q3 Z	B5 Q4 Z	B6 Q5 Z	B7 Q6 Z	B8 Q7 Z	AND
H L H	↑	L	B1 L Z	B2 Q1 Z	B3 Q2 Z	B4 Q3 Z	B5 Q4 Z	B6 Q5 Z	B7 Q6 Z	B8 Q7 Z	B TO A
H H L	H or L	X	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	SHIFT
H H L	↑	H	Z H Z	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	
H H L	↑	L	Z L Z	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	
H H H	H or L	X	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	CLEAR
H H H	↑	X	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	

n = level of Q_n(n = 1, 2, . . . 8) established on the most recent ↑ transition of CLK. Q1 through Q8 are the shift register outputs; only Q8 is available externally. The double inversions that take place as data travels from port to port are ignored in this table.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.

2
LSI Devices

SN54AS852, SN74AS852

8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

absolute maximum ratings over free-air temperature range

Supply voltage, V_{CC}	7 V
Input voltage: All inputs	7 V
I/O ports	5.5 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range: SN54AS852	-55°C to 125°C
SN74AS852	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54AS852			SN74AS852			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current	A1-A8, B1-B8		-12	-15		mA	
		Q8		-2	-2			
I_{OL}	Low-level output current	A1-A8, B1-B8		32	48		mA	
		Q8		20	20			
f_{clock}	Clock frequency	0	45	0	50		MHz	
t_w	Duration of clock pulse	11		10			ns	
t_{su}	Setup time before CLK1	A1-A8, B1-B8, SERIN		5.5	5.5		ns	
		S0, S1, S2		5.5	5.5			
t_h	Hold-time, data after CLK1	A1-A8, B1-B8, SERIN		0	0		ns	
		S0, S1, S2		0	0			
T_A	Operating free-air temperature	-55	125	0	70		°C	

2

LSI Devices

SN54AS852, SN74AS852 8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

electrical characteristics over recommended operating free-air temperature range
(unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54AS852		SN74AS852		UNIT
			MIN	TYP† MAX	MIN	TYP† MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = -18 mA	-1.2		-1.2		V
V _{OH}	A1-A8, B1-B8	V _{CC} = 4.5 V, I _{OH} = -12 mA	2.4	3.2			V
	All outputs	V _{CC} = 4.5 V, I _{OH} = -15 mA			2.4	3.3	
V _{OL}	All outputs except Q8	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -2 mA	V _{CC} -2		V _{CC} -2		V
		V _{CC} = 4.5 V, I _{OL} = 32 mA	0.3	0.5			
	Q8	V _{CC} = 4.5 V, I _{OL} = 48 mA			0.35	0.5	
I _I	S0, S1, S2	V _{CC} = 5.5 V, V _I = 7 V			0.3		mA
	CLK and SERIN				0.1		
	A1-A8, B1-B8				0.2		
I _{IH}	S0, S1, S2	V _{CC} = 5.5 V, V _I = 2.7 V			60		μA
	CLK and SERIN				20		
	A1-A8, B1-B8‡				70		
I _{IL}	S0, S1, S2	V _{CC} = 5.5 V, V _I = 0.4 V			-1		mA
	CLK and SERIN				-0.5		
	A1-A8, B1-B8‡				-0.5		
I _O §	Except Q8	V _{CC} = 5.5 V, V _O = 2.25 V	-30	-112	-30	-112	mA
	Q8		-20	-112	-20	-112	
I _{CC}		V _{CC} = 5.5 V	136	220	136	220	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the output currents I_{OZH} and I_{OZL}, respectively.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	R _L = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX				UNIT
			SN54AS852		SN74AS852		
			MIN	MAX	MIN	MAX	
f _{max}			45		50	MHz	
t _{PLH}	Any A port	Any B port	2	9	2	7.5	ns
t _{PHL}			3	12.5	3	11	
t _{PLH}	Any B port	Any A port	2	9	2	7.5	ns
t _{PHL}			3	12.5	3	11	
t _{PLH}	S0, S1, S2†	Any A or B port	3	11.5	3	10	ns
t _{PHL}			3	12	3	10.5	
t _{PLH}	CLK	Any A or B port	2	11	2	9	ns
t _{PHL}			3	14	3	12.5	
t _{PLH}	CLK	Q8	2	10.5	2	8	ns
t _{PHL}			3	11.5	3	10	
t _{PHZ}	S0, S1, S2	Any A or B port	2	9	2	7	ns
t _{PLZ}			3	13	3	10.5	
t _{PZH}			2	9	2	7	
t _{PZL}			3	13	3	10.5	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

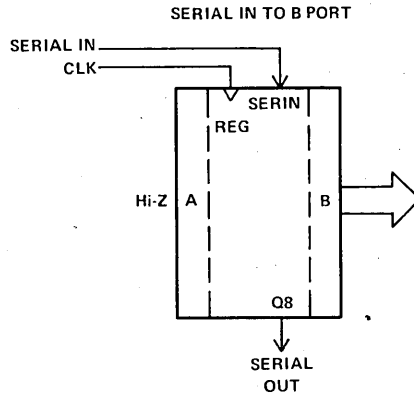
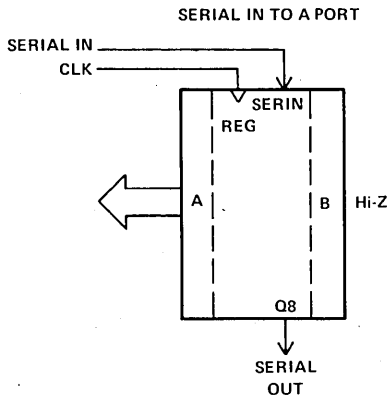
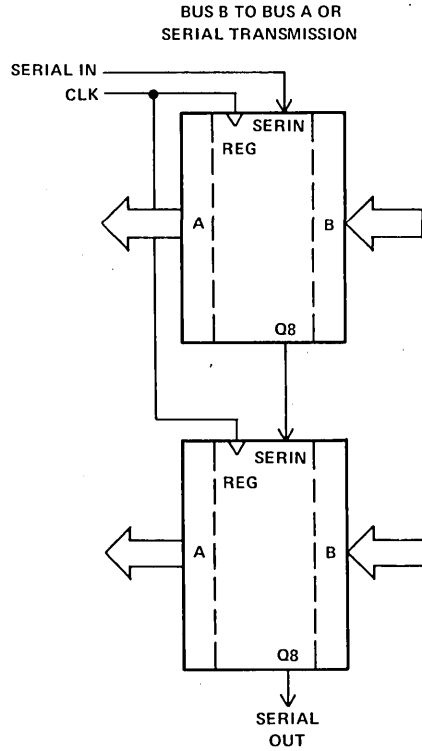
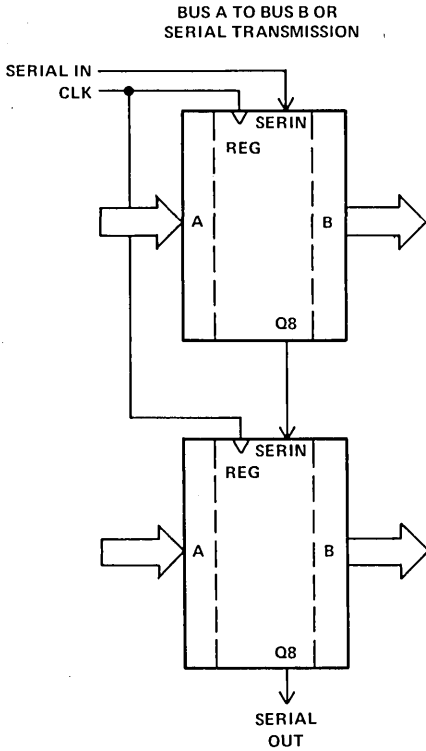
† The positive transition of S1 control pin will cause low-level data on the A or B bus to be invalid for 17.5 ns.

2
LSI Devices

SN54AS852, SN74AS852
8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

TYPICAL APPLICATION DATA

2
LSI Devices

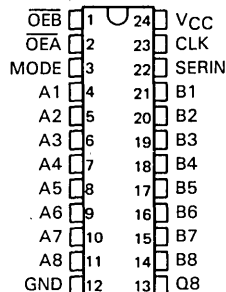


SN54AS856, SN74AS856 8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

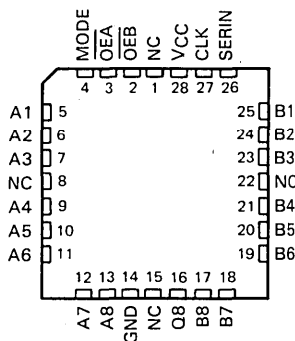
D2814, DECEMBER 1983—REVISED MARCH 1985

- Included Among the Package Options are Compact, 24-Pin, 300-mil-Wide DIPs and Both 28-Pin Plastic and Ceramic Chip Carriers
- Buffered 3-State Outputs Drive Bus Lines Directly
- Cascadable to n-Bits
- Eight Selectable Transceiver/Port Functions:
 - B to A
 - Register to A and/or B
 - Off-Line Shifts (A and B Ports in High-Impedance State)
 - Shifted to A and/or B
- Particularly Suitable for Use in Diagnostics Analysis Circuitry
- Serial Register Provides:
 - Parallel Storage of Either A or B Input Data
 - Serial Transmission of Data from Either A or B Port
 - Readback Mode B to A
- Dependable Texas Instruments Quality and Reliability

SN54AS856 . . . JT PACKAGE
SN74AS856 . . . DW or NT PACKAGE
(TOP VIEW)



SN54AS856 . . . FK PACKAGE
SN74AS856 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

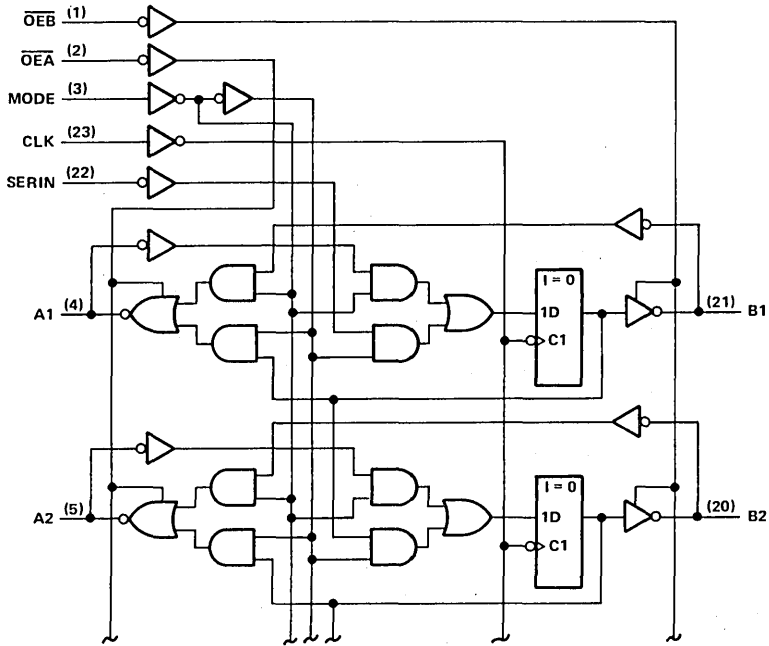
description

The 'AS856 features two 8-bit I/O ports (A1-A8 and B1-B8), an 8-bit parallel-load, serial-in, parallel-out shift register, and control logic. With these features, this device is capable of performing eight selectable transceiver or port functions, depending on the state of the three control lines \overline{OEA} , \overline{OEB} , and \overline{MODE} . These functions include: transferring data from port A to port B or vice versa (i.e., the transceiver function), serial shifting data to either or both ports, and performing off-line shifts (with A and B ports active as transceivers in a high-impedance state). Synchronous parallel loading of the internal register can be accomplished from either port on the positive transition of the clock while serially shifting data in via the SERIN input. The 'AS856 is ideally suited for applications needing signature-analysis circuitry to enhance system verification and/or fault analysis. All serial data is shifted right. All outputs are buffer-type outputs designed specifically to drive bus lines directly and all are 3-state except for Q8, which is a totem-pole output.

The SN54AS856 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AS856 is characterized for operation from 0°C to 70°C .

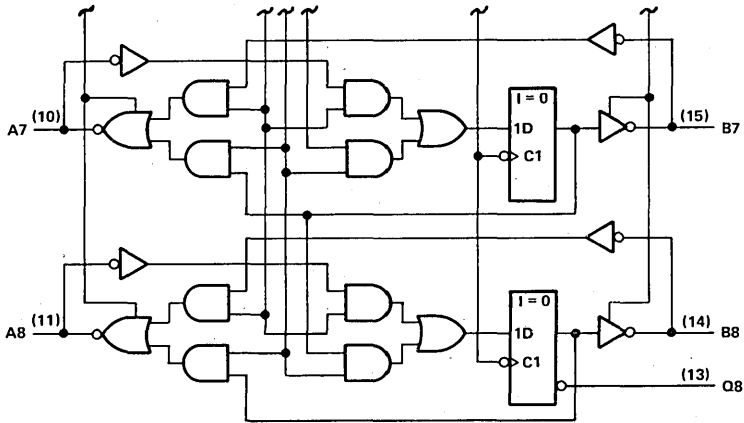
SN54AS856, SN74AS856
8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

logic diagram (positive logic)



FOUR IDENTICAL CHANNELS NOT SHOWN
 INPUTS/OUTPUTS NOT SHOWN:

- | | |
|--------|---------|
| (6) A3 | (19) B3 |
| (7) A4 | (18) B4 |
| (8) A5 | (17) B5 |
| (9) A6 | (16) B6 |



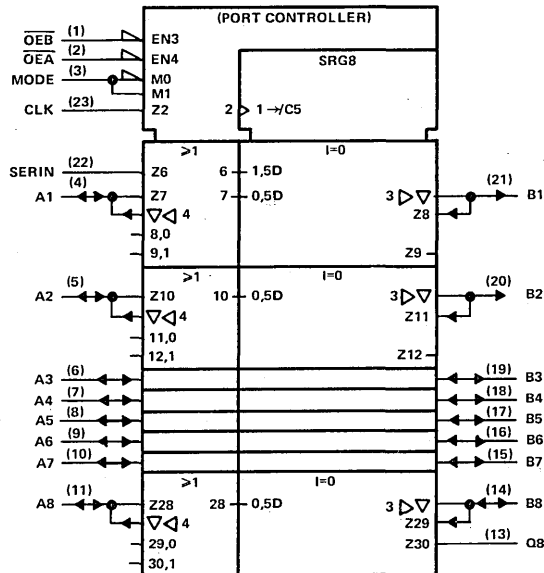
SN54AS856, SN74AS856 8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

FUNCTION TABLE

MODE			CLOCK	SERIN	A1 Q1 B1		A2 Q2 B2		A3 Q3 B3		A4 Q4 B4		A5 Q5 B5		A6 Q6 B6		A7 Q7 B7		A8 Q8 B8		FUNCTION
MODE	OEA	OEB																			
L	L	L	H or L	X	Q1 Q1 Q1	Q2 Q2 Q2	Q3 Q3 Q3	Q4 Q4 Q4	Q5 Q5 Q5	Q6 Q6 Q6	Q7 Q7 Q7	Q8 Q8 Q8	Q8 Q8 Q8	Q8 Q8 Q8	Q8 Q8 Q8	Q8 Q8 Q8	Q8 Q8 Q8	Q8 Q8 Q8	Q8 Q8 Q8	Q8 Q8 Q8	FEEDBACK
L	L	L	↑	X	Q1 Q1 Q1	Q2 Q2 Q2	Q3 Q3 Q3	Q4 Q4 Q4	Q5 Q5 Q5	Q6 Q6 Q6	Q7 Q7 Q7	Q8 Q8 Q8	Q8 Q8 Q8	Q8 Q8 Q8	Q8 Q8 Q8	Q8 Q8 Q8	Q8 Q8 Q8	Q8 Q8 Q8	Q8 Q8 Q8	Q8 Q8 Q8	FEEDBACK
L	L	H	H or L	X	B1 Q1 Z	B2 Q2 Z	B3 Q3 Z	B4 Q4 Z	B5 Q5 Z	B6 Q6 Z	B7 Q7 Z	B8 Q8 Z	B8 Q8 Z	B8 Q8 Z	B8 Q8 Z	B8 Q8 Z	B8 Q8 Z	B8 Q8 Z	B8 Q8 Z	B8 Q8 Z	B to A
L	L	H	↑	X	B1 B1 Z	B2 B2 Z	B3 B3 Z	B4 B4 Z	B5 B5 Z	B6 B6 Z	B7 B7 Z	B8 B8 Z	B8 B8 Z	B8 B8 Z	B8 B8 Z	B8 B8 Z	B8 B8 Z	B8 B8 Z	B8 B8 Z	B8 B8 Z	A to Q
L	H	L	H or L	X	Z Q1 Q1	Z Q2 Q2	Z Q3 Q3	Z Q4 Q4	Z Q5 Q5	Z Q6 Q6	Z Q7 Q7	Z Q8 Q8	Z Q8 Q8	Z Q8 Q8	Z Q8 Q8	Z Q8 Q8	Z Q8 Q8	Z Q8 Q8	Z Q8 Q8	Z Q8 Q8	A to Q
L	H	L	↑	X	Z A1 A1	Z A2 A2	Z A3 A3	Z A4 A4	Z A5 A5	Z A6 A6	Z A7 A7	Z A8 A8	Z A8 A8	Z A8 A8	Z A8 A8	Z A8 A8	Z A8 A8	Z A8 A8	Z A8 A8	Z A8 A8	Q to B
L	H	H	H or L	X	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	Z Q8 Z	Z Q8 Z	Z Q8 Z	Z Q8 Z	Z Q8 Z	Z Q8 Z	Z Q8 Z	Z Q8 Z	Z Q8 Z	A to Q
L	H	H	↑	X	Z A2 Z	Z A3 Z	Z A4 Z	Z A5 Z	Z A6 Z	Z A7 Z	Z A8 Z	Z A8 Z	Z A8 Z	Z A8 Z	Z A8 Z	Z A8 Z	Z A8 Z	Z A8 Z	Z A8 Z	Z A8 Z	A to Q
H	L	L	H or L	X	Q1 Q _n Q1	Q2 Q _n Q2	Q3 Q _n Q3	Q4 Q _n Q4	Q5 Q _n Q5	Q6 Q _n Q6	Q7 Q _n Q7	Q8 Q _n Q8	Q8 Q _n Q8	Q8 Q _n Q8	Q8 Q _n Q8	Q8 Q _n Q8	Q8 Q _n Q8	Q8 Q _n Q8	Q8 Q _n Q8	Q8 Q _n Q8	SHIFT
H	L	L	↑	H	H H H	Q1 Q1 Q1	Q2 Q2 Q2	Q3 Q3 Q3	Q4 Q4 Q4	Q5 Q5 Q5	Q6 Q6 Q6	Q7 Q7 Q7	Q8 Q8 Q8	Q8 Q8 Q8	Q8 Q8 Q8	Q8 Q8 Q8	Q8 Q8 Q8	Q8 Q8 Q8	Q8 Q8 Q8	Q8 Q8 Q8	TO
H	L	L	↑	L	L L L	Q1 Q1 Q1	Q2 Q2 Q2	Q3 Q3 Q3	Q4 Q4 Q4	Q5 Q5 Q5	Q6 Q6 Q6	Q7 Q7 Q7	Q8 Q8 Q8	Q8 Q8 Q8	Q8 Q8 Q8	Q8 Q8 Q8	Q8 Q8 Q8	Q8 Q8 Q8	Q8 Q8 Q8	Q8 Q8 Q8	A and B
H	L	H	H or L	X	Q1 Q _n Z	Q2 Q _n Z	Q3 Q _n Z	Q4 Q _n Z	Q5 Q _n Z	Q6 Q _n Z	Q7 Q _n Z	Q8 Q _n Z	Q8 Q _n Z	Q8 Q _n Z	Q8 Q _n Z	Q8 Q _n Z	Q8 Q _n Z	Q8 Q _n Z	Q8 Q _n Z	Q8 Q _n Z	SHIFT
H	L	H	↑	H	H H Z	Q1 Q1 Z	Q2 Q2 Z	Q3 Q3 Z	Q4 Q4 Z	Q5 Q5 Z	Q6 Q6 Z	Q7 Q7 Z	Q8 Q8 Z	Q8 Q8 Z	Q8 Q8 Z	Q8 Q8 Z	Q8 Q8 Z	Q8 Q8 Z	Q8 Q8 Z	Q8 Q8 Z	TO
H	L	H	↑	L	L L Z	Q1 Q1 Z	Q2 Q2 Z	Q3 Q3 Z	Q4 Q4 Z	Q5 Q5 Z	Q6 Q6 Z	Q7 Q7 Z	Q8 Q8 Z	Q8 Q8 Z	Q8 Q8 Z	Q8 Q8 Z	Q8 Q8 Z	Q8 Q8 Z	Q8 Q8 Z	Q8 Q8 Z	A
H	H	L	H or L	X	Z Q _n Q1	Z Q _n Q2	Z Q _n Q3	Z Q _n Q4	Z Q _n Q5	Z Q _n Q6	Z Q _n Q7	Z Q _n Q8	Z Q _n Q8	Z Q _n Q8	Z Q _n Q8	Z Q _n Q8	Z Q _n Q8	Z Q _n Q8	Z Q _n Q8	Z Q _n Q8	SHIFT
H	H	L	↑	H	Z H H	Z Q1 Q1	Z Q2 Q2	Z Q3 Q3	Z Q4 Q4	Z Q5 Q5	Z Q6 Q6	Z Q7 Q7	Z Q8 Q8	Z Q8 Q8	Z Q8 Q8	Z Q8 Q8	Z Q8 Q8	Z Q8 Q8	Z Q8 Q8	Z Q8 Q8	TO
H	H	L	↑	L	Z L L	Z Q1 Q1	Z Q2 Q2	Z Q3 Q3	Z Q4 Q4	Z Q5 Q5	Z Q6 Q6	Z Q7 Q7	Z Q8 Q8	Z Q8 Q8	Z Q8 Q8	Z Q8 Q8	Z Q8 Q8	Z Q8 Q8	Z Q8 Q8	Z Q8 Q8	B
H	H	H	H or L	X	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	SHIFT
H	H	H	↑	H	Z H Z	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	Z Q8 Z	Z Q8 Z	Z Q8 Z	Z Q8 Z	Z Q8 Z	Z Q8 Z	Z Q8 Z	Z Q8 Z	SHIFT
H	H	H	↑	L	Z L H	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	Z Q8 Z	Z Q8 Z	Z Q8 Z	Z Q8 Z	Z Q8 Z	Z Q8 Z	Z Q8 Z	Z Q8 Z	SHIFT

n = level of Q_n (n = 1, 2, . . . 8) established on most recent ↑ transition of CLK. Q1 through Q8 are the shift register outputs; only Q8 is available externally. The double inversions that take place as data travels from port to port are ignored in this table.

logic symbol†



Pin numbers shown are for DW, JT, and NT packages.

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54AS856, SN74AS856

8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

absolute maximum ratings over free-air temperature range

Supply voltage, V_{CC}	7 V
Input voltage: All inputs	7 V
I/O ports	5.5 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range: SN54AS856	-55°C to 125°C
SN74AS856	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54AS856			SN74AS856			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage	0.8			0.8			V
I_{OH}	High-level output current	A1-A8, B1-B8		-12	-15		mA	
		Q8		-2	-2			
I_{OL}	Low-level output current	A1-A8, B1-B8		32	48		mA	
		Q8		20	20			
f_{clock}	Clock frequency	0	45	0	50	MHz		
t_w	Duration of clock pulse	11			10			ns
t_{su}	Setup time before CLK↑	A1-A8, B1-B8 SERIN		5.5	5.5		ns	
		$\overline{OE}B, \overline{OE}A, MODE$		5.5	5.5			
t_h	Hold-time, data after CLK↑	A1-A8, B1-B8 SERIN		0	0		ns	
		$\overline{OE}B, \overline{OE}A, MODE$		0	0			
T_A	Operating free-air temperature	-55	125	0	70	°C		

SN54AS856, SN74AS856 8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

electrical characteristics over recommended operating free-air temperature range
(unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS856		SN74AS856		UNIT	
		MIN	TYP†	MAX	MIN		TYP†
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2		-1.2	V
V _{OH}	A1-A8 B1-B8	V _{CC} = 4.5 V, I _{OH} = -12 mA	2	3.2			V
		V _{CC} = 4.5 V, I _{OH} = -15 mA			2	3.3	
	All outputs	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -2 mA	V _{CC} -2		V _{CC} -2		
V _{OL}	All outputs except Q8	V _{CC} = 4.5 V, I _{OL} = 32 mA	0.25	0.5			V
		V _{CC} = 4.5 V, I _{OL} = 48 mA			0.35	0.5	
	Q8	V _{CC} = 4.5 V, I _{OL} = 20 mA		0.5		0.5	
I _I	OE _B , OE _A , MODE CLK and SERIN	V _{CC} = 5.5 V, V _I = 7 V		0.2		0.2	mA
				0.1		0.1	
	A1-A8, B1-B8	V _{CC} = 5.5 V, V _I = 5.5 V		0.2		0.2	
I _{IH}	OE _B , OE _A , MODE CLK and SERIN	V _{CC} = 5.5 V, V _I = 2.7 V		40		40	μA
				20		20	
	A1-A8, B1-B8†			70		70	
I _{IL}	OE _B , OE _A , MODE CLK and SERIN	V _{CC} = 5.5 V, V _I = 0.4 V		-1		-1	mA
				-0.5		-0.5	
	A1-A8, B1-B8†			-0.5		-0.5	
I _O ‡	Except Q8	V _{CC} = 5.5 V, V _O = 2.25 V	-30	-112	-30	-112	mA
	Q8		-20	-112	-20	-112	
I _{CC}	V _{CC} = 5.5 V		118	200	118	200	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡For I/O ports, the parameters I_{IH} and I_{IL} include the output currents I_{OZH} and I_{OZL}, respectively.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_OS.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX				UNIT
			SN54AS856		SN74AS856		
			MIN	MAX	MIN	MAX	
f _{max}			45		50	MHz	
t _{PLH}	Any B port	Any A port	2	8	2	7	ns
t _{PHL}			2	10.5	2	9.5	
t _{PLH}	↑MODE†	Any A or B port	2	8.5	2	7.5	ns
t _{PHL}			5	20	5	19	
t _{PLH}	↓MODE	Any A or B port	2	8.5	2	7.5	ns
t _{PHL}			2	9.5	2	8	
t _{PLH}	CLK	Any A or B port	3	12	3	9	ns
t _{PHL}			3	12	3	11	
t _{PLH}	CLK	Q8	2	9	2	7.5	ns
t _{PHL}			2	10	2	9	
t _{PHZ}	OE _A or OE _B	Any A or B port	2	9	2	7	ns
t _{PLZ}			2	12	2	9.5	
t _{PZH}			2	8	2	7	
t _{PZL}			2	11	2	10	

†The positive transition of the MODE control will cause low-level data at the A output Bus or stored in Q to be invalid for 12 ns.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

2

LSI Devices

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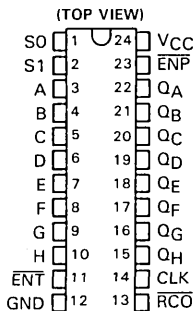
LSI Devices

SN54AS867, SN54AS869, SN74AS867, SN74AS869 SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

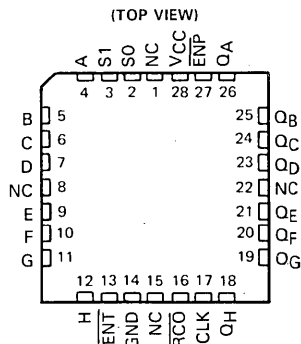
D2661, DECEMBER 1982—AUGUST 1985

- Included among the Package Options are Compact, 24-Pin, 300-mil-Wide DIPs and 28-Pin Ceramic Chip Carriers
- Fully Programmable with Synchronous Counting and Loading
- 'AS867 Has Asynchronous Clear, 'AS869 Has Synchronous Clear
- Fully Independent Clock Circuit Simplifies Use
- Ripple Carry Output for n-Bit Cascading
- Improved Performance Compared to Schottky TTL:
 - Typical Power Reduced by 38%
 - Maximum Count Frequency is 25% Higher
- Dependable Texas Instruments Quality and Reliability

SN54AS867, SN54AS869 JT PACKAGE
SN74AS867, SN74AS869 DW OR NT PACKAGE



SN54AS867, SN54AS869 FK PACKAGE



NC—No internal connection

description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the eight flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load mode circuitry allows parallel loading of the cascaded counters. As loading is synchronous, selecting the load mode disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs (ENP and ENT) must be low to count. The direction of the count is determined by the levels of the select inputs (see Function Table). Input ENT is fed forward to enable the carry output. The ripple carry output thus enabled will produce a low-level pulse while the count is zero (all outputs low) counting down or 255 counting up (all outputs high). This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable ENP and ENT inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

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TEXAS
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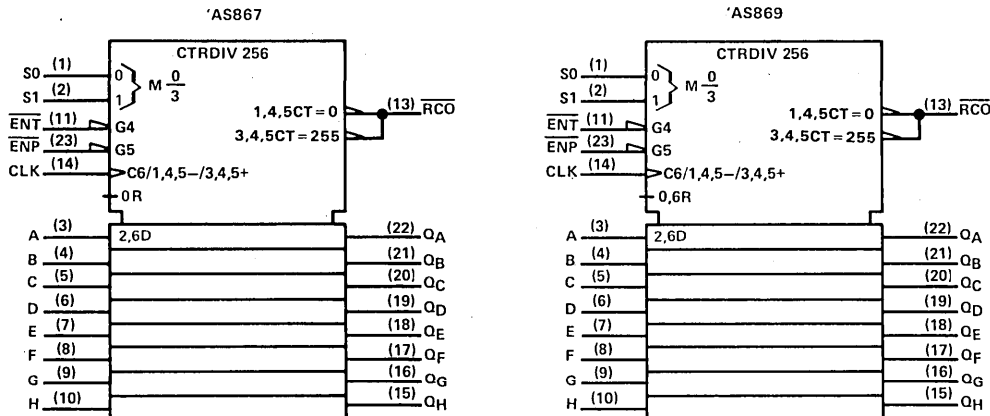
LSI Devices

SN54AS867, SN54AS869, SN74AS867, SN74AS869 SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

These counters feature a fully independent clock circuit. With the exception of the asynchronous clear on the 'AS867, changes at control inputs (S0, S1) that will modify the operating mode have no effect on the Q outputs until clocking occurs. Anytime the $\overline{\text{ENP}}$ and/or $\overline{\text{ENT}}$ is taken high, $\overline{\text{RCO}}$ will either go or remain high. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

The SN54AS867 and SN54AS869 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AS867 and SN74AS869 are characterized for operation from 0°C to 70°C .

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.

FUNCTION TABLE

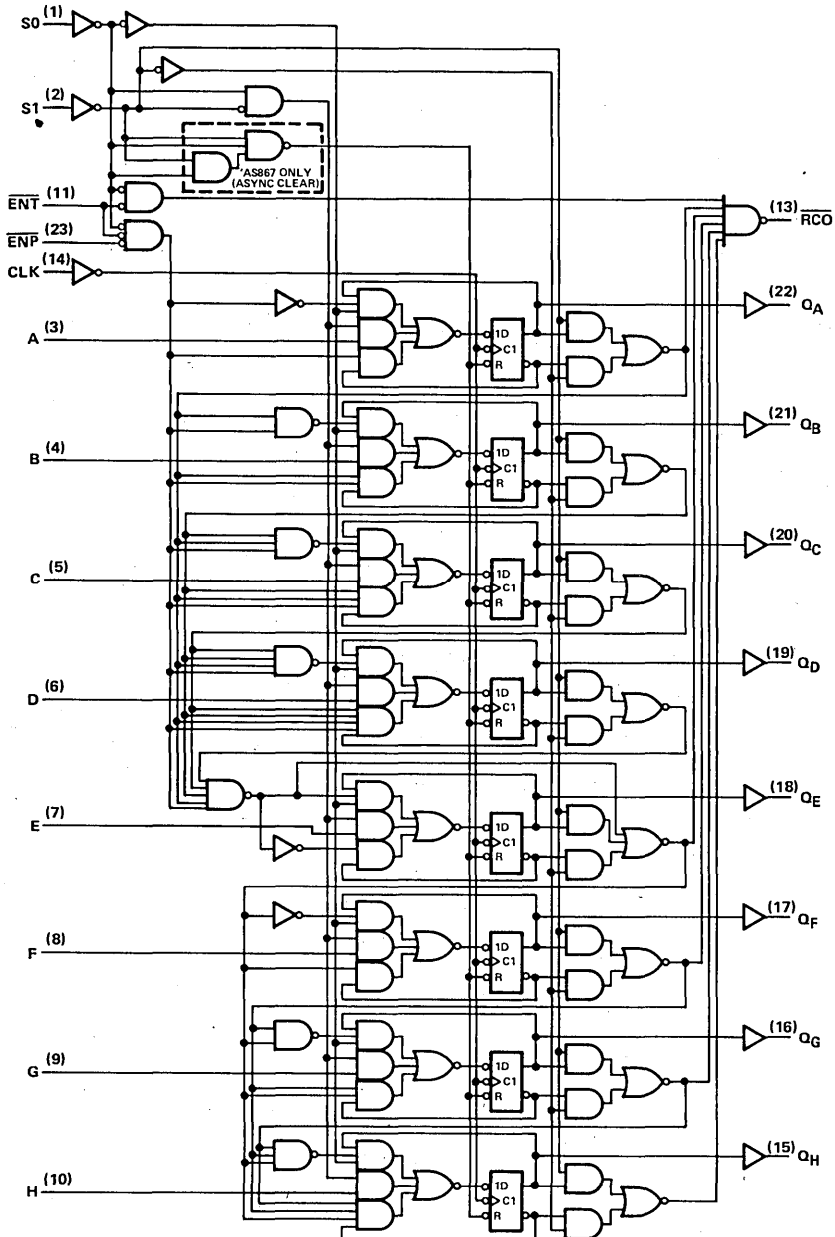
S1	S0	FUNCTION
L	L	Clear
L	H	Count down
H	L	Load
H	H	Count up

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Operating free-air temperature range: SN54AS867, SN54AS869	-55°C to 125°C
SN74AS867, SN74AS869	0°C to 70°C
Storage temperature range	-65°C to 150°C

SN54AS867, SN54AS869, SN74AS867, SN74AS869
 SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

2
 LSI Devices

SN54AS867, SN74AS867

SYNCHRONOUS 8-BIT UP/DOWN COUNTERS WITH ASYNCHRONOUS CLEAR

recommended operating conditions

		SN54AS867			SN74AS867			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage				0.8			V
I _{OH}	High-level output current				-2			mA
I _{OL}	Low-level output current				20			mA
f _{clock}	Clock frequency	0	40		0	50		MHz
t _{w(clock)}	Duration	12.5			10			ns
t _{w(clear)}	Duration of clear pulse (S0 and S1 low)	12.5			10			ns
t _{su}	Setup time †	Data inputs A-H		5	4		ns	
		Enable P (ENP) or Enable T (ENT)		9	8		ns	
		S0 or S1 (load)		11	10		ns	
		S0 or S1 (clear)		11	10		ns	
		S0 or S1 (count down)		42	40		ns	
		S0 or S1 (count up)		42	40		ns	
t _h	Hold time at any input with respect to clock †	0			0			ns
t _{skew}	Skew time between S0 and S1 (maximum to avoid inadvertent clear)	8			7			ns
T _A	Operating free-air temperature	-55	125		0	70		°C

† This setup time is required to ensure stable data.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS867		SN74AS867		UNIT
				MIN	TYP †	MAX	MIN	
V _{IK}		V _{CC} = 4.5 V, I _I = 18 mA		-1.2		-1.2		V
V _{OH}		V _{CC} = 4.5 V to 5.5 V, I _{OH} = -2 mA		V _{CC} - 2		V _{CC} - 2		V
V _{OL}		V _{CC} = 4.5 V, I _{OL} = 20 mA		0.34	0.5	0.34	0.5	V
I _I		V _{CC} = 5.5 V, V _I = 7 V		0.1		0.1		mA
I _{IH}	ENT	V _{CC} = 5.5 V, V _I = 2.7 V		40		40		μA
	Other inputs			20		20		
I _{IL}	ENT	V _{CC} = 5.5 V, V _I = 0.4 V		-4		-4		mA
	Other inputs			-2		-2		
I _O §		V _{CC} = 5.5 V, V _O = 2.25 V		-30	-112	-30	-112	mA
I _{CC}		V _{CC} = 5.5 V		134	195	134	195	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

2

LSI Devices

SN54AS869, SN74AS869
SYNCHRONOUS 8-BIT UP/DOWN COUNTERS WITH SYNCHRONOUS CLEAR

recommended operating conditions

		SN54AS869			SN74AS869			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage	0.8			0.8			V
I _{OH}	High-level output current	-2			-2			mA
I _{OL}	Low-level output current	20			20			mA
f _{clock}	Clock frequency	0			40			MHz
t _{w(clock)}	Duration	12.5			11			ns
t _{su}	Setup time†	Data inputs A-H		6		5		ns
		Enable P (ENP) or Enable T (ENT)		10		9		ns
		S0 or S1 (load)		13		11		ns
		S0 or S1 (clear)		13		11		ns
		S0 or S1 (count down)		52		50		ns
S0 or S1 (count up)		52		50		ns		
t _h	Hold time at any input with respect to clock†	0			0			ns
T _A	Operating free-air temperature	-65		125		0		70 °C

†This setup time is required to ensure stable data.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54AS869		SN74AS869		UNIT
			MIN	TYP‡	MAX	MIN	
V _{IK}		V _{CC} = 4.5 V, I _I = 18 mA	-1.2		-1.2		V
V _{OH}		V _{CC} = 4.5 V to 5.5 V, I _{OH} = -2 mA	V _{CC} -2		V _{CC} -2		V
V _{OL}		V _{CC} = 4.5 V, I _{OL} = 20 mA	0.34	0.5	0.34	0.5	V
I _I		V _{CC} = 5.5 V, V _I = 7 V	0.1		0.1		mA
I _{IH}	ENT	V _{CC} = 5.5 V, V _I = 2.7 V	40		40		μA
	Other inputs		20		20		
I _{IL}	ENT	V _{CC} = 5.5 V, V _I = 0.4 V	-4		-4		mA
	Other inputs		-2		-2		
I _O §		V _{CC} = 5.5 V, V _O = 2.25 V	-30	-112	-30	-112	mA
I _{CC}		V _{CC} = 5.5 V	125	180	125	180	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{O5}.

2

LSI Devices

SN54AS867, SN54AS869, SN74AS867, SN74AS869
SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

'AS867 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO OUTPUT	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX				UNIT
			SN54AS867		SN74AS867		
			MIN	MAX	MIN	MAX	
f _{max}			40		50	MHz	
t _{PLH}	CLK	$\overline{\text{RCO}}$	5	31	5	22	ns
t _{PHL}			6	19	6	16	
t _{PLH}	CLK	Any Q	3	12	3	11	ns
t _{PHL}			4	16	4	15	
t _{PLH}	$\overline{\text{ENT}}$	$\overline{\text{RCO}}$	3	19	3	10	ns
t _{PHL}			5	21	5	17	
t _{PLH}	$\overline{\text{ENP}}$	$\overline{\text{RCO}}$	5	14	5	14	ns
t _{PHL}			5	21	5	17	
t _{PHL}	Clear (S ₀ , S ₁ low)	Any Q	7	23	7	21	ns

'AS869 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX				UNIT
			SN54AS869		SN74AS869		
			MIN	MAX	MIN	MAX	
f _{max}			40		45	MHz	
t _{PLH}	CLK	$\overline{\text{RCO}}$	6	35	6	35	ns
t _{PHL}			6	20	6	18	
t _{PLH}	CLK	Any Q	3	12	3	11	ns
t _{PHL}			4	16	4	15	
t _{PLH}	$\overline{\text{ENT}}$	$\overline{\text{RCO}}$	3	25	3	15	ns
t _{PHL}			6	21	6	17	
t _{PLH}	$\overline{\text{ENP}}$	$\overline{\text{RCO}}$	5	27	5	19	ns
t _{PHL}			6	21	6	18	

NOTE 1: Load circuit and voltage waveforms, are shown in Section 1.

2

LSI Devices

SN54AS870, SN54AS871, SN74AS870, SN74AS871 DUAL 16-BY-4 REGISTER FILES

D2661, DECEMBER 1982—REVISED JANUARY 1986

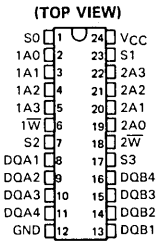
- 'AS870 in 24-Pin Small Outline, 300-mil DIP and Both Plastic and Ceramic 28-Pin Chip Carriers
- 'AS871 in 28-Pin 600-mil DIP and Both Plastic and Ceramic Chip Carriers
- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Typical Access Time is 11 ns
- Each Register File Has Individual Write Enable Controls and Address Lines
- Designed Specifically for Multibus Architecture and Overlapping File Operations
- Prioritized B Input Port Prevents Write Conflicts During Dual Input Mode
- Dependable Texas Instruments Quality and Reliability

description

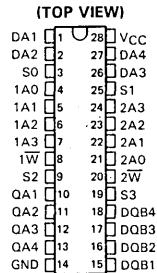
These devices feature two 16-word by 4-bit register files. Each register file has individual write-enable controls and address lines. The 'AS870 has two 4-bit data I/O ports (DQA1-DQA4 and DQB1-DQB4). The 'AS871 has one 4-bit data I/O port (DQB1-DQB4) with the other data port having individual data inputs (DA1-DA4) and data outputs (QA1-QA4). The data I/O ports can output to Bus A and Bus B; receive input from Bus A and Bus B, receive input from Bus A and output to Bus B, or output to Bus A and receive input from Bus B. To prevent writing conflicts in the dual-input mode, the B input port takes priority. Two select lines, S0 and S1, control which port has access to which register. S2 determines whether the A ports are in the input or the output modes and S3 does likewise for the B ports. The address lines (1A0-1A3 or 2A0-2A3) are decoded by an internal 1-of-16 decoder to select which register word is to be accessed. All outputs are 3-state buffer-type outputs designed specifically to drive bus lines directly.

The SN54AS870 and SN54AS871 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74AS870 and SN74AS871 are characterized for operation from 0°C to 70°C.

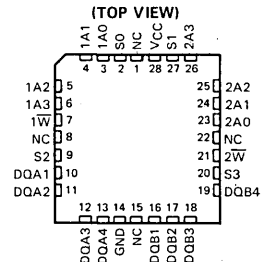
SN54AS870 . . . JT PACKAGE
SN74AS870 . . . DW OR NT PACKAGE



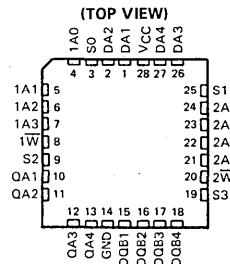
SN54AS871 . . . JD PACKAGE
SN74AS871 . . . N PACKAGE



SN54AS870 . . . FK PACKAGE
SN74AS870 . . . FN PACKAGE



SN54AS871 . . . FK PACKAGE
SN74AS871 . . . FN PACKAGE



NC—No internal connection

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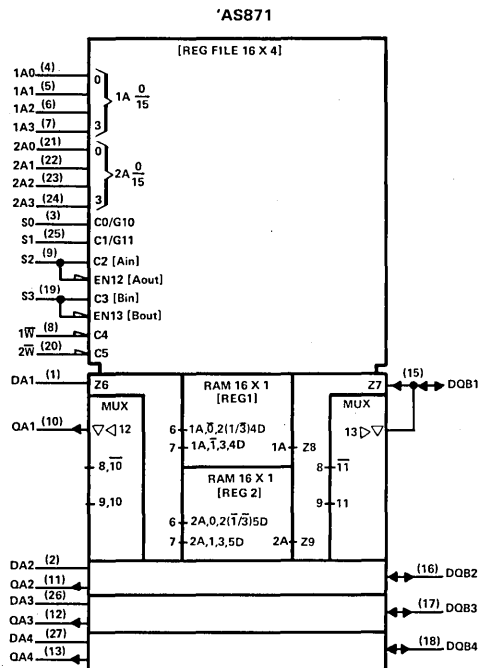
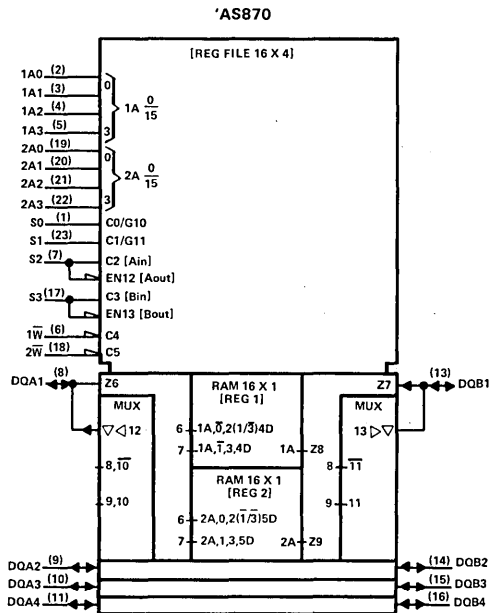
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SN54AS870, SN54AS871, SN74AS870, SN74AS871

DUAL 16-BY-4 REGISTER FILES

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

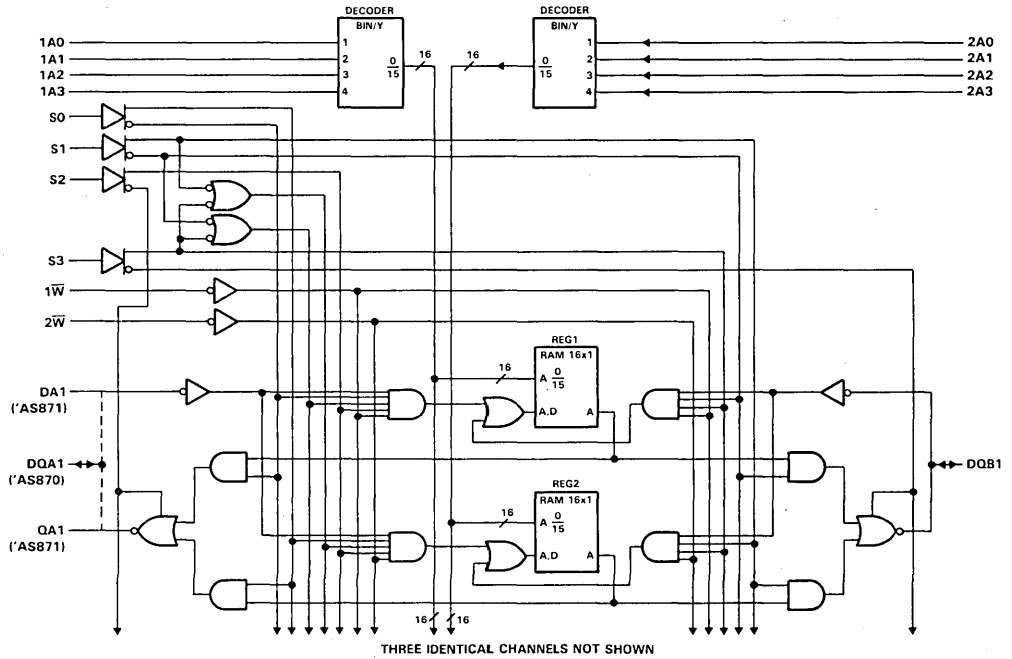
Pin numbers shown are for DW, JT, and NT packages.

2

LSI Devices

SN54AS870, SN54AS871, SN74AS870, SN74AS871
 DUAL 16-BY-4 REGISTER FILES

logic diagram (positive logic)



2
 LSI Devices

SN54AS870, SN54AS871, SN74AS870, SN74AS871
DUAL 16-BY-4 REGISTER FILES

FUNCTION TABLE

FILE SELECT			INPUT/OUTPUT		
S0	S1	FILE SEL	S2	S3	I/O SEL
L	L	1R TO A, 1R TO B	L	L	A OUT, B OUT
H	L	2R TO A, 1R TO B			
L	H	1R TO A, 2R TO B			
H	H	2R TO A, 2R TO B			
L	L	A TO 1R, 1R TO B	H	L	A IN, B OUT
H	L	A TO 2R, 1R TO B			
L	H	A TO 1R, 2R TO B			
H	H	A TO 2R, 2R TO B			
L	L	1R TO A, B TO 1R	L	H	A OUT, B IN
H	L	2R TO A, B TO 1R			
L	H	1R TO A, B TO 2R			
H	H	2R TO A, B TO 2R			
L	L	B TO 1R	H	H	A IN, B IN
H	L	A TO 2R, B TO 1R			
L	H	A TO 1R, B TO 2R			
H	H	B TO 2R			

2

LSI Devices

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage: All inputs	7 V
I/O ports	5.5 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range: SN54AS870, SN54AS871	-55°C to 125°C
SN74AS870, SN74AS871	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54AS870 SN54AS871			SN74AS870 SN74AS871			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX		
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
V _{IH}	High-level input voltage	2			2			V	
V _{IL}	Low-level input voltage				0.8			V	
I _{OH}	High-level output current				-15			mA	
I _{OL}	Low-level output current				48			mA	
t _w	Duration of write pulse	12			12			ns	
t _{su}	Setup times	Address before write†		5		5		ns	
		Data before write†		15		15			
		Select before write†		12		12			
t _h	Hold times	Address after write†		0		0		ns	
		Data after write†		0		0			
		Select after write†		12		12			
T _A	Operating free-air temperature	-55		125		0		70	°C

SN54AS870, SN54AS871, SN74AS870, SN74AS871 DUAL 16-BY-4 REGISTER FILES

¹AS870 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS870		SN74AS870		UNIT
		MIN	TYP [†] MAX	MIN	TYP [†] MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA		-1.2		-1.2	V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -2 mA	V _{CC} - 2		V _{CC} - 2		V
	V _{CC} = 4.5 V, I _{OH} = -12 mA	2.4	3.2			
	V _{CC} = 4.5 V, I _{OH} = -15 mA			2.4	3.2	
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 32 mA	0.25	0.5			V
	V _{CC} = 4.5 V, I _{OL} = 48 mA			0.35	0.5	
I _I	Control inputs	V _{CC} = 5.5 V, V _I = 7 V		0.1		mA
	DQA and DQB ports	V _{CC} = 5.5 V, V _I = 5.5 V		0.2		
I _{IH}	1 \bar{W} and 2 \bar{W}			20		μ A
	Other control inputs	V _{CC} = 5.5 V, V _I = 2.7 V		40		
	DQA and DQB ports [‡]			50		
I _{IL}	Control inputs	V _{CC} = 5.5 V, V _I = 0.4 V		-2		mA
	DQA and DQB ports [‡]			-2		
I _O [§]	V _{CC} = 5.5 V, V _O = 2.25 V	-30	-112	-30	-112	mA
I _{CC}	V _{CC} = 5.5 V	120	190	120	190	mA

¹AS871 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS871		SN74AS871		UNIT
		MIN	TYP [†] MAX	MIN	TYP [†] MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA		-1.2		-1.2	V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -2 mA	V _{CC} - 2		V _{CC} - 2		V
	V _{CC} = 4.5 V, I _{OH} = -12 mA	2.4	3.2			
	V _{CC} = 4.5 V, I _{OH} = -15 mA			2.4	3.2	
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 32 mA	0.25	0.5			V
	V _{CC} = 4.5 V, I _{OL} = 48 mA			0.35	0.5	
I _{OZH}	QA outputs	V _{CC} = 5.5 V, V _O = 2.7 V		50		μ A
I _{OZL}	QA outputs	V _{CC} = 5.5 V, V _O = 0.4 V		-50		μ A
I _I	Control and DA inputs	V _{CC} = 5.5 V, V _I = 7 V		0.1		mA
	DQB ports	V _{CC} = 5.5 V, V _I = 5.5 V		0.2		
I _{IH}	1 \bar{W} , 2 \bar{W} , and DA inputs			20		μ A
	Other control inputs	V _{CC} = 5.5 V, V _I = 2.7 V		40		
	DQB ports [‡]			50		
I _{IL}	Control and DA inputs	V _{CC} = 5.5 V, V _I = 0.4 V		-2		mA
	DQB ports [‡]			-2		
I _O [§]	V _{CC} = 5.5 V, V _O = 2.25 V	-30	-112	-30	-112	mA
I _{CC}	V _{CC} = 5.5 V	120	190	120	190	mA

[†]All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡]For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§]The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

2

LSI Devices

SN54AS870, SN54AS871, SN74AS870, SN74AS871
DUAL 16-BY-4 REGISTER FILES

'AS870 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $R_1 = 500 \Omega$, $R_2 = 500 \Omega$, $T_A = \text{MIN to MAX}$				UNIT
			SN54AS870		SN74AS870		
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Any A	Any DQ	5	20	5	15	ns
$t_{a(S)}$	SO	Any DQA	3	15	3	13	ns
	S1	Any DQB	3	15	3	13	
t_{dis}	S2	Any DQA	3	12	3	11	ns
	S3	Any DQB	3	12	3	11	
t_{en}	S2	Any DQA	3	15	3	12	ns
	S3	Any DQB	3	15	3	12	
t_{pd}	\bar{W}	Any DQ	5	23	5	19	ns
	DQA	DQB	5	25	5	22	
	DQB	DQA	5	25	5	22	

2

LSI Devices

'AS871 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $R_1 = 500 \Omega$, $R_2 = 500 \Omega$, $T_A = \text{MIN to MAX}$				UNIT
			SN54AS871		SN74AS871		
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Any A	Any QA or DQB	5	20	5	16	ns
$t_{a(S)}$	SO	Any QA	3	15	3	13	ns
	S1	Any DQB	3	15	3	13	
t_{dis}	S2	Any QA	3	12	3	11	ns
	S3	Any DQB	3	12	3	11	
t_{en}	S2	Any QA	3	15	3	12	ns
	S3	Any DQB	3	15	3	12	
t_{pd}	\bar{W}	Any QA or DQB	5	23	5	19	ns
	DA	DQB	5	26	5	23	
	DQB	QA	5	26	5	23	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54AS877, SN74AS877 8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

D2661, DECEMBER 1982—REVISED AUGUST 1985

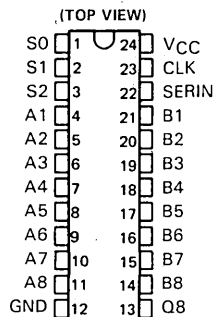
- Included Among the Package Options are Compact, 24-Pin, 300-mil-Wide Dips and Both 28-Pin Plastic and Ceramic Chip Carriers
- Buffered 3-State Outputs Drive Bus Lines Directly
- Cascaded to n-Bits
- Eight Selectable Transceiver/Port Functions:
 - A to B or B to A
 - Register to A or Register to B
 - Shifted to A or Shifted to B
 - Off-Line Shifts (A and B Ports in High-Impedance State)
 - Register Clear
- Particularly Suitable for Use in Signature-Analysis Circuitry
- Serial Register Provides:
 - Parallel Storage of Either A or B Input Data
 - Serial Transmission of Data from Either A or B Port
- Dependable Texas Instruments Quality and Reliability

description

The 'AS877 features two 8-bit I/O ports (A1-A8 and B1-B8), an 8-bit parallel-load, serial-in, parallel-out shift register, and control logic. With these features, this device is capable of performing eight selectable transceiver or port functions, depending on the state of the three select lines S0, S1, and S2. These functions include: transferring data from port A to port B or vice versa (i.e., the transceiver function), transferring data from the register to either port, serial shifting data to either port, performing off-line shifts (with A and B ports in high-impedance state), and clearing the register. Synchronous parallel loading of the internal register can be accomplished from either port on the positive transition of the clock while serially shifting data in via the SERIN input. The 'AS877 is ideally suited for applications needing signature-analysis circuitry to enhance system verification and/or fault analysis. All serial data is shifted right. All outputs are buffer-type outputs designed specifically to drive bus lines directly and all are 3-state except for Q8, which is a totem-pole output.

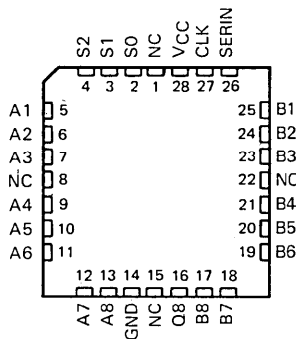
The SN54AS877 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AS877 is characterized for operation from 0°C to 70°C .

SN54AS877 . . . JT PACKAGE
SN74AS877 . . . DW OR NT PACKAGE



SN54AS877 . . . FK PACKAGE
SN74AS877 . . . FN PACKAGE

(TOP VIEW)



NC—No internal connection

2

LSI Devices

SN54AS877, SN74AS877

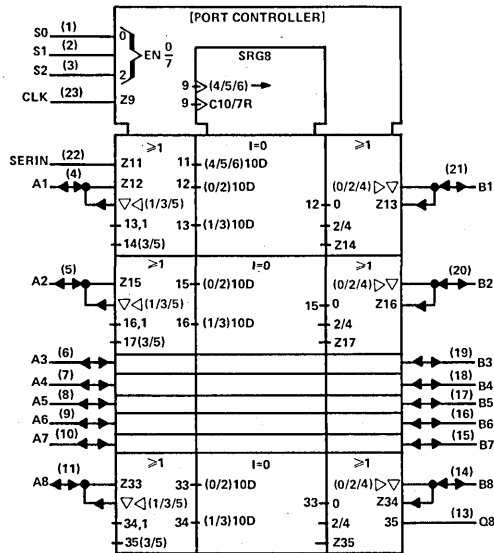
8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

FUNCTION TABLE

MODE S2 S1 S0	CLOCK	SERIN	A1 Q1 B1	A2 Q2 B2	A3 Q3 B3	A4 Q4 B4	A5 Q5 B5	A6 Q6 B6	A7 Q7 B7	A8 Q8 B8	PORT FUNCTION
L L L	H or L	X	Z Q _n A1	Z Q _n A2	Z Q _n A3	Z Q _n A4	Z Q _n A5	Z Q _n A6	Z Q _n A7	Z Q _n A8	A TO B
L L L	↑	X	Z A1 A1	Z A2 A2	Z A3 A3	Z A4 A4	Z A5 A5	Z A6 A6	Z A7 A7	Z A8 A8	
L L H	H or L	X	B1 Q _n Z	B2 Q _n Z	B3 Q _n Z	B4 Q _n Z	B5 Q _n Z	B6 Q _n Z	B7 Q _n Z	B8 Q _n Z	B TO A
L L H	↑	X	B1 B1 Z	B2 B2 Z	B3 B3 Z	B4 B4 Z	B5 B5 Z	B6 B6 Z	B7 B7 Z	B8 B8 Z	
L H L	H or L	X	X Q _n Q1	X Q _n Q2	X Q _n Q3	X Q _n Q4	X Q _n Q5	X Q _n Q6	X Q _n Q7	X Q _n Q8	Q _N TO B _N
L H L	↑	X	Z A1 A1	Z A2 A2	Z A3 A3	Z A4 A4	Z A5 A5	Z A6 A6	Z A7 A7	Z A8 A8	
L H H	H or L	X	Q1 Q _n X	Q2 Q _n X	Q3 Q _n X	Q4 Q _n X	Q5 Q _n X	Q6 Q _n X	Q7 Q _n X	Q8 Q _n X	Q _N TO A _N
L H H	↑	X	B1 B1 Z	B2 B2 Z	B3 B3 Z	B4 B4 Z	B5 B5 Z	B6 B6 Z	B7 B7 Z	B8 B8 Z	
H L L	H or L	X	Z Q _n Q1	Z Q _n Q2	Z Q _n Q3	Z Q _n Q4	Z Q _n Q5	Z Q _n Q6	Z Q _n Q7	Z Q _n Q8	SHIFT TO B
H L L	↑	H	Z H H	Z Q1 Q1	Z Q2 Q2	Z Q3 Q3	Z Q4 Q4	Z Q5 Q5	Z Q6 Q6	Z Q7 Q7	
H L L	↑	L	Z L L	Z Q1 Q1	Z Q2 Q2	Z Q3 Q3	Z Q4 Q4	Z Q5 Q5	Z Q6 Q6	Z Q7 Q7	
H L H	H or L	X	Q1 Q _n Z	Q2 Q _n Z	Q3 Q _n Z	Q4 Q _n Z	Q5 Q _n Z	Q6 Q _n Z	Q7 Q _n Z	Q8 Q _n Z	SHIFT TO A
H L H	↑	H	H H Z	Q1 Q1 Z	Q2 Q2 Z	Q3 Q3 Z	Q4 Q4 Z	Q5 Q5 Z	Q6 Q6 Z	Q7 Q7 Z	
H L H	↑	L	L L Z	Q1 Q1 Z	Q2 Q2 Z	Q3 Q3 Z	Q4 Q4 Z	Q5 Q5 Z	Q6 Q6 Z	Q7 Q7 Z	
H H L	H or L	X	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	SHIFT
H H L	↑	H	Z H Z	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	
H H L	↑	L	Z L Z	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	
H H H	H or L	X	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	Z Q _n Z	CLEAR
H H H	↑	X	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	

n = level of Q_n (n = 1, 2, ...8) established on most recent ↑ transition of CLK. Q1 thru Q8 are the shift register outputs; only Q8 is available externally. The double inversions that take place as data travels from port to port are ignored in this table.

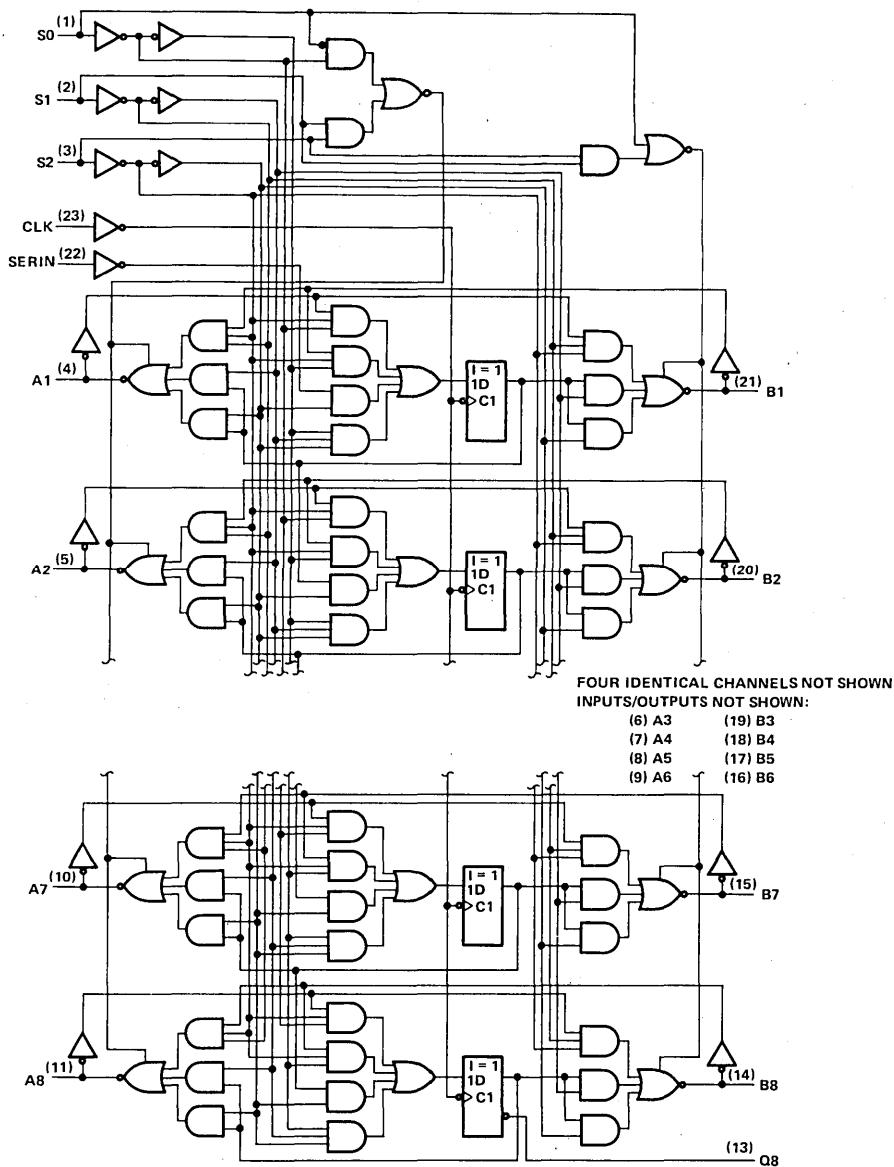
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.

SN54AS877, SN74AS877 8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

2
LSI Devices

SN54AS877, SN74AS877

8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

absolute maximum ratings over free-air temperature range

Supply voltage, V_{CC}	7 V
Input voltage: All inputs	7 V
I/O ports	5.5 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range: SN54AS877	-55°C to 125°C
SN74AS877	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54AS877			SN74AS877			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage	0.8			0.8			V
I_{OH}	High-level output current	A1-A8, B1-B8		-12	-15		mA	
		Q8		-2	-2			
I_{OL}	Low-level output current	A1-A8, B1-B8		32	48		mA	
		Q8		20	20			
f_{clock}	Clock frequency	0	45	0	50		MHz	
t_w	Duration of clock pulse	11			10			ns
t_{su}	Setup time before CLK†	A1-A8, B1-B8 SERIN		5.5	5.5		ns	
		S0, S1, S2		5.5	5.5			
t_h	Hold time, data after CLK†	A1-A8, B1-B8 SERIN		0	0		ns	
		S0, S1, S2		0	0			
T_A	Operating free-air temperature	-55	125	0	70		°C	

2
LSI Devices

SN54AS877, SN74AS877

8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS877		SN74AS877		UNIT
				MIN	TYP†	MAX	MIN	
V _{IK}		V _{CC} = 4.5 V,	I _I = -18 mA	-1.2		-1.2		V
V _{OH}	A1-A8 B1-B8	V _{CC} = 4.5 V,	I _{OH} = -12 mA	2	3.2			V
		V _{CC} = 4.5 V,	I _{OH} = -15 mA			2	3.3	
All outputs		V _{CC} = 4.5 V to 5.5 V, I _{OH} = -2 mA		V _{CC} - 2		V _{CC} - 2		
V _{OL}	All outputs except Q8	V _{CC} = 4.5 V,	I _{OL} = 32 mA	0.25	0.5			V
		V _{CC} = 4.5 V,	I _{OL} = 48 mA			0.35	0.5	
	Q8	V _{CC} = 4.5 V,	I _{OL} = 20 mA	0.25	0.5	0.25	0.5	
I _I	S0, S1, S2	V _{CC} = 5.5 V,	V _I = 7 V			0.3	0.3	mA
	CLK and SERIN					0.1	0.1	
	A1-A8, B1-B8			V _{CC} = 5.5 V,	V _I = 5.5 V	0.2	0.2	
I _{IH}	S0, S1, S2	V _{CC} = 5.5 V,	V _I = 2.7 V			60	60	μA
	CLK and SERIN					20	20	
	A1-A8, B1-B8‡					70	70	
I _{IL}	S0, S1, S2	V _{CC} = 5.5 V,	V _I = 0.4 V			-1	-1	mA
	CLK and SERIN					-0.5	-0.5	
	A1-A8, B1-B8‡					-0.75	-0.75	
I _O §	Except Q8	V _{CC} = 5.5 V,	V _O = 2.25 V	-30	-112	-30	-112	mA
	Q8			-20	-112	-20	-112	
I _{CC}		V _{CC} = 5.5 V		136	220	136	220	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡For I/O ports, the parameters I_{IH} and I_{IL} include the output currents I_{OZH} and I_{OZL}, respectively.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_OS.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX				UNIT
			SN54AS877		SN74AS877		
			MIN	MAX	MIN	MAX	
f _{max}			45		50	MHz	
t _{PLH}	Any A port	Any B port	2	8.5	2	7	ns
t _{PHL}			3	10.5	3	9	
t _{PLH}	Any B port	Any A port	2	9	2	7.5	ns
t _{PHL}			3	10.5	3	9	
t _{PLH}	S0, S1, S2†	Any A or B port	3	11.5	3	10	ns
t _{PHL}			2	9.5	2	8	
t _{PLH}	CLK	Any A or B port	2	11	2	9	ns
t _{PHL}			3	13	3	11.5	
t _{PLH}	CLK	Q8	2	10.5	2	8	ns
t _{PHL}			3	10	3	8.5	
t _{PHZ}	S0, S1, S2	Any A or B port	2	7.5	2	6.5	ns
t _{PLZ}			3	13	3	10.5	
t _{PZH}			2	9	2	7	
t _{PZL}			3	11.5	3	9.5	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

†The positive transition of S2 will cause low-level data at the A output Bus or stored in the shift register to be invalid for 12 ns.

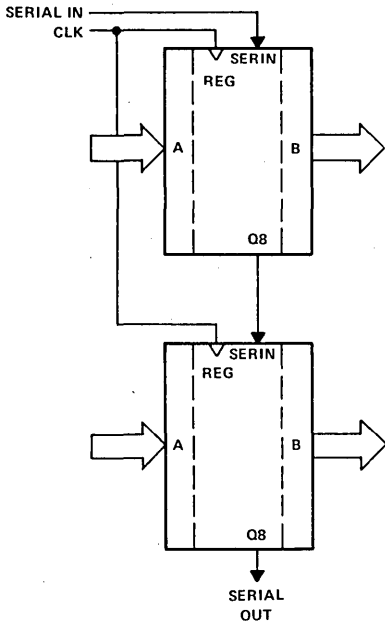
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LSI Devices

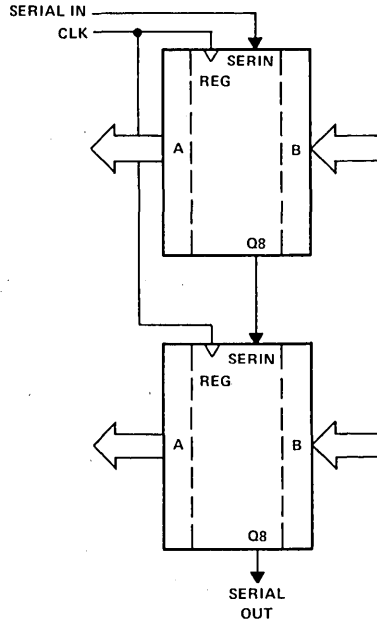
SN54AS877, SN74AS877
8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

TYPICAL APPLICATION DATA

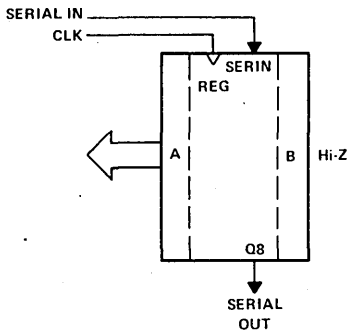
BUS A TO BUS B OR SERIAL TRANSMISSION



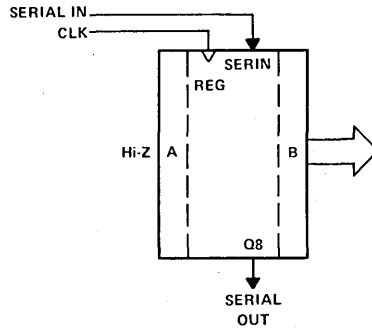
BUS B TO BUS A OR SERIAL TRANSMISSION



SERIAL IN TO A PORT



SERIAL IN TO B PORT



2
LSI Devices

SN54AS882A, SN74AS882A 32-BIT LOOK-AHEAD CARRY GENERATORS

D2661, DECEMBER 1982—REVISED NOVEMBER 1985

- Directly Compatible with 'AS181B, 'AS1181, 'AS881B, and 'AS1881 ALUs
- Included among the Package Options are Compact, 24-Pin, 300-mil-Wide DIPs and Both 28-Pin Plastic and Ceramic Chip Carriers
- Capable of Anticipating the Carry Across a Group of Eight 4-Bit Binary Adders
- Cascadable to Perform Look-Ahead Across n-Bit Adders
- Typical Carry Time, C_n to Any C_{n+i} , is Less Than 6 ns
- Dependable Texas Instruments Quality and Reliability

description

The 'AS882A is a high-speed look-ahead carry generator capable of anticipating the carry across a group of eight 4-bit adders permitting the designer to implement look-ahead for a 32-bit ALU with a single package or, by cascading 'AS882A's, full look-ahead is possible across n-bit adders.

The SN54AS882A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AS882A is characterized for operation from 0°C to 70°C .

'AS882A LOGIC EQUATIONS

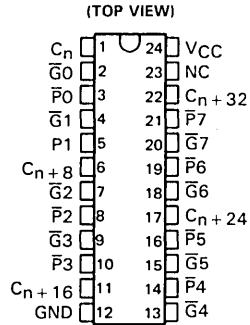
$$C_{n+8} = G1 + P1G0 + P1P0C_n$$

$$C_{n+16} = G3 + P3G2 + P3P2G1 + P3P2P1G0 + P3P2P1P0C_n$$

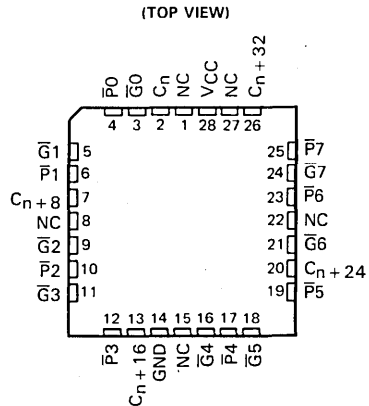
$$C_{n+24} = G5 + P5G4 + P5P4G3 + P5P4P3G2 + P5P4P3P2G1 + P5P4P3P2P1G0 + P5P4P3P2P1P0C_n$$

$$C_{n+32} = G7 + P7G6 + P7P6G5 + P7P6P5G4 + P7P6P5P4G3 + P7P6P5P4P3G2 + P7P6P5P4P3P2G1 + P7P6P5P4P3P2P1G0 + P7P6P5P4P3P2P1P0C_n$$

SN54AS882A . . . JT PACKAGE
SN74AS882A . . . DW OR NT PACKAGE



SN54AS882A . . . FK PACKAGE
SN74AS882A . . . FN PACKAGE



NC—No internal connection

2

LSI Devices

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

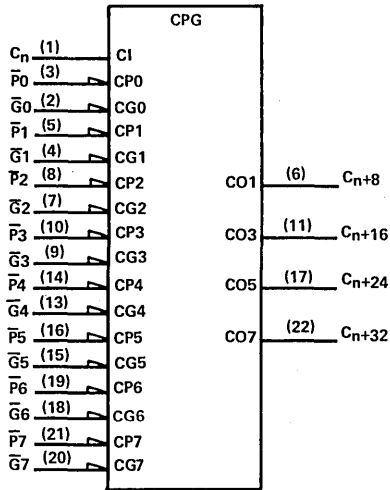
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2-231

SN54AS882A, SN74AS882A
32-BIT LOOK-AHEAD CARRY GENERATORS

logic symbol†



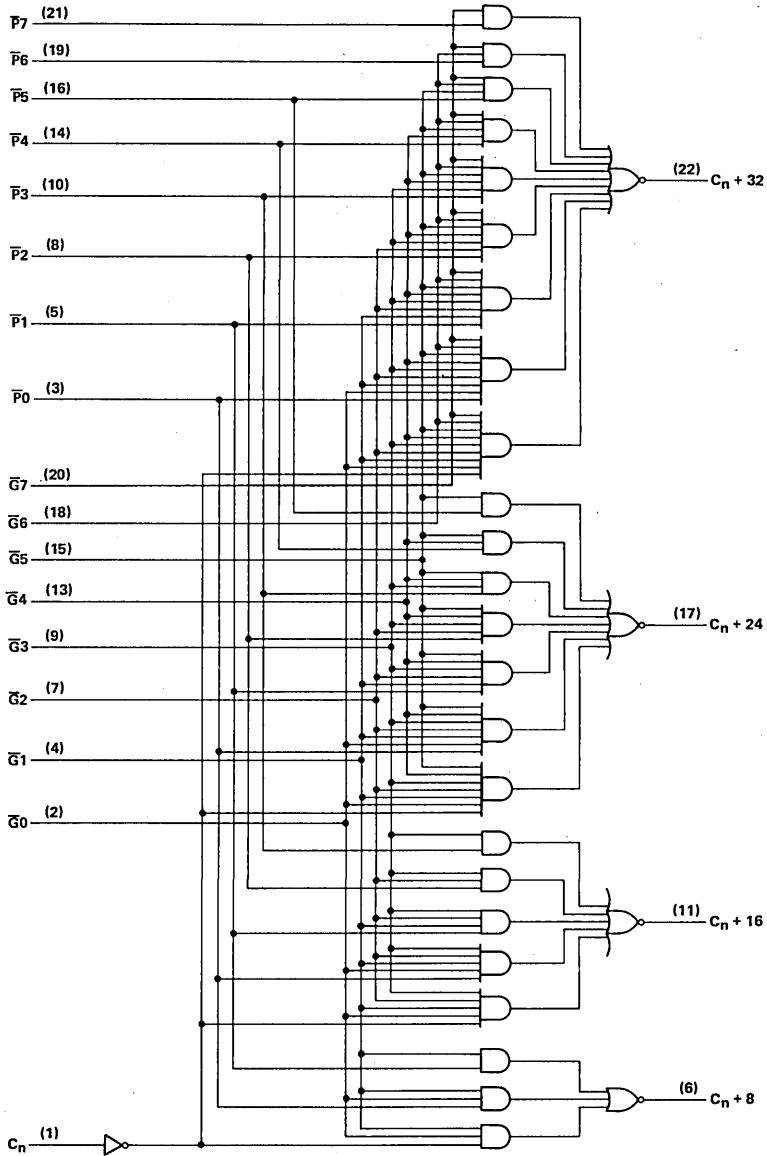
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
 Pin numbers shown are for DW, JT, and NT packages.

2

LSI Devices

SN54AS882A, SN74AS882A
32-BIT LOOK-AHEAD CARRY GENERATORS

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

SN54AS882A, SN74AS882A
32-BIT LOOK-AHEAD CARRY GENERATORS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Operating free-air temperature range: SN54AS882A	-55°C to 125°C
SN74AS882A	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54AS882A			SN74AS882A			UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX			
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V		
V_{IH}	High-level input voltage	2			2			V		
V_{IL}	Low-level input voltage	0.8			0.8			V		
I_{OH}	High-level output current	-2			-2			mA		
I_{OL}	Low-level output current	20			20			mA		
T_A	Operating free-air temperature	-55			125			0	70	°C

2
LSI Devices

SN54AS882A, SN74AS882A

32-BIT LOOK-AHEAD CARRY GENERATORS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54AS882A			SN74AS882A			UNIT
			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = -18 mA	-1.2			-1.2			V
V _{OH}		V _{CC} = 4.5 V, to 5.5 V, I _{OH} = -2 mA	V _{CC} -2			V _{CC} -2			V
V _{OL}		V _{CC} = 4.5 V, I _{OL} = 20 mA	0.3 0.5			0.3 0.5			V
I _I	C _n , P ₀ , P ₁	V _{CC} = 5.5 V, V _I = 7 V	0.4			0.4			mA
	G ₀ , G ₆		0.8			0.8			
	G ₁ , G ₂ , G ₄		1.2			1.2			
	G ₃ , G ₅		1.5			1.5			
	G ₇		0.9			0.9			
	P ₂ , P ₃		0.3			0.3			
	P ₄ , P ₅		0.2			0.2			
P ₆ , P ₇	0.1			0.1					
I _{IH}	C _n , P ₀ , P ₁	V _{CC} = 5.5 V, V _I = 2.7 V	80			80			μA
	G ₀ , G ₆		160			160			
	G ₁ , G ₂ , G ₄		240			240			
	G ₃ , G ₅		300			300			
	G ₇		180			180			
	P ₂ , P ₃		60			60			
	P ₄ , P ₅		40			40			
P ₆ , P ₇	20			20					
I _{IL}	C _n , P ₀ , P ₁	V _{CC} = 5.5 V, V _I = 0.4 V	-2			-2			mA
	G ₀ , G ₆		-4			-4			
	G ₁ , G ₂ , G ₄		-6			-6			
	G ₃ , G ₅		-7.5			-7.5			
	G ₇		-4.5			-4.5			
	P ₂ , P ₃		-1.5			-1.5			
	P ₄ , P ₅		-1			-1			
P ₆ , P ₇	-0.5			-0.5					
I _O [‡]	V _{CC} = 5.5 V, V _O = 2.25 V	-30	-130	-30	-130	mA			
I _{CC}	V _{CC} = 5.5 V	44 70		44 70		mA			

[†]All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

2

LSI Devices

SN54AS882A, SN74AS882A 32-BIT LOOK-AHEAD CARRY GENERATORS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54AS882A		SN74AS882A		
			MIN	MAX	MIN	MAX	
t_{PLH}	C_n	Any output	2	10	2	9	ns
t_{PHL}			3	15	3	14	
t_{PLH}	\bar{P} or \bar{G}	C_{n+8}	2	8	2	7	
t_{PHL}			2	8	2	7	
t_{PLH}	\bar{P} or \bar{G}	C_{n+16}	2	8	2	7	
t_{PHL}			2	8	2	7	
t_{PLH}	\bar{P} or \bar{G}	C_{n+24}	2	8	2	7	
t_{PHL}			2	11	2	10	
t_{PLH}	\bar{P} or \bar{G}	C_{n+32}	1.5	9	2	8	
t_{PHL}			2	13	2	12	

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

2

LSI Devices

SN54AS882A, SN74AS882A
32-BIT LOOK-AHEAD CARRY GENERATORS

TYPICAL APPLICATION DATA

The application given in Figure 1 illustrates how the 'AS882A can implement look-ahead carry for a 32-bit ALU (in this case, the popular 'AS881A) with a single package. Typical carry times shown are derived using the standard Advanced Schottky load circuit.

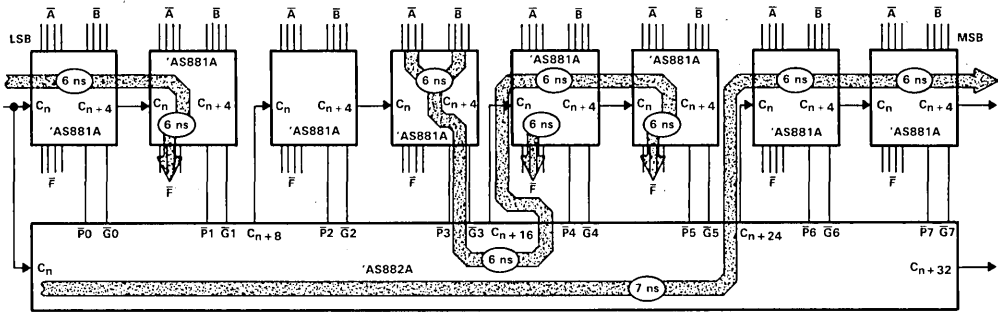


FIGURE 1

Likewise, Figure 2 illustrates the same 32-bit ALU using two 'AS882s. This shows the worst-case delay from LSB to MSB to be 19 ns as opposed to 25 ns in Figure 1.

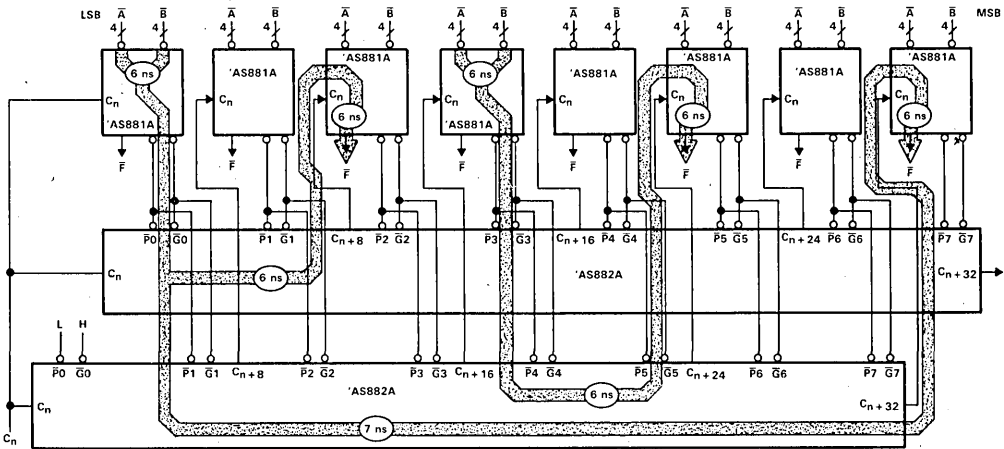


FIGURE 2

2

LSI Devices

SN54AS885, SN74AS885 8-BIT MAGNITUDE COMPARATORS

D2661, DECEMBER 1982—REVISED MARCH 1985

- Included among the Package Options Are Compact, 24-Pin, 300-mil DIPs and Both 28-Pin Ceramic and Plastic Chip Carriers
- Latchable P Input Ports with Power-Up Clear
- Choice of Logical or Arithmetic (2's Complement) Comparison
- Data and PLE Inputs Utilize P-N-P Input Transistors to Reduce DC Loading Effects
- Approximately 35% Improvement in AC Performance Over Schottky TTL while Performing More Functions
- Cascadable to n-Bits while Maintaining High Performance
- 10% Less Power than STTL for an 8-Bit Comparison
- Dependable Texas Instruments Quality and Reliability

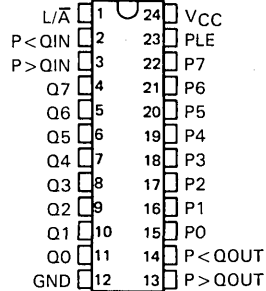
description

These advanced Schottky devices are capable of performing high-speed arithmetic or logic comparisons on two 8-bit binary or two's complement words. Two fully decoded decisions about words P and Q are externally available at two outputs. These devices are fully expandable to any number of bits without external gates. The $P > Q$ and $P < Q$ outputs of a stage handling less-significant bits may be connected to the $P > Q$ and $P < Q$ inputs of the next stage handling more-significant bits to obtain comparisons of words of longer lengths. The cascading paths are implemented with only a two-gate-level delay to reduce overall comparison times for long words. Two alternative methods of cascading are shown in the typical application data.

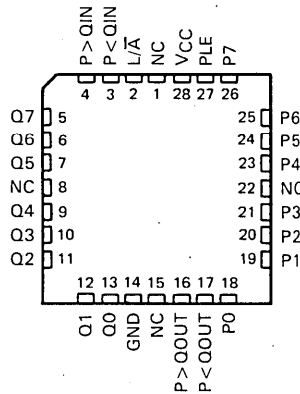
The latch is transparent when P Latch Enable (PLE) is high; the P input port is latched when PLE is low. This provides the designer with temporary storage for the P data word. The enable circuitry is implemented with minimal delay times to enhance performance when cascaded for longer words. The PLE and P and Q data inputs utilize p-n-p input transistors to reduce the low-level current input requirement to typically -0.25 mA, which minimizes dc loading effects.

The SN54AS885 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AS885 is characterized for operation from 0°C to 70°C .

SN54AS885 JT PACKAGE
SN74AS885 DW OR NT PACKAGE
(TOP VIEW)



SN54AS885 FK PACKAGE
SN74AS885 FN PACKAGE
(TOP VIEW)



2

LSI Devices

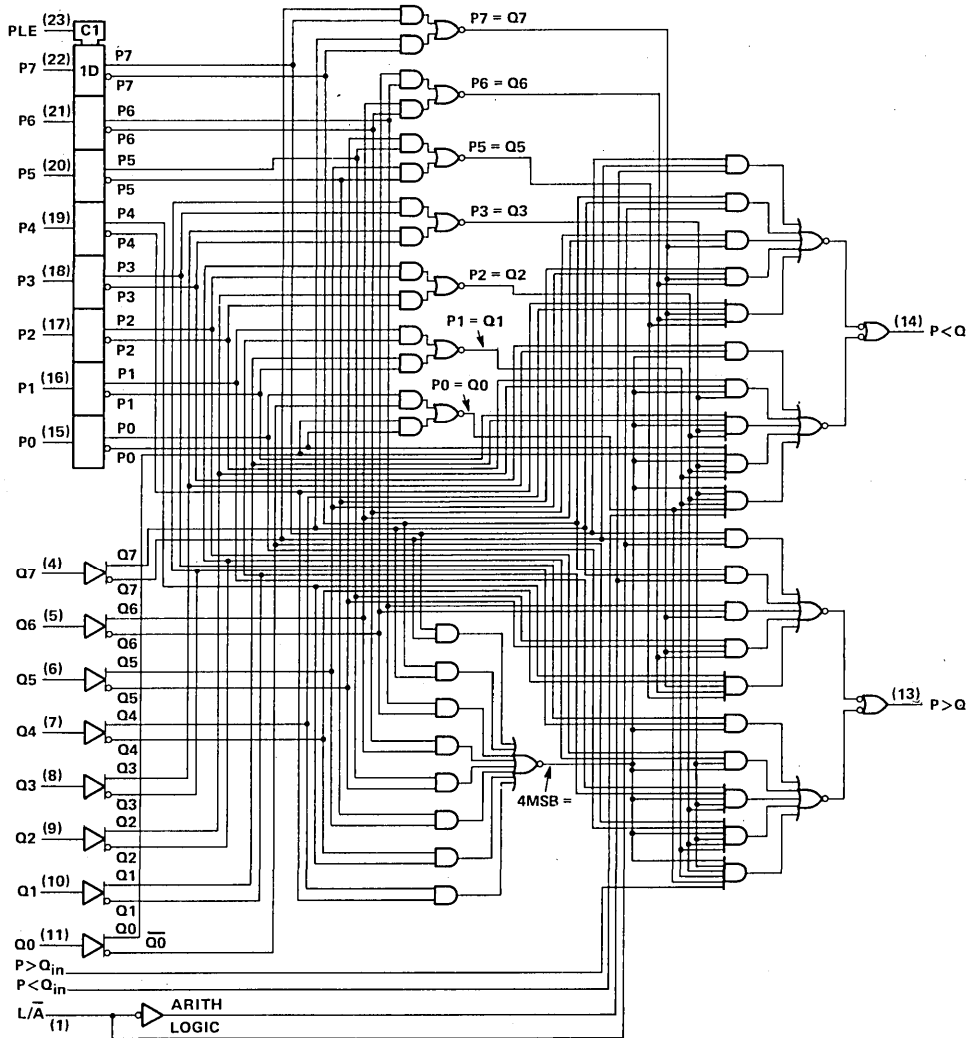
PRODUCTION DATA
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SN54AS885, SN74AS885
8-BIT MAGNITUDE COMPARATORS

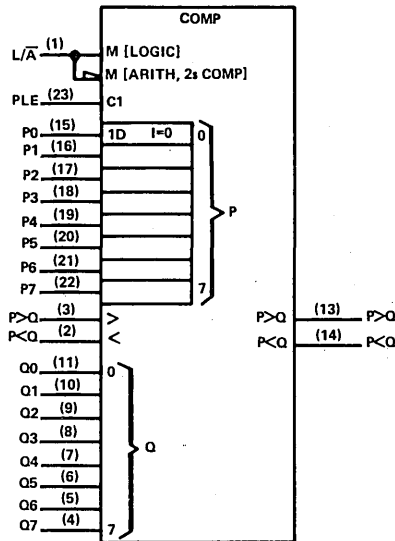
logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

SN54AS885, SN74AS885 8-BIT MAGNITUDE COMPARATORS

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.

FUNCTION TABLE

COMPARISON	L/ \bar{A}	DATA INPUTS P0-P7, Q0-Q7	INPUT		OUTPUTS	
			P > Q	P < Q	P > Q	P < Q
LOGICAL	H	P > Q	X	X	H	L
LOGICAL	H	P < Q	X	X	L	H
LOGICAL†	H	P = Q	H OR L	H OR L	H OR L	H OR L
ARITHMETIC	L	P AG Q	X	X	H	L
ARITHMETIC	L	Q AG P	X	X	L	H
ARITHMETIC†	L	P = Q	H OR L	H OR L	H OR L	H OR L

†In these cases the P > Q output will follow the P > Q input, and the P < Q output will follow the P < Q input.

AG – arithmetically greater than

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Operating free-air temperature range: SN54AS885	-55°C to 125°C
SN74AS885	0°C to 70°C
Storage temperature range	-65°C to 150°C

2

LSI Devices

SN54AS885, SN74AS885

8-BIT MAGNITUDE COMPARATORS

recommended operating conditions

PARAMETER	SN54AS885			SN74AS885			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage	0.8			0.8			V
I _{OH} High-level output current	-2			-2			mA
I _{OL} Low-level output current	20			20			mA
t _{su} Setup time to PLE↓	2			2			ns
t _h Hold time after PLE↓	4			4			
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS885		SN74AS885		UNIT
		MIN	TYP†	MAX	MIN	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA	-1.2		-1.2		V
V _{OH}	V _{CC} = 4.5 to 5.5 V, I _{OH} = -2 mA	V _{CC} -2		V _{CC} -2		V
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 20 mA	0.35	0.5	0.35	0.5	V
I _I	V _{CC} = 5.5 V, V _I = 7 V	0.1		0.1		μA
I _{IH}	L/A	40		40		μA
	Others	20		20		
I _{IL}	L/A	-4		-4		mA
	P > Q _{in}	-2		-2		
	P < Q _{in}	-2		-2		
	P, Q, PLE	-1		-1		
I _O †	V _{CC} = 5.5 V, V _O = 2.25 V	-20	-112	-20	-112	mA
I _{CC}	V _{CC} = 5.5 V See Note 1	130 210		130 210		mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit current, I_{OS}.

NOTE 1: I_{CC} is measured with all inputs high except L/A, which is low.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX				UNIT
			SN54AS885		SN74AS885		
			MIN	TYP†	MAX	MIN	
t _{PLH}	L/A	P < Q, P > Q	8.5	14	8.5	13	ns
t _{PHL}			7.5	14	7.5	13	
t _{PLH}	P < Q _{in}		5	10	5	8	ns
t _{PHL}	P > Q _{in}		5.5	10	5.5	8	
t _{PLH}	Any P or Q		13.5	21	13.5	17.5	ns
t _{PHL}	Data Input		10	17	10	15	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

2

LSI Devices

SN54AS885, SN74AS885 8-BIT MAGNITUDE COMPARATORS

TYPICAL APPLICATION DATA

The 'AS885 can be cascaded to compare words longer than 8-bits. Figure 1 shows the comparison of two 32-bit words; however, the design is expandable to n-bits. Figure 1 shows the optimum cascading arrangement for comparing words of 32 bits or greater. Typical delay times shown are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, and use the standard Advanced Schottky load of $R_L = 500\ \Omega$, $C_L = 50\text{ pF}$.

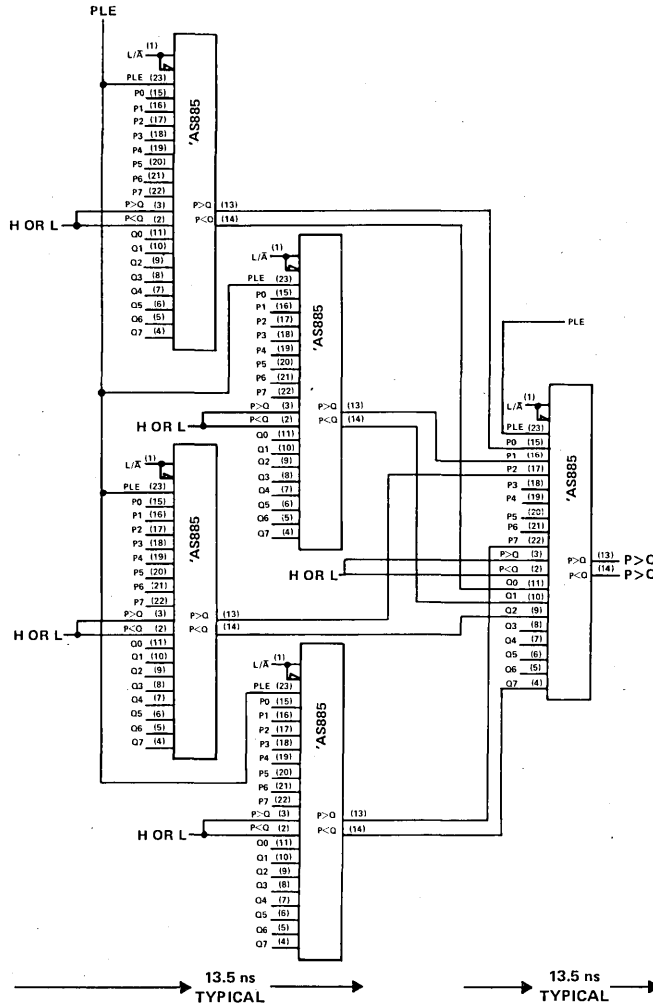


FIGURE 1. 32-BIT TO 72 (N)-BIT MAGNITUDE COMPARATOR

SN54AS885, SN74AS885
8-BIT MAGNITUDE COMPARATORS

TYPICAL APPLICATION DATA

The method shown in Figure 2 is the fastest cascading arrangement for comparing 16-bit or 24-bit words. Typical delay times shown are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, and use the standard Advanced Schottky load of $R_L = 500\ \Omega$, $C_L = 50\text{ pF}$.

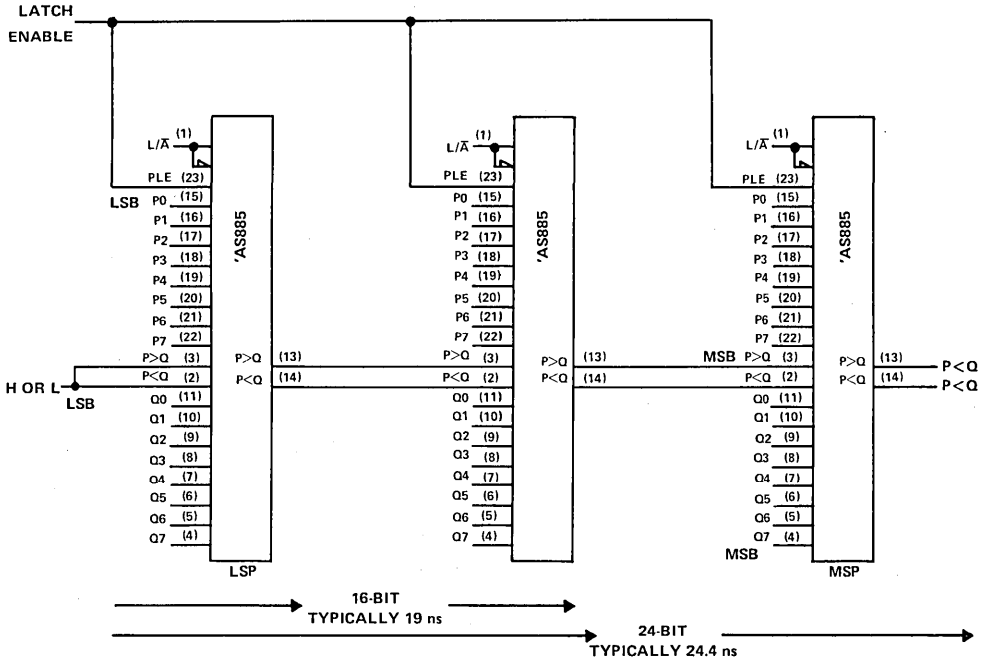


FIGURE 2

2
LSI Devices

- STL-AS Technology
- Parallel 8-Bit ALU with Expansion Inputs and Outputs
- 13 Arithmetic and Logic Functions
- 8 Conditional Shifts (Single and Double Length)
- 4 Instructions that Manipulate Bits
- Add and Subtract Immediate Instructions
- Absolute Value Instruction
- Signed Magnitude to/from Two's Complement Conversion
- Single- and Double-Length Normalize
- Select Functions
- Signed and Unsigned Divides with Overflow Detection; Input does not Need to be Prescaled
- Signed, Mixed, and Unsigned Multiplies
- Three-Operand, 16-Word Register File
- Full Carry Look Ahead Support
- Sign, Carry Out, Overflow, and Zero-Detect Status Capabilities
- Excess-3 BCD Arithmetic
- Internal Shift Multiplexers that Eliminate the Need for External Shift Control Parts
- ALU Bypass Path to Increase Speeds of Multiply, Divide, and Normalize Instructions and to Provide New Instructions such as Bit Set, Bit Reset, and Bit Test
- 3-Operand Register Files to Allow an Operation and a Move Instruction to be Combined
- Bit Masks that are Shared with Register Address Fields to Minimize Control Store Word Width
- 3 Data Input/Output Paths to Maximize Data Throughput

description

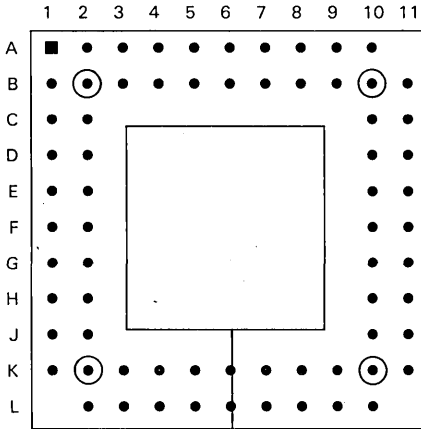
These 8-bit Advanced Schottky TTL integrated circuits are designed to implement high performance digital computers or controllers. An architecture and instruction set has been chosen that supports a fast system clock, a narrow micro-code word width, and a high system throughput. The powerful instruction set allows high-speed system architecture to be implemented and also allows an existing system's performance to be upgraded while protecting software investments. These processors are non-cascadable versions of the 'AS888. They are designed for 8-bit applications only.

The SN54AS887 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AS887 and SN74AS887-1 are characterized for operation from 0°C to 70°C .

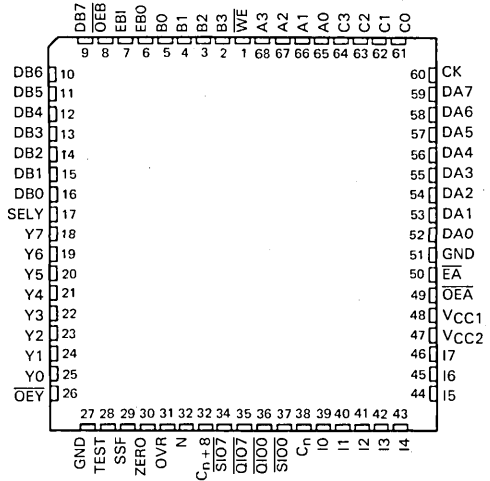
Package options include both plastic and ceramic chip carriers in addition to a 68-pin grid array ceramic package.

SN54AS887, SN74AS887 8-BIT PROCESSORS

SN54AS887, SN74AS887 . . . GB PACKAGE
(TOP VIEW)



SN54AS887 . . . FK PACKAGE
SN74AS887 . . . FN PACKAGE
(TOP VIEW)



GB PACKAGE PIN ASSIGNMENTS

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
A-2	C _n	B-9	OEY	F-10	Y3	K-4	C2
A-3	S100	B-10	Y0	F-11	DB2	K-5	A0
A-4	Q100	B-11	Y1	G-1	DA2	K-6	A3
A-5	Q107	C-1	I5	G-2	DA0	K-7	WE
A-6	C _{n+8}	C-2	VCC2	G-10	DB0	K-8	DB7
A-7	N	C-10	Y4	G-11	DB3	K-9	OE8
A-8	OVR	C-11	Y6	H-1	DA3	K-10	E80
A-9	ZERO	D-1	I6	H-2	DA1	K-11	EB1
A-10	TEST	D-2	VCC1	H-10	DB6	L-2	CK
B-1	I2	D-10	Y5	H-11	DB4	L-3	C1
B-2	I3	D-11	Y7	J-1	DA4	L-4	C3
B-3	I1	E-1	I7	J-2	DA5	L-5	A1
B-4	I0	E-2	OE \bar{A}	J-10	SELY	L-6	A2
B-5	I4	E-10	Y2	J-11	DB5	L-7	B3
B-6	S107	E-11	DB1	K-1	DA6	L-8	B2
B-7	SSF	F-1	EA	K-2	DA7	L-9	B1
B-8		F-2	GND	K-3	C0	L-10	B0

2

LSI Devices

**SN54AS887, SN74AS887
8-BIT PROCESSORS**

PIN GRID ARRAY	CHIP CARRIER	NAME	I/O	DESCRIPTION
A-10	28	TEST	I	Test input pin. Connected to ground for normal operation.
B-7	29	SSF	I/O	Special shift function. Used to transfer required information between packages during special instruction execution.
A-9	30	ZERO	I/O	Device zero detection, open collector. Input during certain special instructions.
A-8	31	OVR	O	ALU overflow, low active.
A-7	32	N	O	ALU negative, low active.
A-6	33	C _{n+8}	O	ALU ripple carry output.
B-6	34	$\overline{SIO7}$	I/O	Bidirectional shift pin, low active.
A-5	35	$\overline{QIO7}$	I/O	
A-4	36	$\overline{QIO0}$	I/O	
A-3	37	$\overline{SIO0}$	I/O	
A-2	38	C _n	I	ALU carry input.
B-4	39	I0	I	Instruction input.
B-3	40	I1	I	
B-1	41	I2	I	
B-2	42	I3	I	
B-5	43	I4	I	
C-1	44	I5	I	
D-1	45	I6	I	
E-1	46	I7	I	
C-2	47	VCC2		Low voltage power supply (2 V).
D-2	48	VCC1		I/O interface supply voltage (5 V).
E-2	49	$\overline{OE}A$	I	DA bus enable, low active.
F-1	50	\overline{EA}	I	ALU input operand select. High state selects external DA bus and low state selects register file.
F-2	51	GND		Ground pin.
G-2	52	DA0	I/O	A port data bus. Outputs register file data ($\overline{EA} = 0$) or inputs external data ($\overline{EA} = 1$).
H-2	53	DA1	I/O	
G-1	54	DA2	I/O	
H-1	55	DA3	I/O	
J-1	56	DA4	I/O	
J-2	57	DA5	I/O	
K-1	58	DA6	I/O	
K-2	59	DA7	I/O	
L-2	60	CK	I	Clocks all synchronous registers on positive edge.
K-3	61	C0	I	Register file write address select.
L-3	62	C1	I	
K-4	63	C2	I	
L-4	64	C3	I	
K-5	65	A0	I	Register file A port read address select.
L-5	66	A1	I	
L-6	67	A2	I	
K-6	68	A3	I	

2

LSI Devices

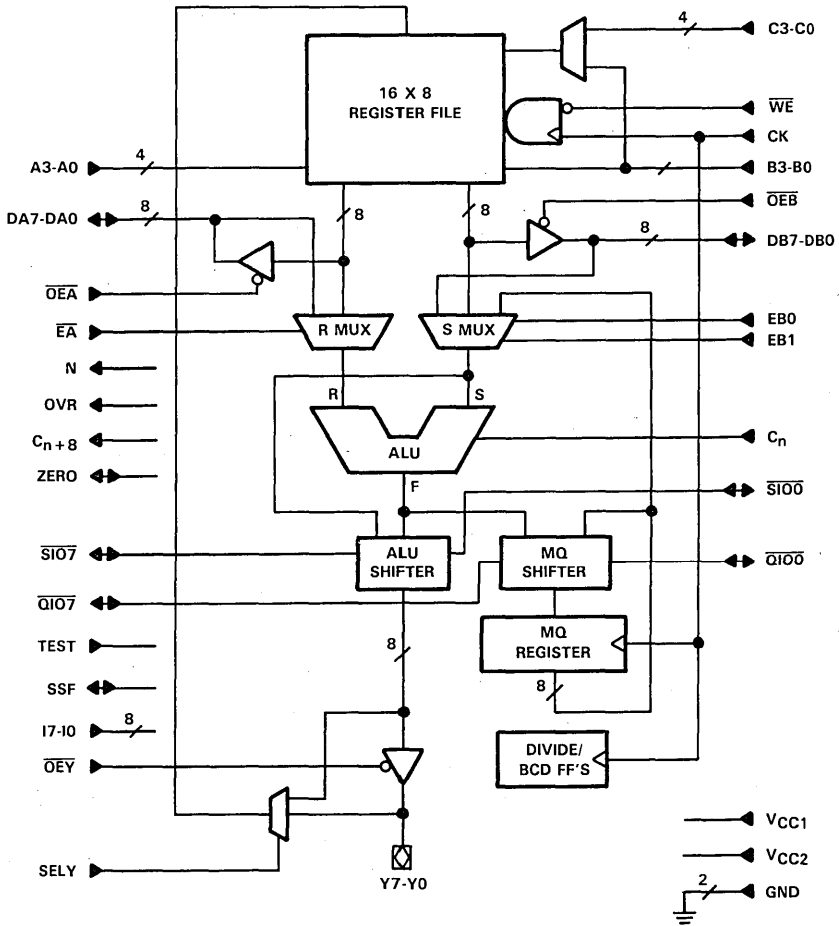
SN54AS887, SN74AS887
8-BIT PROCESSORS

PIN GRID ARRAY	CHIP CARRIER	NAME	I/O	DESCRIPTION
K-7	1	\overline{WE}	I	Register file (RF) write enable. Data is written into RF when \overline{WE} is low and a low-to-high clock transition occurs. RF write is inhibited when \overline{WE} is high.
L-7	2	B3	I	Register file B port read address select. (0 = LSB).
L-8	3	B2	I	
L-9	4	B1	I	
L-10	5	B0	I	
K-10	6	EBO	I	ALU input operand select. EBO and EB1 selects the source of data that the S multiplexer provides for the S bus. Independent control of the DB bus and data path selection allow the user to isolate the DB bus while the ALU continues to process data.
K-11	7	EB1	I	
K-9	8	\overline{OEB}	I	DB bus enable, low active.
K-8	9	DB7	I/O	B port data bus. Outputs register data ($\overline{OEB} = 0$) or used to input external data ($\overline{OEB} = 1$), (0 = LSB).
H-10	10	DB6	I/O	
J-11	11	DB5	I/O	
H-11	12	DB4	I/O	
G-11	13	DB3	I/O	
F-11	14	DB2	I/O	
E-11	15	DB1	I/O	
G-10	16	DB0	I/O	
J-10	17	SELY	I	Y bus select, high active.
D-11	18	Y7	I/O	Y port data bus. Outputs instruction results ($\overline{OEY} = 0$) or used to put external data into register file ($\overline{OEY} = 1$).
C-11	19	Y6	I/O	
D-10	20	Y5	I/O	
C-10	21	Y4	I/O	
F-10	22	Y3	I/O	
E-10	23	Y2	I/O	
B-11	24	Y1	I/O	
B-10	25	Y0	I/O	
B-9	26	\overline{OEY}	I	Y bus output enable, low active.
F-2	27	GND		Ground pin

2 LSI Devices

SN54AS887, SN74AS887
8-BIT PROCESSORS

functional block diagram



SN54AS887, SN74AS887 8-BIT PROCESSORS

architectural elements

3-port register file

Working registers consist of 128 storage elements organized into sixteen 8-bit words. These storage elements appear to the user as 16 positive edge-triggered registers. The three port addresses, one write (C) and two reads (A and B), are completely independent of each other to implement a 3-operand register file. Data is written into the register file when \overline{WE} is low and a low-to-high clock transition occurs. The ADD and SUBTRACT immediate instructions require only one source operand. The B address is used as the source address, and the bits of the A address are used to provide a constant field. The SET, RESET, and TEST BIT instructions use the B addressed register as both the source and destination register while the A and C addresses are used as masks. These instructions are explained in more detail in the instruction section.

S multiplexer

The S multiplexer selects the ALU operand, as follows:

EB1	EB0	S bus
Low	Low	RF data
Low	High	MQ data
High	Low	DB data
High	High	MQ data

DB port

The 8-bit bidirectional DB port inputs external data to the ALU or outputs the register file. If \overline{OEB} is low, the DB bus is active; if \overline{OEB} is high, the DB bus is in the high impedance state. Notice that the DB port may be isolated at the same time that register file data is passed to the ALU.

R multiplexer

The R multiplexer selects the other operand of the ALU. Except for those instructions that require constants or masks, the R bus will contain DA if \overline{EA} is high or the RF data pointed to by A if \overline{EA} is low.

DA port

The 8-bit bidirectional DA port inputs external data to the ALU or outputs the register file. If \overline{OEA} is low, the DA bus is active; if \overline{OEA} is high, the DA bus is in the high-impedance state.

Notice that the DA bus may be isolated while register file data is passed to the ALU.

ALU

The shift instructions are summarized in Table 4 and illustrated in Figure 2. The ALU can perform seven arithmetic and six logical instructions on two 8-bit operands. It also supports multiplication, division, normalization, bit set, reset, test, byte operations, and excess-3 BCD arithmetic. These source operands are the outputs of the S and R multiplexers.

ALU and MQ shifters

ALU and MQ shifters perform all of the shift, multiply, divide, and normalize functions. Table 4 shows the value of the $\overline{SIO7}$ and $\overline{QIO7}$ pins of the most significant package. The standard shifts may be made into conditional shifts and the serial data may be input or output with the aid of two three-state gates. These capabilities are discussed further in the arithmetic and logic section.

MQ register

The multiplier-quotient (MQ) register has specific functions in multiplication, division, and normalization. This register may also be used as a temporary storage register. The MQ register may be loaded if the instruction code on pins I7-I0 is E1-E7 or E9-EE (See Table 1).

Y bus

The Y bus contains the output of the ALU shifter if \overline{OEY} is low and is a high impedance input if \overline{OEY} is high. SELY must be low to pass the internal ALU shift bus and must be high to pass the external Y bus to the register file.

status

Four status pins are available on the most significant package, overflow (OVR), sign (N), carry out (C_{n+8}), and zero (ZERO). The C_{n+8} line signifies the ALU result while OVR, ZERO, and N refer the status after the ALU shift has occurred. Notice that the ZERO pin cannot be used to detect whether an input placed on a high impedance Y bus is zero.

divide BCD flip-flops

The multiply-divide flip-flops contain the status of the previous multiply or divide instruction. They are affected by the following instructions:

DIVIDE REMAINDER FIX	SIGNED DIVIDE ITERATE
SIGNED DIVIDE QUOTIENT FIX	UNSIGNED DIVIDE START
SIGNED MULTIPLY	UNSIGNED DIVIDE ITERATE
SIGNED MULTIPLY TERMINATE	UNSIGNED MULTIPLY
SIGNED DIVIDE INITIALIZE	SIGNED DIVIDE TERMINATE
SIGNED DIVIDE START	UNSIGNED DIVIDE TERMINATE

The excess-3 BCD flip-flops are affected by all instructions except NOP. The clear function clears these flip-flops. They preserve the carry from each nibble (4-bits) in excess-3/BCD operations.

test pin (test)

This pin should be connected to ground.

special shift function (SSF) pin

Conditional shifting algorithms may be implemented via control of the SSF pin. The applied voltage to this pin may be set as a function of a potential overflow condition (the two most significant bits are not equal) or any other condition (see Group 1 instructions).

instruction set

The 'AS887 bit-slice processor uses bits 17-10 as instruction inputs. A combination of bits I3-I0 (Group 1 instructions) and bits I7-I4 (Group 2-5 instructions) are used to develop the 8-bit op code for a specific instruction. Group 1 and Group 2 instructions can be combined to perform arithmetic or logical functions plus a shift function in one instruction cycle. A summary of the instruction set is given in Table 1.

TABLE 1. INSTRUCTION SET

GROUP 1 INSTRUCTIONS		
INSTRUCTION BITS (I3-I0) HEX CODE	MNEMONIC	FUNCTION
0		Accesses Group 4 instructions
1	ADD	$R + S + C_n$
2	SUBR	$\bar{R} + S + C_n$
3	SUBS	$R + \bar{S} + C_n$
4	INCS	$S + C_n$
5	INCNS	$\bar{S} + C_n$
6	INCR	$R + C_n$
7	INCNR	$\bar{R} + C_n$
8		Accesses Group 3 instructions
9	XOR	R XOR S
A	AND	R AND S
B	OR	R OR S
C	NAND	R NAND S
D	NOR	R NOR S
E	ANDNR	\bar{R} AND S
F		Accesses Group 5 instructions
GROUP 2 INSTRUCTIONS		
INSTRUCTION BITS (I7-I4) HEX CODE	MNEMONIC	FUNCTION
0	SRA	Arithmetic Right Single
1	SRAD	Arithmetic Right Double
2	SRL	Logical Right Single
3	SRLD	Logical Right Double
4	SLA	Arithmetic Left Single
5	SLAD	Arithmetic Left Double
6	SLC	Circular Left Single
7	SLCD	Circular Left Double
8	SRC	Circular Right Single
9	SRCD	Circular Right Double
A	MQSRA	Pass (F→Y) and Arithmetic Right MQ
B	MQSRL	Pass (F→Y) and Logical Right MQ
C	MQSLL	Pass (F→Y) and Logical Left MQ
D	MQSLC	Pass (F→Y) and Circular Left MQ
E	LOADMQ	Pass (F→Y) and Load MQ (F = MQ)
F	PASS	Pass (F→Y)

TABLE 1. INSTRUCTION SET (Continued)

GROUP 3 INSTRUCTIONS

INSTRUCTION BITS (I7-I0) HEX CODE	MNEMONIC	FUNCTION
08	SET1	Set Bit
18	SETO	Reset Bit
28	TB1	Test Bit (One)
38	TB0	Test Bit (Zero)
48	ABS	Absolute Value
58	SMTC	Sign Magnitude/Two's Complement
68	ADDI	Add Immediate
78	SUBI	Subtract Immediate
88		Reserved
98		Reserved
A8		Reserved
B8		Reserved
C8		Reserved
D8		Reserved
E8		Reserved
F8		Reserved

GROUP 4 INSTRUCTIONS

INSTRUCTION BITS (I7-I0) HEX CODE	MNEMONIC	FUNCTION
00		Reserved
10	SEL	Select S/R
20	SNORM	Single Length Normalize
30	DNORM	Double Length Normalize
40	DIVRF	Divide Remainder Fix
50	SDIVQF	Signed Divide Quotient Fix
60	SMULI	Signed Multiply Iterate
70	SMULT	Signed Multiply Terminate
80	SDIVIN	Signed Divide Initialize
90	SDIVIS	Signed Divide Start
A0	SDIVI	Signed Divide Iterate
B0	UDIVIS	Unsigned Divide Start
C0	UDIVI	Unsigned Divide Iterate
D0	UMULI	Unsigned Multiply Iterate
E0	SDIVIT	Signed Divide Terminate
F0	UDIVIT	Unsigned Divide Terminate

2
LSI Devices

TABLE 1. INSTRUCTION SET (Concluded)

GROUP 5 INSTRUCTIONS

INSTRUCTION BITS (I7-I0) HEX CODE	MNEMONIC	FUNCTION
0F	CLR	Clear
1F	CLR	Clear
2F	CLR	Clear
3F	CLR	Clear
4F	CLR	Clear
5F	CLR	Clear
6F	CLR	Clear
7F	BCDBIN	BCD to Binary
8F		Reserved
9F	EX3C	Excess-3 Word Correction
AF	SDIVO	Signed Divide Overflow Check
BF	CLR	Clear
CF	CLR	Clear
DF	BINEX3	Binary to Excess-3
EF	CLR	Clear
FF	NOP	No-Operation

2

group 1 instructions

TABLE 2. GROUP 1 INSTRUCTIONS

INSTRUCTION BITS (I3-I0) HEX CODE	MNEMONIC	FUNCTION
0		Accesses Group 4 instructions
1	ADD	$R + S + C_n$
2	SUBR	$\bar{R} + S + C_n$
3	SUBS	$R + \bar{S} + C_n$
4	INCS	$S + C_n$
5	INCNS	$\bar{S} + C_n$
6	INCR	$R + C_n$
7	INCR	$\bar{R} + C_n$
8		Accesses Group 3 instructions
9	XOR	R XOR S
A	AND	R AND S
B	OR	R OR S
C	NAND	R NAND S
D	NOR	R NOR S
E	ANDNR	\bar{R} AND S
F		Accesses Group 5 instructions

LSI Devices

Group 1 instructions (excluding hex codes 0, 8, and F), shown in Table 2, may be used in conjunction with Group 2 shift instructions to perform arithmetic or logical functions plus a shift function[†] in one instruction cycle (hex codes 0, 8, and F are used to access Group 4, 3, and 5 instructions, respectively). Each shift may be made into a conditional shift by forcing the special shift function (SSF) pin into the proper state. If the SSF pin is high or floating, the shifted ALU output will be sent to the output buffers. If the SSF pin is pulled low externally, the ALU result will be passed directly to the output buffers. Conditional shifting is useful for scaling inputs in data arrays or in signal processing algorithms.

These instructions set the BCD flip-flop for the excess-3 correct instruction. The status is set with the following results (C_{n+8} is ALU carry out and is independent of shift operation; others are evaluated after shift operation).

[†]Double-precision shifts involve both the ALU and MQ register.

Status is set with the following results:

Arithmetic

- N → MSB of result
- OVR → Signed arithmetic overflow
- C_{n+8} → Carry out equal one
- Z → Result equal zero

Logic

- N → MSB of result
- OVR → None (force to zero)
- C_{n+8} → None (force to zero)
- Z → Result equal zero

group 2 instructions

TABLE 3. GROUP 2 INSTRUCTIONS

INSTRUCTION BITS (I7-I4) HEX CODE	MNEMONIC	FUNCTION
0	SRA	Arithmetic Right Single
1	SRAD	Arithmetic Right Double
2	SRL	Logical Right Single
3	SRLD	Logical Right Double
4	SLA	Arithmetic Left Single
5	SLAD	Arithmetic Left Double
6	SLC	Circular Left Single
7	SLCD	Circular Left Double
8	SRC	Circular Right Single
9	SRCD	Circular Right Double
A	MQSRA	Pass (F→Y) and Arithmetic Right MQ
B	MQSRL	Pass (F→Y) and Logical Right MQ
C	MQSLL	Pass (F→Y) and Logical Left MQ
D	MQSLC	Pass (F→Y) and Circular Left MQ
E	LOADMQ	Pass (F→Y) and Load MQ (F=MQ)
F	PASS	Pass (F→Y)

SN54AS887, SN74AS887
8-BIT PROCESSORS

The processor's shift instructions are implemented using Group 2 instructions (Table 3). The connections are the same on all instructions including multiply, divide, and normalization functions.

The following external connections are required:

$$\begin{array}{l} \overline{SIO7} \text{ to } \overline{SIO0} \\ \overline{QIO7} \text{ to } \overline{QIO0} \end{array}$$

Single- and double-precision shifts are supported. Double-precision shifts assume the most significant half has come through the ALU and will be placed (if WE is low) into the register file on the rising edge of the clock and the least significant half lies in the MQ register. All Group 2 shifts may be made conditional. (see previous page)

The following definitions apply to Group 2 shift instructions:

Arithmetic right shifts copy the sign of the number if no overflow occurs from the ALU calculation; if overflow occurs, the sign bit is inverted.

Arithmetic left shifts do not retain the sign of the number if an overflow occurs. A zero is filled into the LSB if not forced externally.

Logical right shifts fill a zero in the MSB position if not forced externally.

Circular right shifts fill the LSB in the MSB position.

Circular left shifts fill the MSB in the LSB position.

Shifting left is defined as moving a bit position towards the MSB (doubling).

Shifting right is defined as moving a bit towards the LSB (halving).

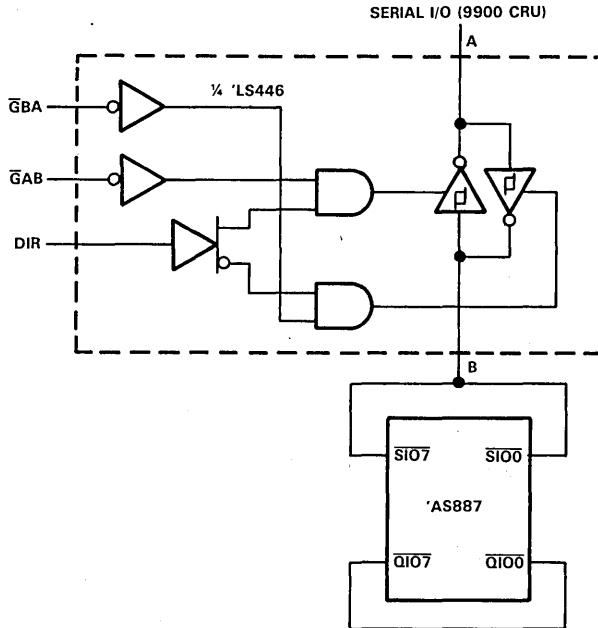


FIGURE 1. SERIAL I/O

Serial input may be performed using the circuitry shown in Figure 1. A single-/or double-precision arithmetic left or logical right shift fills the complement of the data on $\overline{SIO0}$ and $\overline{SIO7}$ into the LSB or MSB of the data word(s). Note that if $\overline{SIO0}$ and $\overline{SIO7}$ are floating (HI-Z), a zero will be filled as an end condition.

Serial output may be performed with circular instructions.

The shift instructions are summarized in Table 4 and illustrated in Figure 2. In Figure 2 and all succeeding figures that illustrate instruction execution, the following definitions apply:

- QBT — End fill for signed divide.
- MQF — End fill for unsigned divide.
- SRF — End fill for signed multiply and the arithmetic right shifts.

TABLE 4. SHIFT INSTRUCTIONS

OP CODE [†]	SHIFT FUNCTION [‡]	$\overline{SIO7} \cdot \overline{SIO0}$ WIRED VALUE	$\overline{QIO7} \cdot \overline{QIO0}$ WIRED VALUE
0N	Arithmetic Right Single	ALU-LSB Output	—
1N	Arithmetic Right Double	MQ-LSB Output	ALU-LSB Output
2N	Logical Right Single	Input to ALU-MSB	ALU-LSB Output
3N	Logical Right Double	Input to ALU-MSB	ALU-LSB Output
4N	Arithmetic Left Single	Input to ALU-LSB	ALU-MSB Output
5N	Arithmetic Left Double	Input to MQ-LSB	MQ-MSB Output
6N	Circular Left Single	ALU-MSB Output	—
7N	Circular Left Double	ALU-MSB Output	MQ-MSB Output
8N	Circular Right Single	ALU-LSB Output	—
9N	Circular Right Double	MQ-LSB Output	ALU-LSB Output
AN	Arithmetic Right (MQ only)	MQ-LSB Output	MQ-LSB Output
BN	Logical Right (MQ only)	MQ-LSB Output	Input to MQ-MSB
CN	Logical Left (MQ only)	Input to MQ-LSB	MQ-MSB Output
DN	Circular Left (MQ only)	MQ-MSB Output	MQ-MSB Output

[†]Op Code N ≠ 0, 8, or F; these select special instruction Groups 4, 3, and 5 respectively.

[‡]Shift I/O pins are active low. Therefore, inputs and outputs must be inverted if true logical values are required.

Status is set with the following results:

Arithmetic

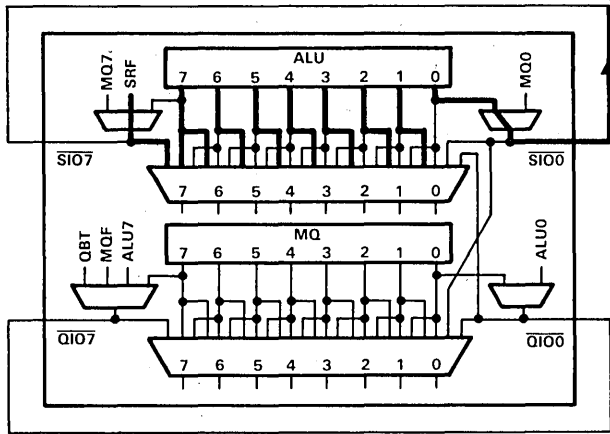
- N → Result MSB equal one
- OVR → Signed arithmetic overflow[†]
- C_{n+8} → Carry out equal one
- Z → Result equal zero

Logic

- N → Result MSB equal one
- OVR → Zero
- C_{n+8} → Zero
- Z → Result equal zero

[†] For the SLA and SLAD instructions, OVR is set if signed arithmetic overflow or if the ALU result MSB XOR MSB-1 equals one.

ARITHMETIC RIGHT SINGLE



ARITHMETIC RIGHT DOUBLE

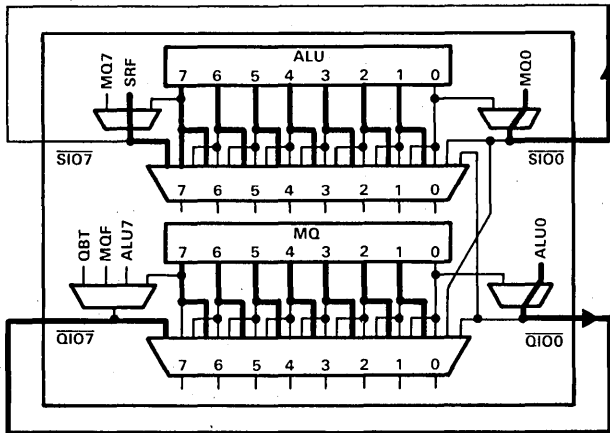
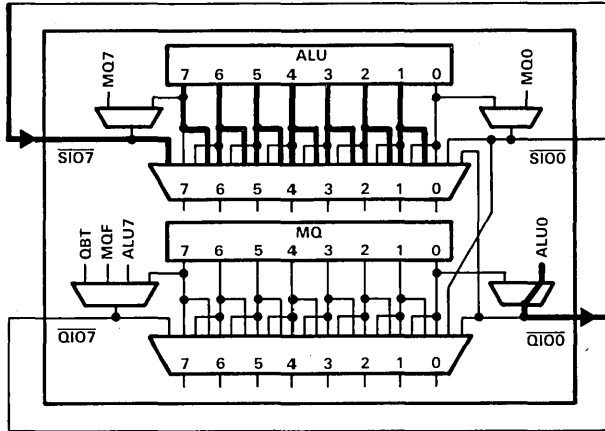


FIGURE 2. SHIFT INSTRUCTIONS

LOGICAL RIGHT SINGLE

FILLS ZERO IF NOT FORCED



LOGICAL RIGHT DOUBLE

FILLS ZERO IF NOT FORCED

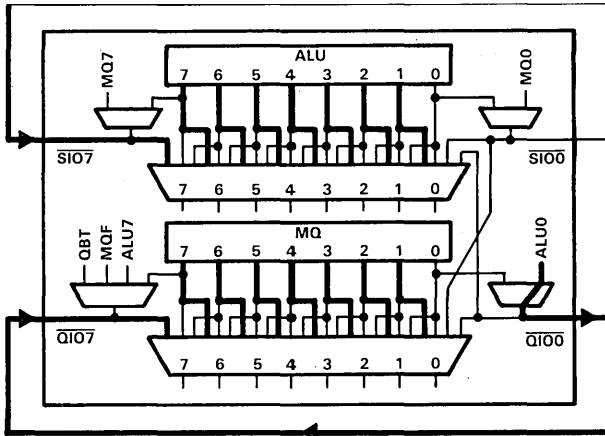
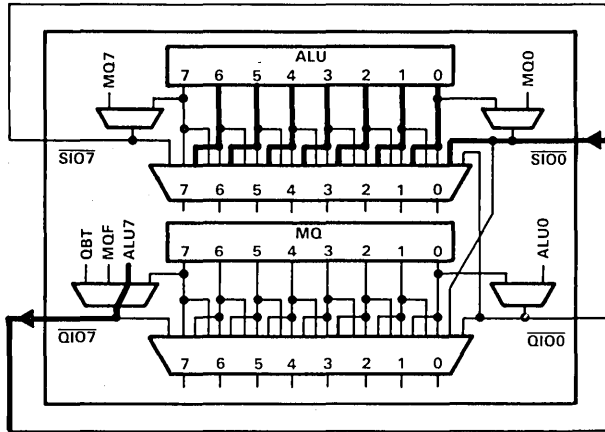


FIGURE 2. SHIFT INSTRUCTIONS (Continued)

ARITHMETIC LEFT SINGLE

FILLS ZERO IF NOT FORCED



ARITHMETIC LEFT DOUBLE

FILLS ZERO IF NOT FORCED

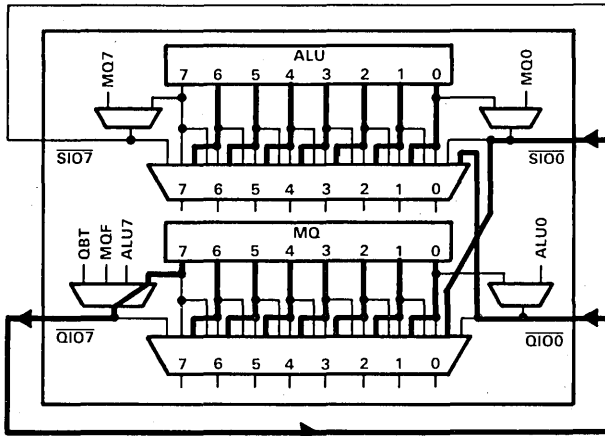
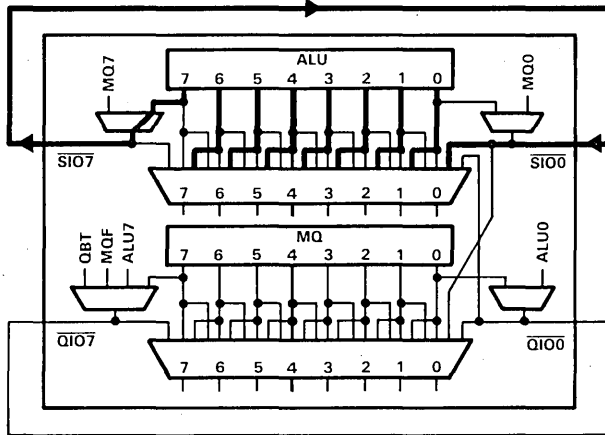


FIGURE 2. SHIFT INSTRUCTIONS (Continued)

2

LSI Devices

CIRCULAR LEFT SINGLE



CIRCULAR LEFT DOUBLE

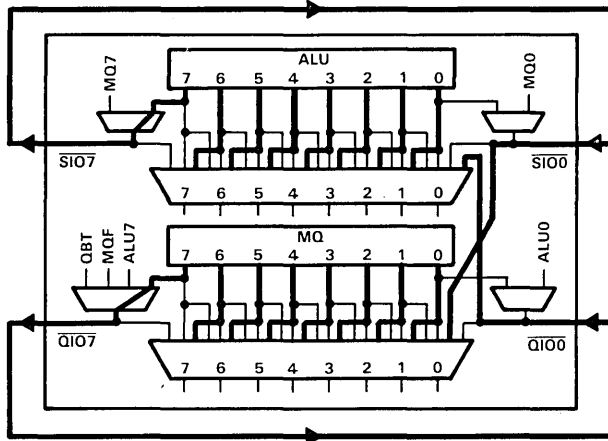
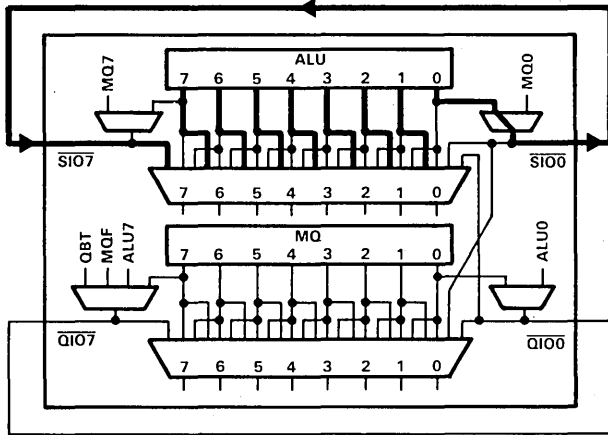


FIGURE 2. SHIFT INSTRUCTIONS (Continued)

CIRCULAR RIGHT SINGLE



CIRCULAR RIGHT DOUBLE

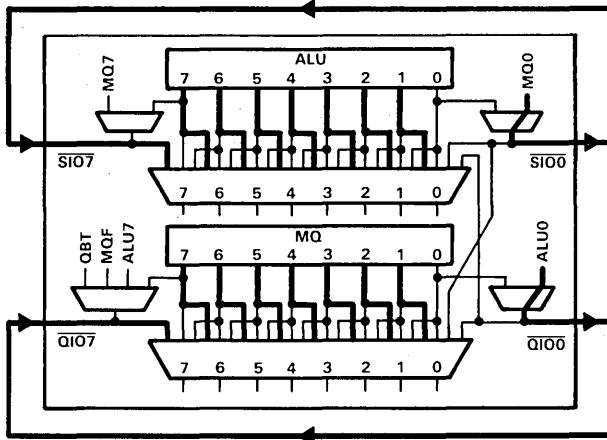
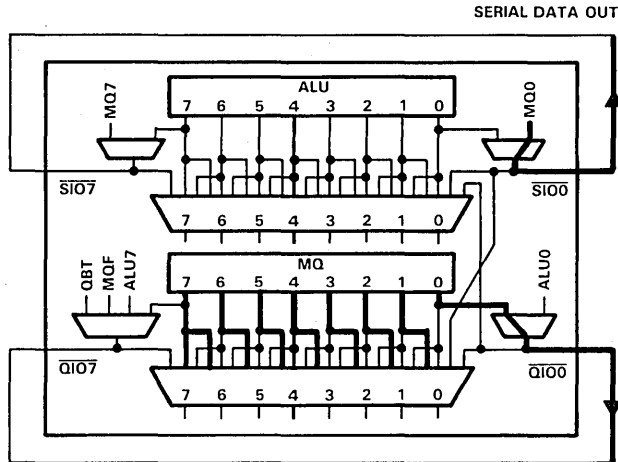
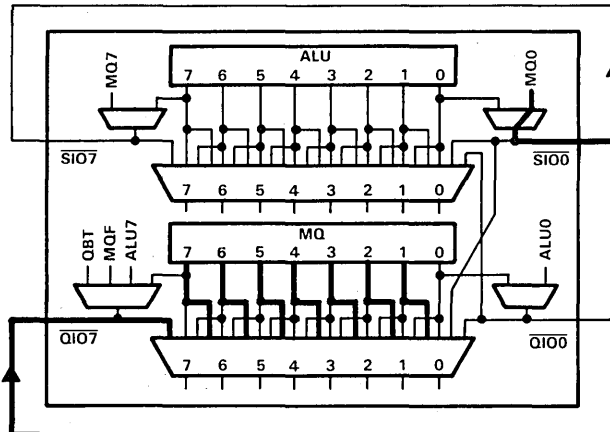


FIGURE 2. SHIFT INSTRUCTIONS (Continued)

ARITHMETIC RIGHT (MQ ONLY)



LOGICAL RIGHT (MQ ONLY)

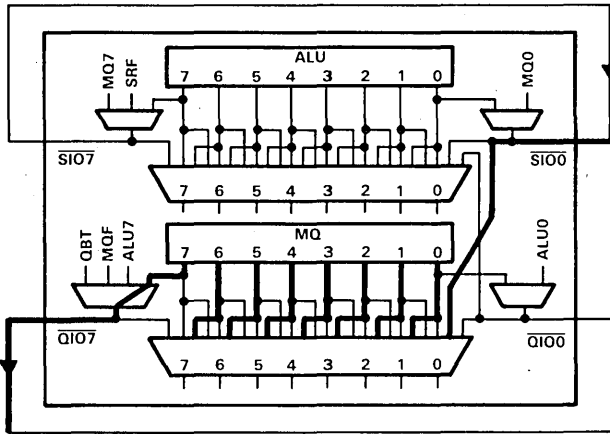


FILLS ZERO IF NOT FORCED

FIGURE 2. SHIFT INSTRUCTIONS (Continued)

LOGICAL LEFT (MQ ONLY)

FILLS ZERO IF NOT FORCED



CIRCULAR LEFT (MQ ONLY)

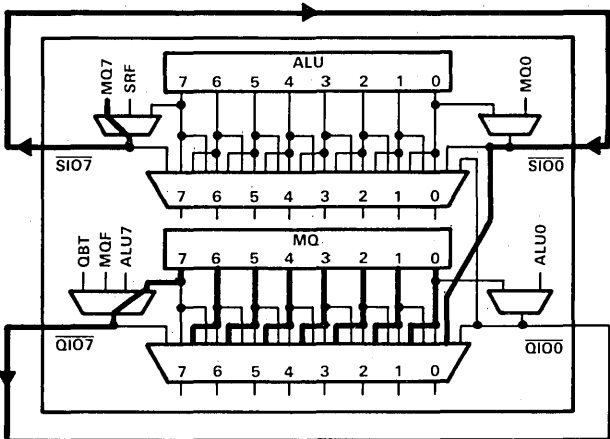


FIGURE 2. SHIFT INSTRUCTIONS (Concluded)

group 3 instructions

Hex code 8 of Group 1 instructions is used to access Group 3 instructions. Group 3 instructions are summarized in Table 5.

TABLE 5. GROUP 3 INSTRUCTIONS

INSTRUCTION BITS (I7-I0) OP CODE (HEX)	MNEMONIC	FUNCTION
08	SET1	Set Bit
18	SET0	Reset Bit
28	TB1	Test Bit (One)
38	TB0	Test Bit (Zero)
48	ABS	Absolute Value
58	SMTC	Sign Magnitude/Two's Complement
68	ADDI	Add Immediate
78	SUBI	Subtract Immediate
88		Reserved
98		Reserved
A8		Reserved
B8		Reserved
C8		Reserved
D8		Reserved
E8		Reserved
F8		Reserved

SN54AS887, SN74AS887 8-BIT PROCESSORS

set bit instruction (set1): I7-I0 = 0816

This instruction (Figure 3) is used to force selected bits to one (any combination of zero to eight bits). The desired bits are specified by an 8-bit mask (C3-C0):(A3-A0)† consisting of register file address ports that are not required to support this instruction. All bits that are in the same bit positions as ones in the mask are forced to a logical one. The B3-B0 address field is used for both source and destination of this instruction. The S bus is the source word for this instruction. $\overline{SIO0}$ must be forced low for proper operation. If $\overline{SIO0}$ is high, data on the S bus is passed unaltered. The status set by the set bit instruction is as follows:

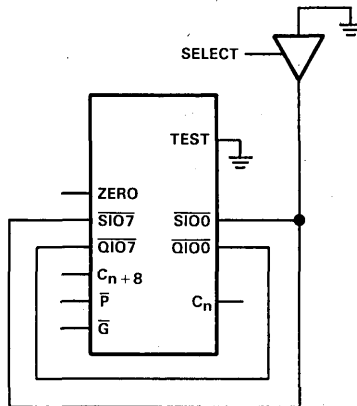
- N → None (force to zero)
- OVR → None (force to zero)
- C_n+8 → None (force to zero)
- Z → Result equal zero

† The symbol ':' is concatenation operator

reset bit instruction (set0): I7-I0 = 1816

This instruction (Figure 3) is used to force selected bits to zero. The desired bits are specified by an 8-bit mask (C3-C0):(A3-A0) consisting of register file address ports that are not required to support this instruction. All bits in the selected byte(s) that are in the same bit positions as ones in the mask are reset. The B3-B0 address field is used for both source and destination of this instruction. The S bus is the source word for this instruction. $\overline{SIO0}$ must be forced low for proper operation. If $\overline{SIO0}$ is high, data on the S bus is passed unaltered. The status set by the reset bit instruction is as follows:

- N → None (force to zero)
- OVR → None (force to zero)
- C_n+8 → None (force to zero)
- Z → Result equal zero



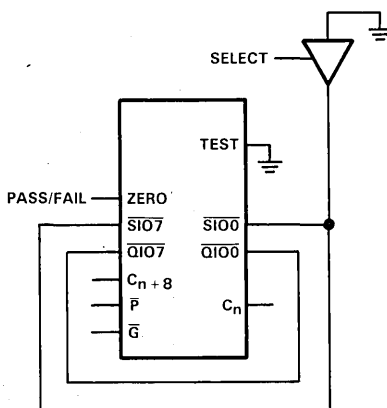
- NOTES: 1. Force $\overline{SIO0}$ low for proper operation.
2. Bit mask (C3-C0):(A3-A0) will set desired bits to one.

FIGURE 3. SET BIT (OR RESET BIT)

test bit (one) instruction (TB1): I7-I0 = 28₁₆

This instruction (Figure 4) is used to test selected bits for ones. Bits to be tested are specified by an 8-bit mask (C3-C0)::(A3-A0) consisting of register file address ports that are not required to support this instruction. Write Enable (\overline{WE}) is internally disabled during this instruction. The test will pass if the selected byte has ones at all bit locations specified by the ones of the mask (Figure 5). The S bus is the source word for this instruction. $\overline{SIO0}$ must be forced low for proper operation. The status set by the test bit (one) instruction is as follows:

- N → None (force to zero)
- OVR → None (force to zero)
- C_{n+8} → None (force to zero)
- Z → Pass



- NOTES: 1. Force $\overline{SIO0}$ low for proper operation.
2. Bit mask (C3-C0)::(A3-A0) will define bits for testing.
3. Pass/fail is indicated on Z output.

FIGURE 4. TEST BIT

test bit (zero) instruction (TB0): I7-I0 = 38₁₆

This instruction (Figure 4) is used to test selected bits for ones. Bits to be tested are specified by an 8-bit mask (C3-C0)::(A3-A0) consisting of register file address ports that are not required to support this instruction. Write Enable (\overline{WE}) is internally disabled during this instruction. The test will pass if the selected byte has zeros at all bit locations specified by the ones of the mask (Figure 6). The S bus is the source word for this instruction. $\overline{SIO0}$ must be forced low for proper operation. The status set by the test bit (zero) instruction is as follows:

- N → None (force to zero)
- OVR → None (force to zero)
- C_{n+8} → None (force to zero)
- Z → Pass

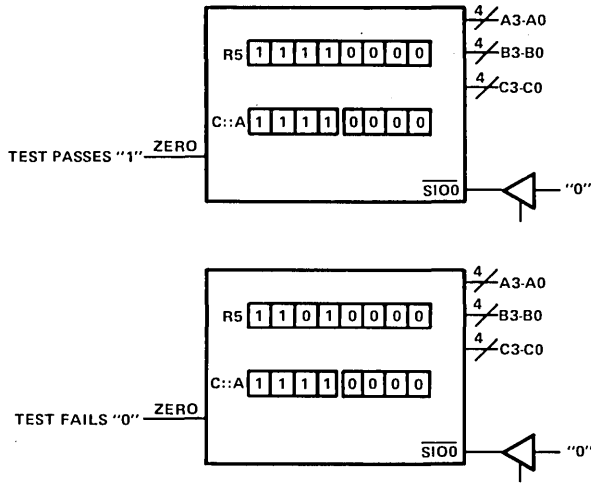


FIGURE 5. TEST BIT ONE EXAMPLES

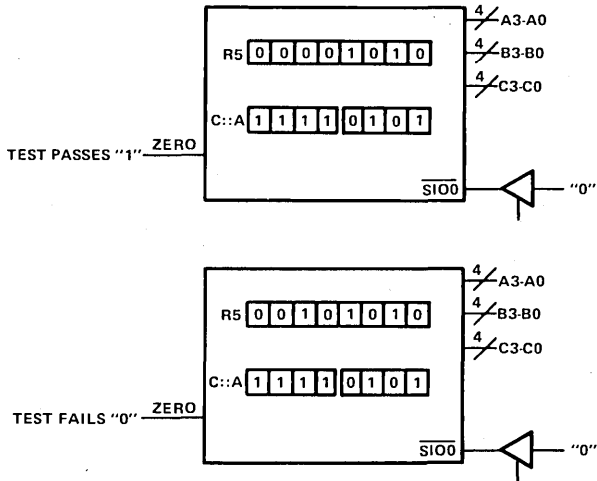


FIGURE 6. TEST BIT ZERO EXAMPLES

absolute value instruction (ABS): I7-I0 = 4816

This instruction is used to convert two's complement numbers to their positive value. The operand placed on the S bus is the source for this instruction. The 'AS887 will test the sign of the S bus and force the SSF pin to the proper value. The status set by the absolute value instruction is as follows:

- N → Input MSB equal one
- OVR → Input equal 80 (hex)
- C_{n+8} → S = 0
- Z → Result equal zero

sign magnitude/two's complement instruction (SMTC): I7-I0 = 5816

This instruction allows conversion from two's complement representation to sign magnitude representation, or vice-versa, in one clock cycle. The operand placed on the S bus is the source for this instruction.

When a negative zero (80 hex) is converted, the result is 00 with an overflow. If the input is in two's complement notation, the overflow indicates an illegal conversion. The status set by the sign magnitude/two's complement instruction is as follows:

- N → Result MSB equal one
- OVR → Input equal 80 (hex)
- C_{n+8} → Input equal 00 (hex)
- Z → Result equal zero

add immediate instruction (ADDI): I7-I0 = 6816

This instruction is used to add a specified constant value to the operand placed on the S bus. The constant will be between the values of 0 and 15. The constant value is specified by the unused register file address (A port) not required to support this instruction. Forcing the carry input will add an additional one to the result. The status set by the add immediate instruction is as follows:

- N → Result MSB equal one
- OVR → Arithmetic signed overflow
- C_{n+8} → Carry out equal one
- Z → Result equal zero

subtract immediate instruction (SUBI): I7-I0 = 7816

This instruction is used to subtract a specified constant value from the operand placed on the S bus. The constant value is specified by the unused register file address (A port) that is not required to support this instruction. The constant applied is the least significant four bits of a two's complement number. The device sign extends the constant over the entire word length. The status set by the subtract immediate instruction is as follows:

- N → Result MSB equal one
- OVR → Arithmetic signed overflow
- C_{n+8} → Carry out equal one
- Z → Result equal zero

group 4 instructions

Hex code 0 of Group 1 instructions is used to access Group 4 instructions. Group 4 instructions are summarized in Table 6.

TABLE 6. GROUP 4 INSTRUCTIONS

INSTRUCTION BITS (I7-I0) OP CODE (HEX)	MNEMONIC	FUNCTION
00		Reserved
10	SEL	Select S/R
20	SNORM	Single Length Normalize
30	DNORM	Double Length Normalize
40	DIVRF	Divide Remainder Fix
50	SDIVQF	Signed Divide Quotient Fix
60	SMULI	Signed Multiply Iterate
70	SMULT	Signed Multiply Terminate
80	SDIVIN	Signed Divide Initialize
90	SDIVIS	Signed Divide Start
A0	SDIVI	Signed Divide Iterate
B0	UDIVIS	Unsigned Divide Start
C0	UDIVI	Unsigned Divide Iterate
D0	UMULI	Unsigned Multiply Iterate
E0	SDIVIT	Signed Divide Terminate
F0	UDIVIT	Unsigned Divide Terminate

select S/R instruction (SEL): I7-I0 = 10₁₆

This instruction is used to pass either the S bus or the R bus to the output depending on the state of the SSF input pin. Normally, the preceding instruction would test the two operands and the resulting status information would be used to force the SSF input pin. SSF = 0 will output the R bus and SSF = 1 will output the S bus. The status set by the select S/R instruction is as follows:

- N → Result MSB equal one
- OVR → None (force to zero)
- C_n+8 → None (force to zero)
- Z → Result equal zero

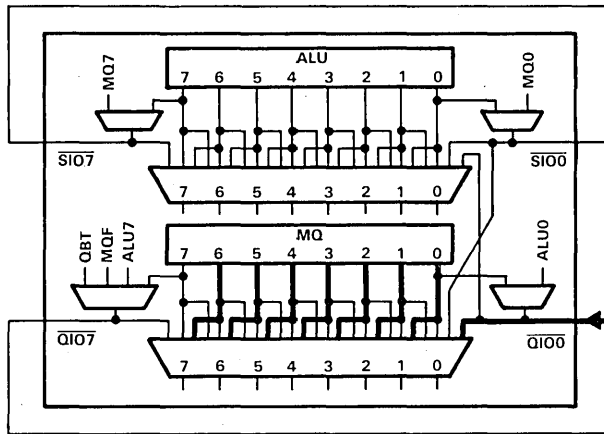
single-length normalize instruction (SNORM): I7-I0 = 20₁₆

This instruction will cause the contents of the MQ register to shift toward the most significant bit. Zeros are shifted in via the $\overline{Q100}$ input. The number of shifts performed can be counted and stored in one of the register files by forcing a high at the C_n input. When the two most significant bits are of opposite value, normalization is complete. This condition is indicated on the microcycle that completes the normalization at the OVR output.

The chip contains conditional logic that inhibits the shift function (and also inhibits the register file increment) if the number within the MQ register is already normalized at the beginning of the instruction (Figure 7). The status set by the single-length normalize instruction is as follows:

- N → MSB of result
- OVR → MSB XOR 2nd MSB
- C_n+8 → Carry out equal one
- Z → Result equal zero

SINGLE-LENGTH NORMALIZE



DOUBLE-LENGTH NORMALIZE

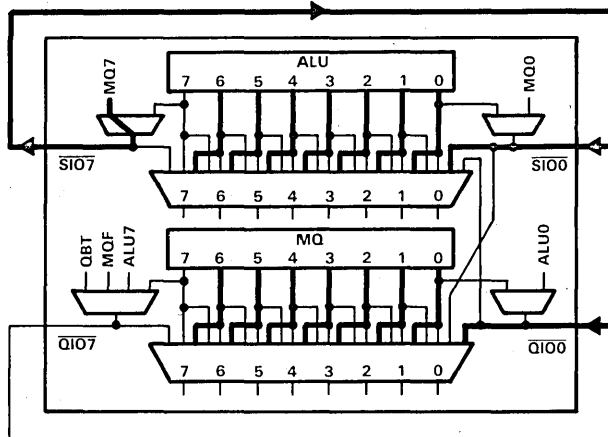


FIGURE 7. SINGLE- AND DOUBLE-LENGTH NORMALIZE

double-length normalize instruction (DNORM): 17-10 = 30₁₆

This instruction will cause the contents of a double-length word (register file contains the most significant half and the MQ register contains the least significant half) to shift toward the most significant bit. Zeros are shifted in via the \overline{QIOO} input. When the two most significant bits are of opposite value, normalization is complete. This condition is indicated on the microcycle that completes the normalization at the OVR output.

The chip contains conditional logic which inhibits the shift function if the number is already normalized at the beginning of the instruction (Figure 7). The most significant half of the operand must be placed on the S bus. The status set by the double-length normalize instruction is as follows:

- N → MSB of result
- OVR → MSB XOR 2nd MSB
- C_{n+8} → None (force to zero)
- Z → Result equal zero

multiply operations

The ALU performs three unique types of 8 by 8 multiplies each of which produces a 16-bit result (Figure 8). All three types of multiplication proceed via the following recursion:

- $P(J+1) = 2[P(J) + \text{Multiplicand} \times M(8-J)]$
- where
- $P(J) = \text{partial product at iteration number } J$
- $P(J+1) = \text{partial product at iteration number } J+1$
- J varies from 0 to 8
- M(8-J) = mode bit (unique to multiply type)
- 2 denotes some type of shift (unique to multiply)

Notice that by proper choice of mode terms and shifting operations, signed, unsigned, and mixed multiplies (signed times unsigned) may be performed.

All multiplies assume that the multiplier is stored in MQ before the operation begins (in the case of mixed multiply, the unsigned number must be the multiplier).

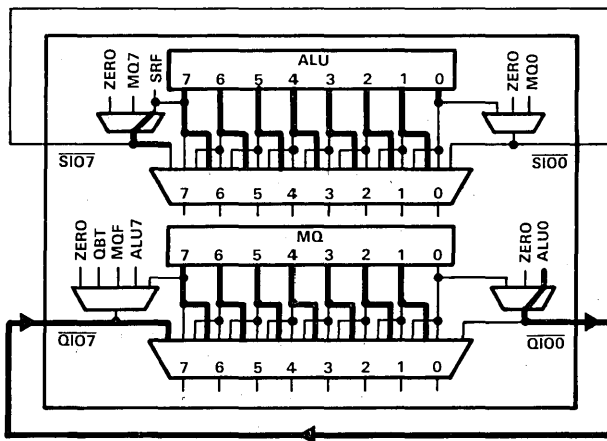
The processor has the following multiply instructions:

1. SIGNED MULTIPLY ITERATE (SMULI): 17-10 = 60₁₆
2. SIGNED MULTIPLY TERMINATE (SMULT): 17-10 = 70₁₆
3. UNSIGNED MULTIPLY ITERATE (UMULI): 17-10 = D0₁₆

The signed multiply iterate (SMULI) instruction performs a signed times signed iteration. This instruction interprets M(8-J) as the 8-J bit of the multiplier. The shift is a double-precision right shift one bit. This instruction is repeated 7 times for a 8 × 8 signed multiply. This instruction will be used 7 consecutive times for a mixed multiplication.

The signed multiply terminate (SMULT) instruction provides correct (negative) weighting of the sign bit of a negative multiplier in signed multiplication. The instruction is identical to signed multiply iterate (SMULI) except that M(8-J) is interpreted as -1 if the sign bit of the multiplier is 1, and 0 if the sign bit of the multiplier is 0.

SMULI, SMULT



UMULI

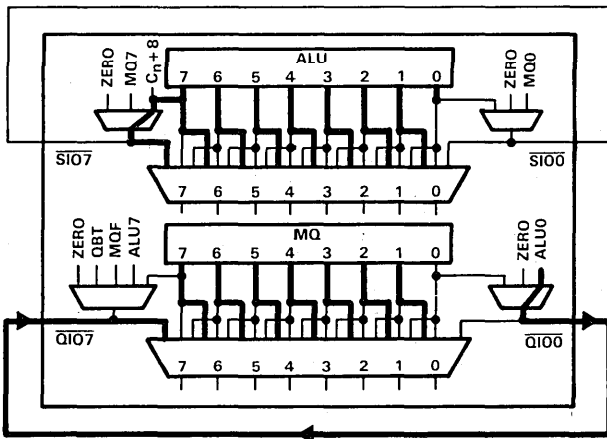


FIGURE 8. MULTIPLICATION OPERATIONS

2
LSI Devices

SN54AS887, SN74AS887 8-BIT PROCESSORS

The unsigned multiply iterate (UMULI) performs an unsigned multiplication iteration. This instruction interprets M(8-J) as the 8-J bit of the multiplier. The shift is a double-precision right shift with the carry out from the P(J) + Multiplcand \times M(8-J) operation forced into bit 8 of P(J + 1). This instruction is used in unsigned and mixed multiplication.

signed multiplication

Signed multiplication performs a ten clock cycle, two's complement multiply. The instructions necessary to produce an algebraically correct result proceed in the following manner:

Zero register to be used for accumulator

Load MQ with multiplier

SMULI (repeat 7 times) S port = Accumulator
 R port = Multiplicand
 F port = Iteration Result

SMULT S port = Accumulator
 R port = Multiplicand
 F port = Product (MSH)

At completion, the accumulator will contain the 8 most significant bits and MQ will contain the 8 least significant bits of the product.

The status for the signed multiply iterate should not be used for any testing (overflow is not set by SMULI). The following status is set for the signed multiply terminate instruction:

N \rightarrow Result MSB equal one
OVR \rightarrow Forced to zero
C_{n+8} \rightarrow Carry out equal to one
Z \rightarrow Double precision result is zero

unsigned multiplication

Unsigned multiplication produces an unsigned times unsigned product in ten clocks. The instructions necessary to produce an algebraically correct result proceed in the following manner:

Zero register to be used for accumulator

Load MQ with multiplier

UMULI (8 times) S port = Accumulator
 R port = Multiplicand
 F port = Iteration result (product MSH on final result)

Upon completion, the accumulator will contain the 8 most significant bits and MQ will contain the 8 least significant bits of the product.

The status set by the unsigned multiply iteration is meaningless except on the final execution of the instruction. The status set by the unsigned multiply iteration instruction is as follows:

- N → Result MSB equal one
- OVR → Forced to zero
- C_{n+8} → Carry out equal to one
- Z → Double-precision result is zero

mixed multiplication

Mixed multiplication multiplies a signed multiplicand times an unsigned multiplier to produce a signed result in ten clocks. The steps are as follows:

Zero register used for accumulator

Load MQ with unsigned multiplier

SMULI (8 times)

- S port = Accumulator
- R port = Multiplicand
- F port = Iteration result

Upon completion, the accumulator will contain the 8 most significant bits and MQ will contain the 8 least significant bits of the product.

The following status is set by the last SMULI instruction:

- N → Result MSB equal one
- OVR → Forced to zero
- C_{n+8} → Carry out equal to one
- Z → Double-precision result is zero

divide operations

The divide uses a nonrestoring technique to perform both signed and unsigned division of a 16 bit integer dividend and an 8 bit integer divisor (Figure 9). It produces an 8 integer quotient and remainder.

The remainder and quotient will be such that the following equation is satisfied:

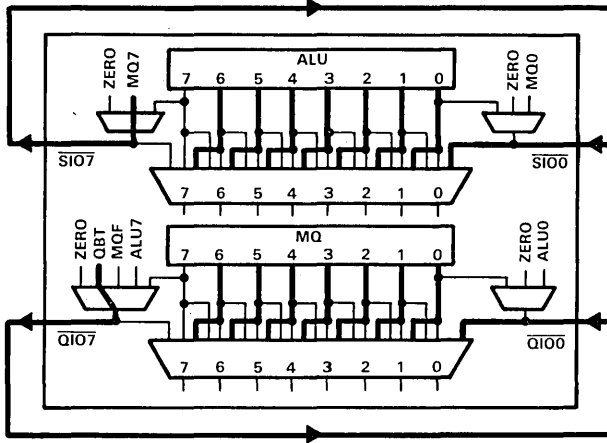
$$(\text{Quotient}) \times (\text{Divisor}) + \text{Remainder} = \text{Dividend}$$

The processor has the following divide instructions:

1. UNSIGNED DIVIDE START (UDIVIS): I7-I0 = B0₁₆
2. UNSIGNED DIVIDE ITERATE (UDIVI): I7-I0 = C0₁₆
3. UNSIGNED DIVIDE TERMINATE (UDIVIT): I7-I0 = F0₁₆
4. SIGNED DIVIDE INITIALIZE (SDIVIN): I7-I0 = 80₁₆
5. SIGNED DIVIDE OVERFLOW TEST (SDIVO): I7-I0 = AF₁₆
6. SIGNED DIVIDE START (SDIVIS): I7-I0 = 90₁₆
7. SIGNED DIVIDE ITERATE (SDIVI): I7-I0 = A0₁₆
8. SIGNED DIVIDE TERMINATE (SDIVIT): I7-I0 = E0₁₆
9. DIVIDE REMAINDER FIX (DIVRF): I7-I0 = 40₁₆
10. SIGNED DIVIDE QUOTIENT FIX (SDIVQF): I7-I0 = 50₁₆

SN54AS887, SN74AS887
8-BIT PROCESSORS

SDIVIN, SDIVS, SDIVI



SDIVT

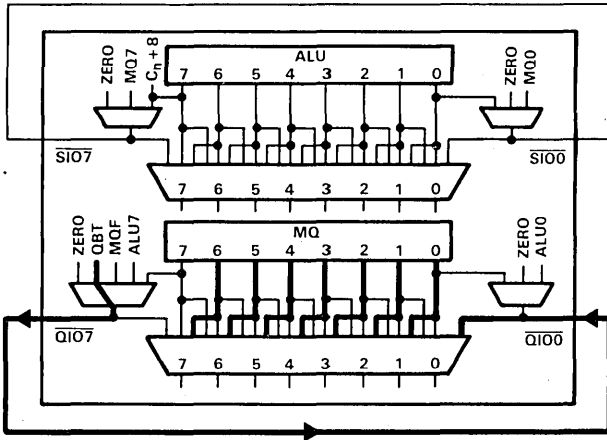


FIGURE 9. DIVIDE OPERATIONS

2

LSI Devices

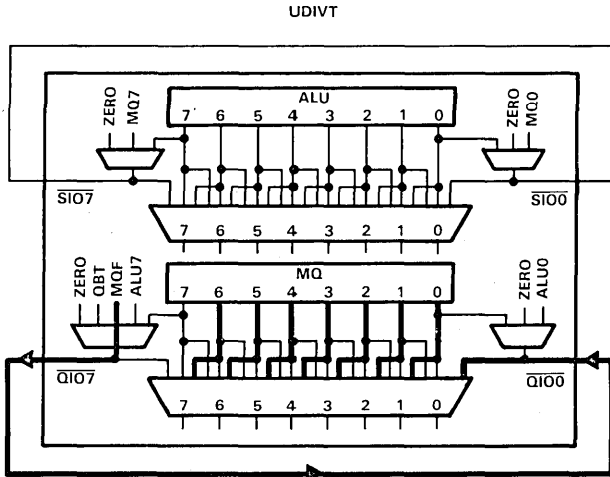
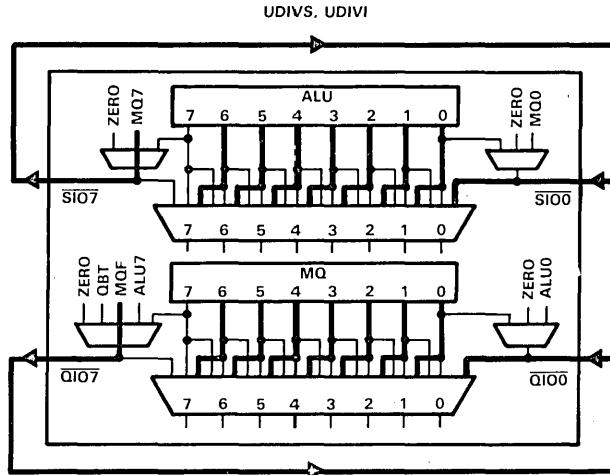


FIGURE 9. DIVIDE OPERATIONS (Continued)

The unsigned divide iterate start (UDIVIS) instruction begins the iterate procedure while testing for overflow. Overflow is reported when the first subtraction of the divisor from the MSH of the dividend produces carry out. The test detects quotient overflow and divide by zero.

The unsigned divide iterate terminate (UDIVIT) instruction completes the iterate procedure generating the last quotient bit.

The signed divide initialize (SDIVIN) instruction prepares for iteration by shifting the dividend and storing the sign of the dividend for use in the following instructions and overflow tests.

The signed divide overflow test (SDIVO) checks for overflow possibilities. This instruction may be deleted from the divide operation if the OVR pin is ignored. If it is removed some overflow conditions will go undetected. \overline{WE} must be high (writing inhibited) when this instruction is used.

The signed divide iterate start (SDIVIS) instruction calculates the difference between the divisor and MSH of the dividend. Partial detection of overflow is also done during this instruction. Operations with like signs (positive quotient) and division by zero will overflow during this instruction (including zero divisor). Operations with unlike signs are tested for overflow during the signed divide quotient fix instruction (SDIVQF). Partial overflow results are saved and will be used during SDIVQF when overflow is reported.

The signed divide iterate (SDIVI) instruction forms the quotient and remainder through iterative subtract/add-shift operations of the divisor and dividend. One quotient bit is generated on each clock.

The signed divide iterate terminate (SDIVIT) instruction completes the iterate procedure, generating the last quotient bit. It also tests for a remainder equal to zero, which determines the action to be taken in the following correction (fix) instructions.

The divide remainder fix (DIVRF) instruction corrects the remainder. If a zero remainder was detected by the previous instructions, the remainder is forced to zero. For nonzero remainder cases where the remainder and dividend have the same sign, the remainder is correct. When the remainder and dividend have unlike signs, a correction add/subtract of the divisor to the remainder is performed.

The signed divide quotient fix (SDIVQF) instruction corrects the quotient if necessary. This correction requires adding one to the incorrect quotient. An incorrect quotient results if the signs of the divisor and dividend differ and the remainder is nonzero. An incorrect quotient also results if the sign of the divisor is negative and the remainder is zero.

Overflow detection is completed during this instruction. Overflow may be generated for differing signs of the dividend and divisor. The partial overflow test result performed during SDIVIS is ORed with this test result to produce a true overflow indication.

signed divide usage

The instructions necessary to perform an algebraically correct division of signed numbers are as follows:

Load MQ with the least significant half of the dividend

SDIVIN	S port = MSH of dividend R port = Divisor F port = Intermediate result
SDIVO	S port = Result of SDIVIN R port = Divisor F port = Test result (WE must be high)
SDIVIS	S port = Result of SDIVIN R port = Divisor F port = Intermediate result
SDIVI (8N-2 times)	S port = Result of SDIVIS (or SDIVI) R port = Divisor F port = Intermediate result
SDIVIT	S port = Result of last SDIVI R port = Divisor F port = Intermediate result
DIVRF	S port = Result of SDIVIT R port = Divisor F port = Remainder
SDIVQF	S port = MQ register R port = Divisor F port = Quotient

The status of all signed divide instructions except SDIVIN, DIVRF, and SDIVQF is as follows:

N	→ Forced to zero
OVR	→ Forced to zero
C _{n+8}	→ Carry out equal to one
Z	→ Intermediate result is zero

The status of the SDIVIN instruction is as follows:

N	→ Forced to zero
OVR	→ Forced to zero
C _{n+8}	→ Forced to zero
Z	→ Divisor is zero

The status of the DIVRF instruction is as follows:

N	→ Forced to zero
OVR	→ Forced to zero
C _{n+8}	→ Carry out equal to one
Z	→ Remainder is zero

SN54AS887, SN74AS887 8-BIT PROCESSORS

The status of the SDIVQF instruction is as follows:

- N → Sign of quotient
- OVR → Divide overflow
- C_{n+8} → Carry out equal to one
- Z → Quotient is zero

The quotient is stored in the MQ register and the remainder is stored in the register file location that originally held the most significant word of the dividend. If fractions are divided, the quotient must be shifted right one bit and the remainder right three bits to obtain the correct fractional representations.

The signed division algorithm is summarized in Table 7.

TABLE 7. SIGNED DIVISION ALGORITHM

OP CODE	MNEMONIC	CLOCK CYCLES	INPUT S PORT	INPUT R PORT	OUTPUT F PORT
E4	LOADMQ	1	Dividend (LSH)	—	Dividend (LSH)
80	SDIVIN	1	Dividend (MSH)	Divisor	Remainder
AF	SDIVO	1	Remainder	Divisor	Test Result
90	SDIVIS	1	Remainder	Divisor	Remainder
A0	SDIVI	7	Remainder	Divisor	Remainder
E0	SDIVIT	1	Remainder	Divisor	Remainder (Unfixed)
40	DIVRF	1	Remainder (Unfixed)	Divisor	Remainder
50	SDIVQF	1	MQ Register	Divisor	Quotient

unsigned divide usage

The instructions necessary to perform an algebraically correct division of unsigned numbers are as follows:

Load MQ with the least significant half of the dividend

- UDIVIS S port = MSH of dividend
 R port = Divisor
 F port = Intermediate result
- UDIVI (8-1 times) S port = Result of UDIVIS (OR UDIVI)
 R port = Divisor
 F port = Intermediate result
- UDIVIT S port = Result of last UDIVI
 R port = Divisor
 F port = Remainder (unfixed)
- DIVRF S port = Result of UDIVIT
 R port = Divisor
 F port = Remainder

The status of all unsigned divide instructions except UDIVIS is as follows:

- N → Forced to zero
- OVR → Forced to zero
- C_{n+8} → Carry out equal to one
- Z → Intermediate result is zero

The status of the UDIVIS instruction is as follows:

- N → Forced to zero
- OVR → Divide overflow
- C_n+8 → Carry out equal to one
- Z → Intermediate result is zero

If fractions are divided, the remainder must be shifted right two bits to obtain the correct fractional representation. The quotient is correct as is. The quotient is stored in the MQ register at the completion of the divide.

The unsigned division algorithm is summarized in Table 8.

TABLE 8. UNSIGNED DIVISION ALGORITHM

OP CODE	MNEMONIC	CLOCK CYCLES	INPUT S PORT	INPUT R PORT	OUTPUT F PORT
E4	LOADMQ	1	Dividend (LSH)	—	Dividend (LSH)
B0	UDIVIS	1	Dividend (MSH)	Divisor	Remainder
C0	UDIVI	7	Remainder	Divisor	Remainder
F0	UDIVIT	1	Remainder	Divisor	Remainder (Unfixed)
40	DIVRF	1	Remainder (Unfixed)	Divisor	Remainder

group 5 instructions

Hex code F of Group 1 instructions is used to access Group 5 instructions. Group 5 instructions are summarized in Table 9.

TABLE 9. GROUP 5 INSTRUCTIONS

INSTRUCTION BITS (I7-I0) OP CODE (HEX)	MNEMONIC	FUNCTION
0F	CLR	Clear
1F	CLR	Clear
2F	CLR	Clear
3F	CLR	Clear
4F	CLR	Clear
5F	CLR	Clear
6F	CLR	Clear
7F	BCDBIN	BCD to Binary
8F		Reserved
9F	EX3C	Excess-3 Word Correction
AF	SDIVO	Signed Divide Overflow Check
BF	CLR	Clear
CF	CLR	Clear
DF	BINEX3	Binary to Excess-3
EF	CLR	Clear
FF	NOP	No Operation

SN54AS887, SN74AS887 8-BIT PROCESSORS

clear instructions (CLR)

There are 11 clear instructions listed in Table 9. The instructions force the ALU output to be zero and the BCD flip-flops to be cleared. The status set by the clear instruction is as follows:

N	→	None (force to zero)
OVR	→	None (force to zero)
C _{n+8}	→	None (force to zero)
Z	→	Active (one)

no operation instruction (NOP): I7-I0 = FF₁₆

This instruction is identical to the clear instructions except that the BCD flip-flops retain their old value.

excess-3 correction instructions (EX3C): 9F₁₆

This instruction corrects excess-3 additions (subtractions). For correct excess-3 arithmetic, this instruction must follow each add/subtract. The operand must be on the S port.

NOTE: The previous arithmetic overflow should be ignored.

The status set by the EX3C instruction is as follows:

N	→	MSB of result
OVR	→	Signed overflow
C _{n+8}	→	Carry out equal one
Z	→	None (force to one)

radix conversions

Conversions between decimal and binary number representations are performed with the aid of two special instructions: BINEX3 and BCDBIN.

BCD to binary instructions (BCDBIN): I7-I0 = 7F₁₆

This instruction (Figure 10) allows the user to convert a 2-digit BCD number to an 8-bit binary number in 12 clocks. This function sums the R bus, the S bus, and the C_n bit, performs an arithmetic left shift on the ALU result, and simultaneously circular shifts the MQ left. The status set by the BCD to binary instruction is as follows:

N	→	MSB of result
OVR	→	Signed arithmetic overflow [†]
C _{n+8}	→	Carry out equal one
Z	→	Result equal zero

[†] Overflow may be the result of an ALU operation or the arithmetic left shift operation.

The following code illustrates the BCD to binary conversion technique.

Let ACC be an accumulator register
Let NUM be the register which contains the BCD number
Let MSK be a mask register

```

LOADMQ NUM                ; LOAD MQ WITH BCD NUMBER
SUB ACC, ACC, SLCMQ       ; CLEAR ACC AND ALIGN MQ
SUB, MSK, MSK, SLCMQ      ; CLEAR MSK AND ALIGN MQ
SLCMQ                     ; ALIGN
SLCMQ                     ; ALIGN
ADDI ACC, MSK, 1510       ; MSK = 1510
AND MQ, MSK, R1, SLCMQ    ; EXTRACT ONE DIGIT
                           ; ALIGN MQ
ADD, ACC, R1, R1, SLCMQ   ; ACC + DIGIT
                           ; IS STORED IN R1
                           ; ALIGN MQ
BCDBIN, R1, R1, ACC       ; 4 × (ACC + DIGIT)
                           ; IS STORED IN ACC
                           ; ALIGN MQ
BCDBIN, ACC, R1, ACC      ; 10 × (ACC + DIGIT)
                           ; IS STORED IN ACC
                           ; ALIGN MQ
AND MQ, MSK, R1          ; FETCH LAST DIGIT
ACC+R1 → ACC             ; ADD IN LAST DIGIT
    
```

The previous code generates a binary number by executing the standard conversion formula for a 2-digit BCD number.

$$AB = A \times 10 + B$$

Notice that the conversion begins with the most significant BCD digit and that the addition is performed in radix 2.

binary to excess-3 instructions (BINEX3): I7-I0 = DF16

This instruction (Figure 11) allows the user to convert an 8-bit binary number to 2-digit excess-3 number representation in 19 clocks. The data on the R and S ports are summed with the MSB of the MQ register. The MQ register is simultaneously shifted left circularly. The status set by the binary to excess-3 instruction is as follows:

N → MSB of result
OVR → Signed arithmetic overflow
C_n+8 → Carry out equal one
Z → Result equal zero

BCDBIN

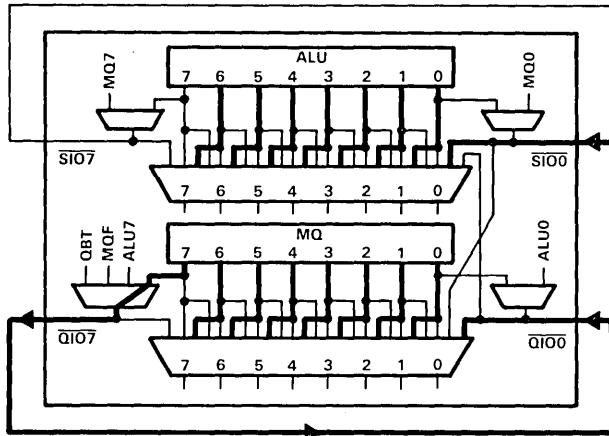


FIGURE 10. BCD TO BINARY

BINEX3

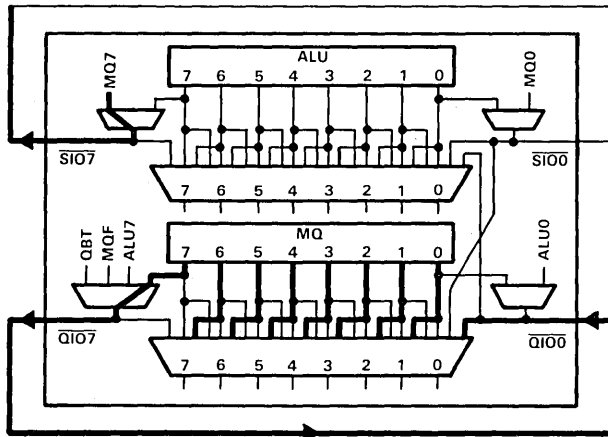


FIGURE 11. BINARY TO EXCESS-3

The following illustrates the binary to excess-3 conversion technique.

Let NUM be a register containing an unsigned binary number
Let ACC be an accumulator

```

M1:      LOADMQ NUM                      ; LOAD MQ WITH BINARY
                                                ; NUMBER
M2:      CLEAR ACC                      ; CLEAR ACC
M3:      SET1 ACC H/33/                 ; ACC → HEX/3333 . . .
L1:      BINEX3 ACC, ACC, ACC           ; DOUBLE ACC AND ADD IN
                                                ; MSB OF MQ
                                                ; ALIGN MQ
L2:      EX3C ACC, ACC                  ; EXCESS 3 CORRECT
                                                ; REPEAT L1 AND L2
                                                ; 7 TIMES
    
```

The previous code generates an excess-3 number by executing the standard conversion formula for a binary number.

$$a_n 2^n + a_{n-1} 2^{n-1} + a_{n-2} 2^{n-2} + \dots + a_0 2^0 = [(2a_n + a_{n-1})2 + a_{n-2}]2 + \dots + a_0$$

Notice that the conversion begins with the most significant binary bit and that the addition is performed in radix-10 (excess-3).

decimal arithmetic

Decimal numbers are represented in excess-3 code. Excess-3 code numbers may be generated by adding three to each digit of a Binary Coded Decimal (BCD) number. The hardware necessary to implement excess-3 arithmetic is only slightly different from binary arithmetic. Carries from one digit to another during addition in BCD occur when the sum of the two digits plus the carry-in is greater than or equal to ten. If both numbers are excess-3, the sum will be excess-6, which will produce the proper carries. Therefore, every addition or subtraction operation may use the binary adder. To convert the result from excess-6 to excess-3, one must consider two cases resulting from a BCD digit add: (1) where a carry-out is produced, and (2) where a carry-out is not produced. If a carry-out is not produced, three must be subtracted from the resulting digit. If a carry is produced, the digit is correct as a BCD number. For example, if BCD 5 is added to BCD 6, the excess-3 result would be $8 + 9 = 1$ (with a carry). A carry rolls the number through the illegal BCD representations into a correct BCD representation. Binary 3 must be added to digit positions that produce a carry-out to correct the result to an excess-3 representation. Every addition and subtraction instruction stores the carry generated from each 4-bit digit location for use by the excess-3 correction function. The correction instruction must be executed in the clock cycle immediately after the addition or subtraction operation.

SN54AS887, SN74AS887 8-BIT PROCESSORS

absolute maximum rating over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1}	7 V
Supply voltage, V_{CC2}	3 V
Input voltage	7 V
High-level voltage applied to 3-state outputs	5.5 V
Operating case temperature range: SN54AS887	-55°C to 125°C
Operating free-air temperature range: SN74AS887, SN74AS887-1	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54AS887			SN74AS887 SN74AS887-1			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC1}	I/O supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{CC2}	STL internal logic supply voltage	1.9	2	2.1	1.9	2	2.1	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage				0.8			V
I_{OH}	High-level output current				-1			-2.6 mA
I_{OL}	Low-level output current	All output except N and ZERO			8			8 mA
		N			16			16 mA
		ZERO			48			48 mA
T_C	Operating case temperature	-55			125			°C
T_A	Operating free-air temperature				0			

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54AS887			SN74AS887 SN74AS887-1			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		$V_{CC1} = 4.5 V, I_I = -18 mA$	-1.2			-1.2			V
V_{OH}	All outputs except ZERO	$V_{CC1} = 4.5 V \text{ to } 5.5 V, I_{OH} = -0.4 mA$	$V_{CC}-2$			$V_{CC}-2$			V
		$V_{CC1} = 4.5 V, I_{OH} = -1 mA$	2.4						
		$V_{CC1} = 4.5 V, I_{OH} = -2.6 mA$				2.4			
I_{OH}	ZERO	$V_{CC1} = 4.5 V, V_{OH} = 5.5 V$	0.1			0.1			mA
V_{OL}	All outputs except N and ZERO	$V_{CC1} = 4.5 V, I_{OL} = 8 mA$	0.5			0.5			V
		$V_{CC1} = 4.5 V, I_{OL} = 16 mA$	0.5			0.5			
		$V_{CC1} = 4.5 V, I_{OL} = 48 mA$	0.5			0.5			
I_I	I/O	$V_{CC1} = 5.5 V, V_I = 5.5 V$	0.1			0.1			mA
	All others	$V_{CC1} = 5.5 V, V_I = 7 V$	0.1			0.1			
I_{IH}^\ddagger		$V_{CC1} = 5.5 V, V_I = 2.7 V$	20			20			μA
I_{IL}^\ddagger		$V_{CC1} = 5.5 V, V_I = 0.5 V$	-0.4			-0.4			mA
I_{O}^\S		$V_{CC1} = 5.5 V, V_O = 2.25 V$	-30	-112		-30	-112	mA	
I_{CC1}		$V_{CC1} = 5.5 V$	150			130			mA
I_{CC2}		$V_{CC2} = 2.1 V$	410			390			mA

† All typical values are at $V_{CC} = 5 V, T_A = 25^\circ C$.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state current.

§ The output conditions have been chosen to produce a current that closely approximates one-half the true short-circuit current, I_{OS} .

2 LSI Devices

SN54AS887, SN74AS887
8-BIT PROCESSORS

SN54AS887 maximum switching characteristics, $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $T_C = -55^\circ\text{C to }125^\circ\text{C}$ (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)										UNIT
		Y	C_{n+8}	\bar{G}, \bar{P}	Z^{\dagger}	N	OVR	DA	DB	$\bar{Q}iO$	$\bar{S}iO$	
t_{pd}	A3-A0 B3-B0	62	42	48	69	62	60	18	18	65	66	ns
	DA7-DA0, DB7-DB0	47	28	28	58	50	42	—	—	50	50	
	C_n	25	14	—	32	24	18	—	—	32	32	
	$\bar{E}A$	54	32	35	62	52	52	—	—	58	58	
	$\bar{E}B$	54	32	35	62	52	52	—	—	58	58	
	17-10	58	32	32	62	52	41	—	—	58	58	
	$\bar{O}E\bar{B}$	—	—	—	—	—	—	—	14	—	—	
	$\bar{O}EY$	14	—	—	—	—	—	—	—	—	—	
	$\bar{Q}iO$ (n) Shift	15	—	—	24	—	—	—	—	—	—	
	$\bar{S}iO$ (n) Shift	15	—	—	24	22	—	—	—	—	—	
	CK	68	60	56	62	50	68	38	38	70	70	
	$\bar{O}E\bar{A}$	—	—	—	—	—	—	14	—	—	—	

\dagger Load resistor $R_1 = 100\ \Omega$.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN74AS887 maximum switching characteristics, $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $T_A = 0^\circ\text{C to }70^\circ\text{C}$ (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)										UNIT
		Y	C_{n+8}	\bar{G}, \bar{P}	Z^{\dagger}	N	OVR	DA	DB	$\bar{Q}iO$	$\bar{S}iO$	
t_{pd}	A3-A0 B3-B0	54	36	42	60	52	50	18	18	58	58	ns
	DA7-DA0, DB7-DB0	44	26	26	52	46	38	—	—	44	44	
	C_n	25	8	—	32	24	18	—	—	31	31	
	$\bar{E}A$	49	29	29	58	49	47	—	—	54	54	
	$\bar{E}B$	49	29	29	58	49	47	—	—	54	54	
	17-10	55	30	30	60	49	39	—	—	54	54	
	$\bar{O}E\bar{B}$	—	—	—	—	—	—	—	12	—	—	
	$\bar{O}EY$	12	—	—	—	—	—	—	—	—	—	
	$\bar{Q}iO$ (n) Shift	15	—	—	24	—	—	—	—	—	—	
	$\bar{S}iO$ (n) Shift	15	—	—	24	19	—	—	—	—	—	
	CK	58	55	52	61	52	62	35	35	60	60	
	$\bar{O}E\bar{A}$	—	—	—	—	—	—	12	—	—	—	

\dagger Load resistor $R_1 = 100\ \Omega$.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

2

LSI Devices

SN54AS887, SN74AS887 8-BIT PROCESSORS

SN74AS887-1 maximum switching characteristics, $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $T_A = 0^\circ\text{C to }70^\circ\text{C}$ (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)										UNIT
		Y	C _{n+8}	\bar{G}, \bar{P}	Z [†]	N	OVR	DA	DB	$\bar{Q}iO$	$\bar{S}iO$	
t _{pd}	A3-A0 B3-B0	44	30	36	50	44	44	17	17	48	48	ns
	DA7-DA0, DB7-DB0	36	24	24	46	41	32	—	—	40	40	
	C _n	22	8	—	27	21	16	—	—	25	25	
	$\bar{E}A$	40	25	25	49	41	41	—	—	44	44	
	$\bar{E}B$	40	25	25	49	41	41	—	—	44	44	
	I7-I0	46	27	27	50	42	35	—	—	45	45	
	$\bar{O}E\bar{B}$	—	—	—	—	—	—	—	12	—	—	
	$\bar{O}E\bar{Y}$	12	—	—	—	—	—	—	—	—	—	
	$\bar{Q}iO$ (n) Shift	14	—	—	20	—	—	—	—	—	—	
	$\bar{S}iO$ (n) Shift	14	—	—	20	18	—	—	—	—	—	
	CK	50	46	46	50	50	50	30	30	50	50	
$\bar{O}E\bar{A}$	—	—	—	—	—	—	—	12	—	—		

† Load resistor R1 = 100 Ω.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

register file write setup and hold times

PARAMETER	SN54AS887		SN74AS887		SN74AS887-1		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
t _{su}	C3-C0	8	7	6			ns
	DB [§]	14	12	11			
	I7-I4	16	14	13			
	I3-I0	24	22	21			
	$\bar{O}E\bar{Y}$	4	3	3			
	Y7-Y0	2	2	2			
	$\bar{W}E$	8	6	6			
	$\bar{Q}iO$ (n), $\bar{S}iO$ (n)	6	5	5			
t _h	SELY	8	6	6			ns
	C3-C0	0	0	0			
	DB [§]	0	0	0			
	I7-I4	0	0	0			
	I3-I0	0	0	0			
	$\bar{O}E\bar{Y}$	6	5	5			
	Y7-Y0	10	10	10			
	$\bar{W}E$	3	2	2			
$\bar{Q}iO$ (n), $\bar{S}iO$ (n)	0	0	0				
SELY	8	6	6				

§ DB (during select instruction) through Y port.

special instruction switching characteristics

The SSF pin is used internally during certain instructions. The following tables list the instructions which force the SSF pin during their execution. The propagation delay from various inputs is also shown. The parameter which limits normal system performance is indicated by a dagger.

SN54AS887 SSF PIN DELAYS AND SETUP TIMES

MNEMONIC	HEX CODE	INPUT → SSF (ns)				SSF SETUP TIME (ns)
		C _n	I _(n)	CK	B _(n)	
SNORM	20	—	29 [†]	46	—	20
DNORM	30	—	29	55	40 [†]	20
DIVRF	40	—	29 [†]	46	—	20
SDIVQF	50	—	26 [†]	—	—	18
SMULI	60	—	26 [†]	43	—	0
SDIVIN	80	—	48	64	44 [†]	0
SDIVIS	90	26 [†]	51	64	55	0
SDIVI	A0	26 [†]	51	64	55	0
UDIVIS	B0	18 [†]	45	64	46	0
UDIVI	C0	18 [†]	50	54	40	0
UMULI	D0	—	25 [†]	48	—	0
SDIVIT	E0	26 [†]	50	56	54	0
ABX	48	—	34	62	39 [†]	20
SMTC	58	—	29	58	39 [†]	20
BINEX3	DF	—	29 [†]	58	—	18
LOADMQ (Arith)		23 [†]	34	62	40	0
LOADMQ (Log)		—	33	62	40 [†]	0

[†] This parameter limits normal system performance.

SN54AS887, SN74AS887
8-BIT PROCESSORS

SN74AS887 SSF PIN DELAYS AND SETUP TIMES

MNEMONIC	HEX CODE	INPUT → SSF (ns)				SSF SETUP
		C _n	I _(n)	CK	B _(n)	TIME (ns)
SNORM	20	—	26 [†]	40	—	17
DNORM	30	—	26	52	37 [†]	17
DIVRF	40	—	26 [†]	40	—	17
SDIVQF	50	—	25 [†]	—	—	17
SMULI	60	—	25 [†]	40	—	0
SDIVIN	80	—	38	60	40 [†]	0
SDIVIS	90	24 [†]	48	60	52	0
SDIVI	A0	24 [†]	48	60	52	0
UDIVIS	80	17 [†]	43	60	45	0
UDIVI	C0	17 [†]	44	52	37	0
UMULI	D0	—	26 [†]	40	—	0
SDIVIT	E0	25 [†]	46	52	49	0
ABX	48	—	32	60	38	17
SMTC	58	—	26	52	38 [†]	17
BINEX3	DF	—	26 [†]	40	—	17
LOADMQ (Arith)		22 [†]	32	50	38	0
LOADMQ (Log)		—	32	50	38 [†]	0

[†] This parameter limits normal system performance.

2

LSI Devices

SN74AS887-1 SSF PIN DELAYS AND SETUP TIMES

MNEMONIC	HEX CODE	INPUT → SSF (ns)				SSF SETUP
		C _n	I _(n)	CK	B _(n)	TIME (ns)
SNORM	20	—	23 [†]	28	—	14
DNORM	30	—	23	40	34 [†]	14
DIVRF	40	—	23 [†]	27	—	14
SDIVQF	50	—	23 [†]	—	—	14
SMULI	60	—	22 [†]	27	—	0
SDIVIN	80	—	35	46	35 [†]	0
SDIVIS	90	22 [†]	42	48	42	0
SDIVI	A0	22 [†]	42	46	42	0
UDIVIS	B0	16 [†]	42	46	38	0
UDIVI	C0	16 [†]	36	46	34	0
UMULI	D0	—	22 [†]	27	—	0
SDIVIT	E0	21 [†]	40	44	42	0
ABX	48	—	28	46	30 [†]	14
SMTC	58	—	24	44	30 [†]	14
BINEX3	DF	—	23 [†]	27	—	14
LOADMQ (Arith)		19 [†]	28	40	30	0
LOADMQ (Log)		—	28	35	30 [†]	0

[†] This parameter limits normal system performance.

2

LSI Devices

SN54AS888, SN74AS888 8-BIT PROCESSOR SLICES

MARCH 1985—REVISED JANUARY 1986

- STL-AS Technology
- Parallel 8-Bit ALU with Expansion Inputs and Outputs
- 13 Arithmetic and Logic Functions
- 8 Conditional Shifts (Single and Double Length)
- 9 Instructions that Manipulate Bytes
- 4 Instructions that Manipulate Bits
- Add and Subtract Immediate Instructions
- Absolute Value Instruction
- Signed Magnitude to/from Two's Complement Conversion
- Single- and Double-Length Normalize
- Select Functions
- Signed and Unsigned Divides with Overflow Detection; Input does not Need to be Prescaled
- Signed, Mixed, and Unsigned Multiplies
- Three-Operand, 16-Word Register File
- Full Carry Look Ahead Support
- Sign, Carry Out, Overflow, and Zero-Detect Status Capabilities
- Excess-3 BCD Arithmetic
- Internal Shift Multiplexers that Eliminate the Need for External Shift Control Parts
- ALU Bypass Path to Increase Speeds of Multiply, Divide, and Normalize Instructions and to Provide New Instructions such as Bit Set, Bit Reset, Bit Test, Byte Subtract, Byte Add, and Byte Logical
- 3-Operand Register Files to Allow an Operation and a Move Instruction to be Combined
- Byte Select Controlled by External 3-State Buffers that may be Eliminated if Bit and Byte Manipulation are not Needed
- Bit and Byte Masks that are Shared with Register Address Fields to Minimize Control Store Word Width
- 3 Data Input/Output Paths to Maximize Data Throughput

description

These 8-bit Advanced Schottky TTL integrated circuits are designed to implement high performance digital computers or controllers. An architecture and instruction set has been chosen that supports a fast system clock, a narrow micro-code word width, and a high system throughput. The powerful instruction set allows high-speed system architecture to be implemented and also allows an existing system's performance to be upgraded while protecting software investments. These processors are designed to be cascadable to any word width 16 bits or greater.

The SN54AS888 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AS888 and SN74AS888-1 are characterized for operation from 0°C to 70°C .

Package options include both plastic and ceramic chip carriers in addition to a 68-pin grid array ceramic package.

2

LSI Devices

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS



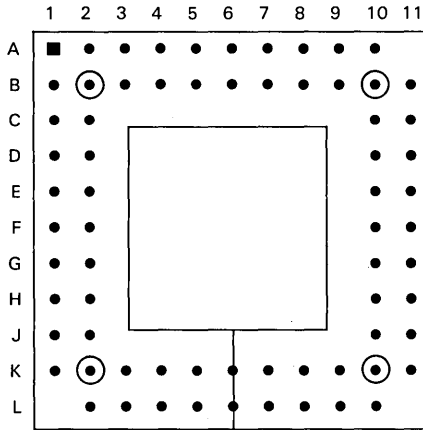
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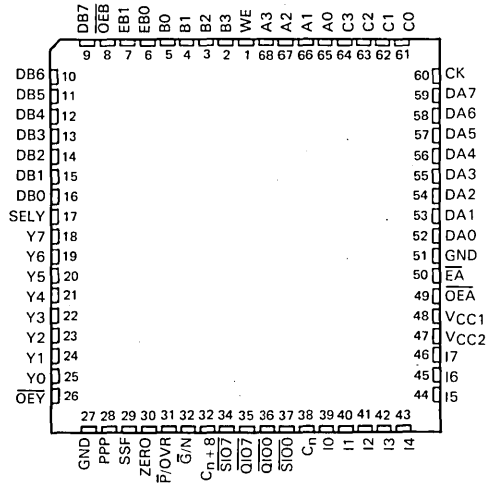
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SN54AS888, SN74AS888 8-BIT PROCESSOR SLICES

SN54AS888, SN74AS888 . . . GB PACKAGE
(TOP VIEW)



SN54AS888 . . . FK PACKAGE
SN74AS888 . . . FN PACKAGE
(TOP VIEW)



GB PACKAGE PIN ASSIGNMENTS

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
A-2	C _n	B-9	OEY	F-10	Y3	K-4	C2
A-3	SIO0	B-10	Y0	F-11	DB2	K-5	A0
A-4	QIO0	B-11	Y1	G-1	DA2	K-6	A3
A-5	QIO7	C-1	I5	G-2	DA0	K-7	WE
A-6	C _n +8	C-2	VCC2	G-10	DB0	K-8	DB7
A-7	G/N	C-10	Y4	G-11	DB3	K-9	OEB
A-8	P/OVR	C-11	Y6	H-1	DA3	K-10	EBO
A-9	ZERO	D-1	I6	H-2	DA1	K-11	EB1
A-10	PPP	D-2	VCC1	H-10	DB6	L-2	CK
B-1	I2	D-10	Y5	H-11	DB4	L-3	C1
B-2	I3	D-11	Y7	J-1	DA4	L-4	C3
B-3	I1	E-1	I7	J-2	DA5	L-5	A1
B-4	I0	E-2	OEA	J-10	SELY	L-6	A2
B-5	I4	E-10	Y2	J-11	DB5	L-7	B3
B-6	SIO7	E-11	DB1	K-1	DA6	L-8	B2
B-7	SSF	F-1	EA	K-2	DA7	L-9	B1
B-8		F-2	GND	K-3	CO	L-10	B0

PIN FUNCTIONAL DESCRIPTION

PIN GRID ARRAY	CHIP CARRIER	NAME	I/O	DESCRIPTION
A-10	28	PPP	I	Package position pin. Tri-level input used to define package significance during instruction execution. Leave open for intermediate positions, tie to V _{CC} for most significant package, and tie to GND for least significant package.
B-7	29	SSF	I/O	Special shift function. Used to transfer required information between packages during special instruction execution.
A-9	30	ZERO	I/O	Device zero detection, open collector. Input during certain special instructions.
A-8	31	P/OVR	O	ALU propagate/instruction overflow for most significant package, low active.
A-7	32	Ḡ/N	O	ALU generate/negative result for most significant package, low active.
A-6	33	C _{n+8}	O	ALU ripple carry output.
B-6	34	SIO7	I/O	Bidirectional shift pin, low active.
A-5	35	Q̄IO7	I/O	
A-4	36	Q̄IO0	I/O	
A-3	37	SIO0	I/O	
A-2	38	C _n	I	ALU carry input.
B-4	39	I0	I	Instruction input.
B-3	40	I1	I	
B-1	41	I2	I	
B-2	42	I3	I	
B-5	43	I4	I	
C-1	44	I5	I	
D-1	45	I6	I	
E-1	46	I7	I	
C-2	47	VCC2		Low voltage power supply (2 V).
D-2	48	VCC1		I/O interface supply voltage (5 V).
E-2	49	OĒA	I	DA bus enable, low active.
F-1	50	ĒA	I	ALU input operand select. High state selects external DA bus and low state selects register file.
F-2	51	GND		Ground pin.
G-2	52	DA0	I/O	A port data bus. Outputs register file data (ĒA = 0) or inputs external data (ĒA = 1).
H-2	53	DA1	I/O	
G-1	54	DA2	I/O	
H-1	55	DA3	I/O	
J-1	56	DA4	I/O	
J-2	57	DA5	I/O	
K-1	58	DA6	I/O	
K-2	59	DA7	I/O	
L-2	60	CK	I	Clocks all synchronous registers on positive edge.
K-3	61	C0	I	Register file write address select.
L-3	62	C1	I	
K-4	63	C2	I	
L-4	64	C3	I	
K-5	65	A0	I	Register file A port read address select.
L-5	66	A1	I	
L-6	67	A2	I	
K-6	68	A3	I	

SN54AS888, SN74AS888
8-BIT PROCESSOR SLICES

PIN FUNCTIONAL DESCRIPTION

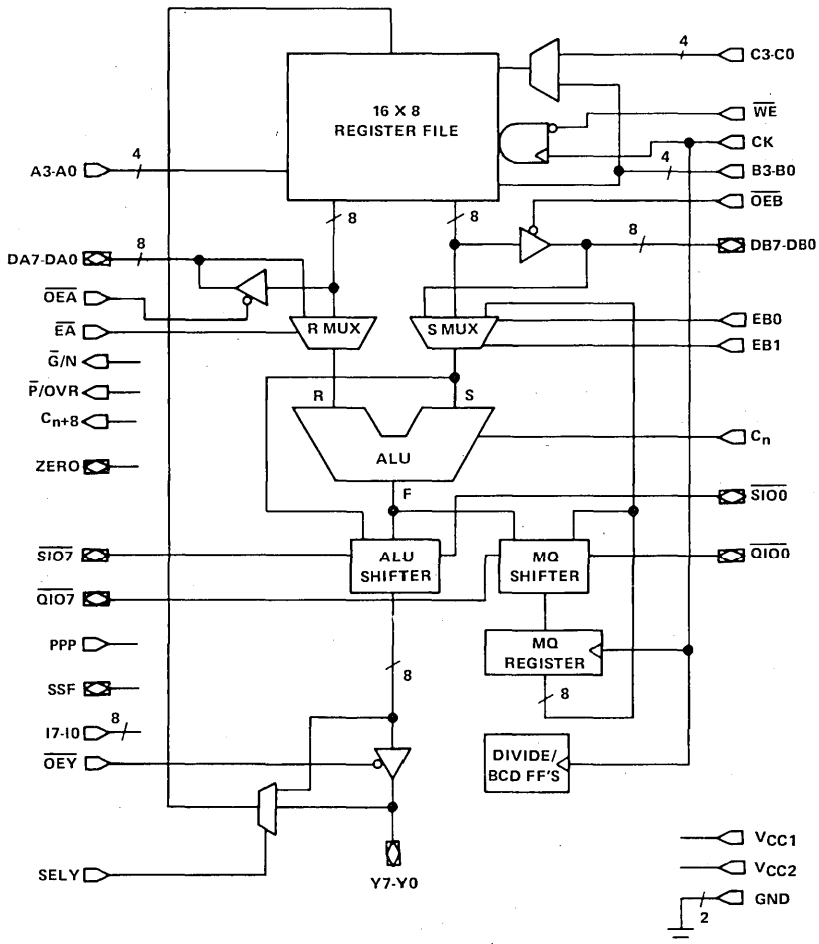
PIN GRID ARRAY	CHIP CARRIER	NAME	I/O	DESCRIPTION
K-7	1	\overline{WE}	I	Register file (RF) write enable. Data is written into RF when \overline{WE} is low and a low-to-high clock transition occurs. RF write is inhibited when \overline{WE} is high.
L-7	2	B3	I	Register file B port read address select. (0 = LSB).
L-8	3	B2	I	
L-9	4	B1	I	
L-10	5	B0	I	
K-10	6	EBO	I	ALU input operand select. EBO and EB1 selects the source of data that the S multiplexer provides for the S bus. Independent control of the DB bus and data path selection allow the user to isolate the DB bus while the ALU continues to process data.
K-11	7	EB1	I	
K-9	8	\overline{OEB}	I	DB bus enable, low active.
K-8	9	DB7	I/O	B port data bus. Outputs register data ($\overline{OEB} = 0$) or used to input external data ($\overline{OEB} = 1$), (0 = LSB).
H-10	10	DB6	I/O	
J-11	11	DB5	I/O	
H-11	12	DB4	I/O	
G-11	13	DB3	I/O	
F-11	14	DB2	I/O	
E-11	15	DB1	I/O	
G-10	16	DB0	I/O	
J-10	17	SELY	I	Y bus select, high active.
D-11	18	Y7	I/O	Y port data bus. Outputs instruction results ($\overline{OEY} = 0$) or used to put external data into register file ($\overline{OEY} = 1$).
C-11	19	Y6	I/O	
D-10	20	Y5	I/O	
C-10	21	Y4	I/O	
F-10	22	Y3	I/O	
E-10	23	Y2	I/O	
B-11	24	Y1	I/O	
B-10	25	Y0	I/O	
B-9	26	\overline{OEY}	I	Y bus output enable, low active.
F-2	27	GND		Ground pin

2

LSI Devices

SN54AS888, SN74AS888
8-BIT PROCESSOR SLICES

functional block diagram



2
LSI Devices

SN54AS888, SN74AS888

8-BIT PROCESSOR SLICES

architectural elements

3-port register file

Working registers consist of 128 storage elements organized into sixteen 8-bit words. These storage elements appear to the user as 16 positive edge-triggered registers. The three port addresses, one write (C) and two reads (A and B), are completely independent of each other to implement a 3-operand register file. Data is written into the register file when \overline{WE} is low and a low-to-high clock transition occurs. The ADD and SUBTRACT immediate instructions require only one source operand. The B address is used as the source address, and the bits of the A address are used to provide a constant field. The SET, RESET, and TEST BIT instructions use the B addressed register as both the source and destination register while the A and C addresses are used as masks. These instructions are explained in more detail in the instruction section.

S multiplexer

The S multiplexer selects the ALU operand, as follows:

EB1	EBO	S bus
Low	Low	RF data
Low	High	MQ data
High	Low	DB data
High	High	MQ data

DB port

Data is passed through the ALU or received from the register file on the 8-bit DB port. If \overline{OEB} is low, the DB bus is active; if \overline{OEB} is high, the DB bus is in the high impedance state. Notice that the DB port may be isolated at the same time that register file data is passed to the ALU.

R multiplexer

The R multiplexer selects the other operand of the ALU. Except for those instructions that require constants or masks, the R bus will contain DA if \overline{EA} is high or the RF data pointed to by A if \overline{EA} is low.

DA bus

The DA bus is active (with register file data) if \overline{OEA} is low. Notice that the DA bus may be isolated while register file data is passed to the ALU.

ALU

The shift instructions are summarized in Table 4 and illustrated in Figure 2. The ALU can perform seven arithmetic and six logical instructions on two 8-bit operands. It also supports multiplication, division, normalization, bit set, reset, test, byte operations, and excess-3 BCD arithmetic. These source operands are the outputs of the S and R multiplexers.

ALU and MQ shifters

ALU and MQ shifters perform all of the shift, multiply, divide, and normalize functions. Table 4 shows the value of the $\overline{SIO7}$ and $\overline{QIO7}$ pins of the most significant package. The standard shifts may be made into conditional shifts and the serial data may be input or output with the aid of two three-state gates. These capabilities are discussed further in the arithmetic and logic section.

2

LSI Devices

MQ register

The multiplier-quotient (MQ) register has specific functions in multiplication, division, and normalization. This register may also be used as a temporary storage register. The MQ register may be loaded if the instruction code on pins 17-10 is E1-E7 or E9-EE (See Table 1).

Y bus

The Y bus contains the output of the ALU shifter if \overline{OEY} is low and is a high impedance input if \overline{OEY} is high. SELY must be low to pass the internal ALU shift bus and must be high to pass the external Y bus to the register file.

status

Four status pins are available on the most significant package, overflow (OVR), sign (N), carry out (C_{n+8}), and zero (ZERO). The C_{n+8} line signifies the ALU result while OVR, ZERO, and N refer the status after the ALU shift has occurred. Notice that the ZERO pin cannot be used to detect whether an input placed on a high impedance Y bus is zero.

divide BCD flip-flops

The multiply-divide flip-flops contain the status of the previous multiply or divide instruction. They are affected by the following instructions:

DIVIDE REMAINDER FIX	SIGNED DIVIDE ITERATE
SIGNED DIVIDE QUOTIENT FIX	UNSIGNED DIVIDE START
SIGNED MULTIPLY	UNSIGNED DIVIDE ITERATE
SIGNED MULTIPLY TERMINATE	UNSIGNED MULTIPLY
SIGNED DIVIDE INITIALIZE	SIGNED DIVIDE TERMINATE
SIGNED DIVIDE START	UNSIGNED DIVIDE TERMINATE

The excess-3 BCD flip-flops are affected by all instructions except NOP. The clear function clears these flip-flops. They preserve the carry from each nibble (4-bits) in excess-3/BCD operations.

package position pin (PPP)

The position of the processor in the system is defined by the voltage level applied to the package position pin (PPP). Intermediate positions are selected by leaving the pin open. Tying the pin to V_{CC} makes the processor the most significant package and tying the pin to GND makes the processor the least significant package.

special shift function (SSF) pin

Conditional shifting algorithms may be implemented via control of the SSF pin. The applied voltage to this pin may be set as a function of a potential overflow condition (the two most significant bits are not equal) or any other condition (see Group 1 instructions).

instruction set

The 'AS888 bit-slice processor uses bits 17-10 as instruction inputs. A combination of bits 13-10 (Group 1 instructions) and bits 17-14 (Group 2-5 instructions) are used to develop the 8-bit op code for a specific instruction. Group 1 and Group 2 instructions can be combined to perform arithmetic or logical functions plus a shift function in one instruction cycle. A summary of the instruction set is given in Table 1.

TABLE 1. INSTRUCTION SET

GROUP 1 INSTRUCTIONS

INSTRUCTION BITS (I3-I0) HEX CODE	MNEMONIC	FUNCTION
0		Accesses Group 4 instructions
1	ADD	$R + S + C_n$
2	SUBR	$\bar{R} + S + C_n$
3	SUBS	$R + \bar{S} + C_n$
4	INCS	$S + C_n$
5	INCNS	$\bar{S} + C_n$
6	INCR	$R + C_n$
7	INCNR	$\bar{R} + C_n$
8		Accesses Group 3 instructions
9	XOR	R XOR S
A	AND	R AND S
B	OR	R OR S
C	NAND	R NAND S
D	NOR	R NOR S
E	ANDNR	\bar{R} AND S
F		Accesses Group 5 instructions

GROUP 2 INSTRUCTIONS

INSTRUCTION BITS (I7-I4) HEX CODE	MNEMONIC	FUNCTION
0	SRA	Arithmetic Right Single
1	SRAD	Arithmetic Right Double
2	SRL	Logical Right Single
3	SRLD	Logical Right Double
4	SLA	Arithmetic Left Single
5	SLAD	Arithmetic Left Double
6	SLC	Circular Left Single
7	SLCD	Circular Left Double
8	SRC	Circular Right Single
9	SRCD	Circular Right Double
A	MQSRA	Pass (F→Y) and Arithmetic Right MQ
B	MQSRL	Pass (F→Y) and Logical Right MQ
C	MQSLL	Pass (F→Y) and Logical Left MQ
D	MQSLC	Pass (F→Y) and Circular Left MQ
E	LOADMQ	Pass (F→Y) and Load MQ (F = MQ)
F	PASS	Pass (F→Y)

2

LSI Devices

TABLE 1. INSTRUCTION SET (Continued)

GROUP 3 INSTRUCTIONS		
INSTRUCTION BITS (I7-I0) HEX CODE	MNEMONIC	FUNCTION
08	SET1	Set Bit
18	SET0	Reset Bit
28	TB1	Test Bit (One)
38	TB0	Test Bit (Zero)
48	ABS	Absolute Value
58	SMTC	Sign Magnitude/Two's Complement
68	ADDI	Add Immediate
78	SUBI	Subtract Immediate
88	BADD	Byte Add R to S
98	BSUBS	Byte Subtract S from R
A8	BSUBR	Byte Subtract R from S
B8	BINCS	Byte Increment S
C8	BINCNS	Byte Increment Negative S
D8	BXOR	Byte XOR R and S
E8	BAND	Byte AND R and S
F8	BOR	Byte OR R and S
GROUP 4 INSTRUCTIONS		
INSTRUCTION BITS (I7-I0) HEX CODE	MNEMONIC	FUNCTION
00		Reserved
10	SEL	Select S/R
20	SNORM	Single Length Normalize
30	DNORM	Double Length Normalize
40	DIVRF	Divide Remainder Fix
50	SDIVQF	Signed Divide Quotient Fix
60	SMULI	Signed Multiply Iterate
70	SMULT	Signed Multiply Terminate
80	SDIVIN	Signed Divide Initialize
90	SDIVIS	Signed Divide Start
A0	SDIVI	Signed Divide Iterate
B0	UDIVIS	Unsigned Divide Start
C0	UDIVI	Unsigned Divide Iterate
D0	UMULI	Unsigned Multiply Iterate
E0	SDIVIT	Signed Divide Terminate
F0	UDIVIT	Unsigned Divide Terminate

2

LSI Devices

TABLE 1. INSTRUCTION SET (Concluded)

GROUP 5 INSTRUCTIONS		
INSTRUCTION BITS (I7-I0) HEX CODE	MNEMONIC	FUNCTION
0F	CLR	Clear
1F	CLR	Clear
2F	CLR	Clear
3F	CLR	Clear
4F	CLR	Clear
5F	CLR	Clear
6F	CLR	Clear
7F	BCDBIN	BCD to Binary
8F	EX3BC	Excess-3 Byte Correction
9F	EX3C	Excess-3 Word Correction
AF	SDIVO	Signed Divide Overflow Check
BF	CLR	Clear
CF	CLR	Clear
DF	BINEX3	Binary to Excess-3
EF	CLR	Clear
FF	NOP	No Operation

2

LSI Devices

group 1 instructions

TABLE 2. GROUP 1 INSTRUCTIONS

INSTRUCTION BITS (I3-I0) HEX CODE	MNEMONIC	FUNCTION
0		Accesses Group 4 instructions
1	ADD	$R + S + C_n$
2	SUBR	$\bar{R} + S + C_n$
3	SUBS	$R + \bar{S} + C_n$
4	INCS	$S + C_n$
5	INCNS	$\bar{S} + C_n$
6	INCR	$R + C_n$
7	INCNR	$\bar{R} + C_n$
8		Accesses Group 3 instructions
9	XOR	R XOR S
A	AND	R AND S
B	OR	R OR S
C	NAND	R NAND S
D	NOR	R NOR S
E	ANDNR	\bar{R} AND S
F		Accesses Group 5 instructions

Group 1 instructions (excluding hex codes 0, 8, and F), shown in Table 2, may be used in conjunction with Group 2 shift instructions to perform arithmetic or logical functions plus a shift function[†] in one instruction cycle (hex codes 0, 8, and F are used to access Group 4, 3, and 5 instructions, respectively). Each shift may be made into a conditional shift by forcing the special shift function (SSF) pin into the proper state. If the SSF pin is high or floating, the shifted ALU output will be sent to the output buffers. If the SSF pin is pulled low externally, the ALU result will be passed directly to the output buffers. Conditional shifting is useful for scaling inputs in data arrays or in signal processing algorithms.

These instructions set the BCD flip-flop for the excess-3 correct instruction. The status is set with the following results (C_{n+8} is ALU carry out and is independent of shift operation; others are evaluated after shift operation).

[†]Double-precision shifts involve both the ALU and MQ register.

condition code

Arithmetic

- N — MSB of result
- OVR — Signed arithmetic overflow
- C_{n+8} — Carry out equal one
- Z — Result equal zero

Logic

- N — MSB of result
- OVR — None (force to zero)
- C_{n+8} — None (force to zero)
- Z — Result equal zero



group 2 instructions

TABLE 3. GROUP 2 INSTRUCTIONS

INSTRUCTION BITS (I7-I4) HEX CODE	MNEMONIC	FUNCTION
0	SRA	Arithmetic Right Single
1	SRAD	Arithmetic Right Double
2	SRL	Logical Right Single
3	SRLD	Logical Right Double
4	SLA	Arithmetic Left Single
5	SLAD	Arithmetic Left Double
6	SLC	Circular Left Single
7	SLCD	Circular Left Double
8	SRC	Circular Right Single
9	SRCD	Circular Right Double
A	MQSRA	Pass (F→Y) and Arithmetic Right MQ
B	MQSRL	Pass (F→Y) and Logical Right MQ
C	MQSLL	Pass (F→Y) and Logical Left MQ
D	MQSLC	Pass (F→Y) and Circular Left MQ
E	LOADMQ	Pass (F→Y) and Load MQ (F = MQ)
F	PASS	Pass (F→Y)

SN54AS888, SN74AS888 8-BIT PROCESSOR SLICES

The processor's shift instructions are implemented by a combination of Group 2 instructions (Table 3) and certain wired connections on the packages used. The following external connections are required.

On intermediate packages:

$\overline{SIO7}$ is connected to $\overline{SIO0}$ of the next most significant package

$\overline{QIO7}$ is connected to $\overline{QIO0}$ of the next most significant package

$\overline{SIO0}$ is connected to $\overline{SIO7}$ of the next least significant package

$\overline{QIO0}$ is connected to $\overline{QIO7}$ of the next least significant package

On the two end packages:

$\overline{SIO7}$ on the most significant package is connected to $\overline{SIO0}$ of the least significant package

$\overline{QIO7}$ on the most significant package is connected to $\overline{QIO0}$ of the least significant package

The connections are the same on all instructions including multiply, divide, CRC, and normalization functions.

Single- and double-precision shifts are supported. Double-precision shifts assume the most significant half has come through the ALU and will be placed (if \overline{WE} is low) into the register file on the rising edge of the clock and the least significant half lies in the MQ register. All Group 2 shifts may be made conditional (see previous page).

The following definitions apply to Group 2 shift instructions:

Arithmetic right shifts copy the sign of the number if no overflow occurs from the ALU calculation; if overflow occurs, the sign bit is inverted.

Arithmetic left shifts do not retain the sign of the number if an overflow occurs. A zero is filled into the LSB if not forced externally.

Logical right shifts fill a zero in the MSB position if not forced externally.

Circular right shifts fill the LSB in the MSB position.

Circular left shifts fill the MSB in the LSB position.

Shifting left is defined as moving a bit position towards the MSB (doubling).

Shifting right is defined as moving a bit towards the LSB (halving).

Serial input may be performed using the circuitry shown in Figure 1. A single-/or double-precision arithmetic left or logical right shift fills the complement of the data on $\overline{SIO0}$ and $\overline{SIO7}$ into the LSB or MSB of the data word(s). Note that if $\overline{SIO0}$ and $\overline{SIO7}$ are floating (HI-Z), a zero will be filled as an end condition.

Serial output may be performed with circular instructions.



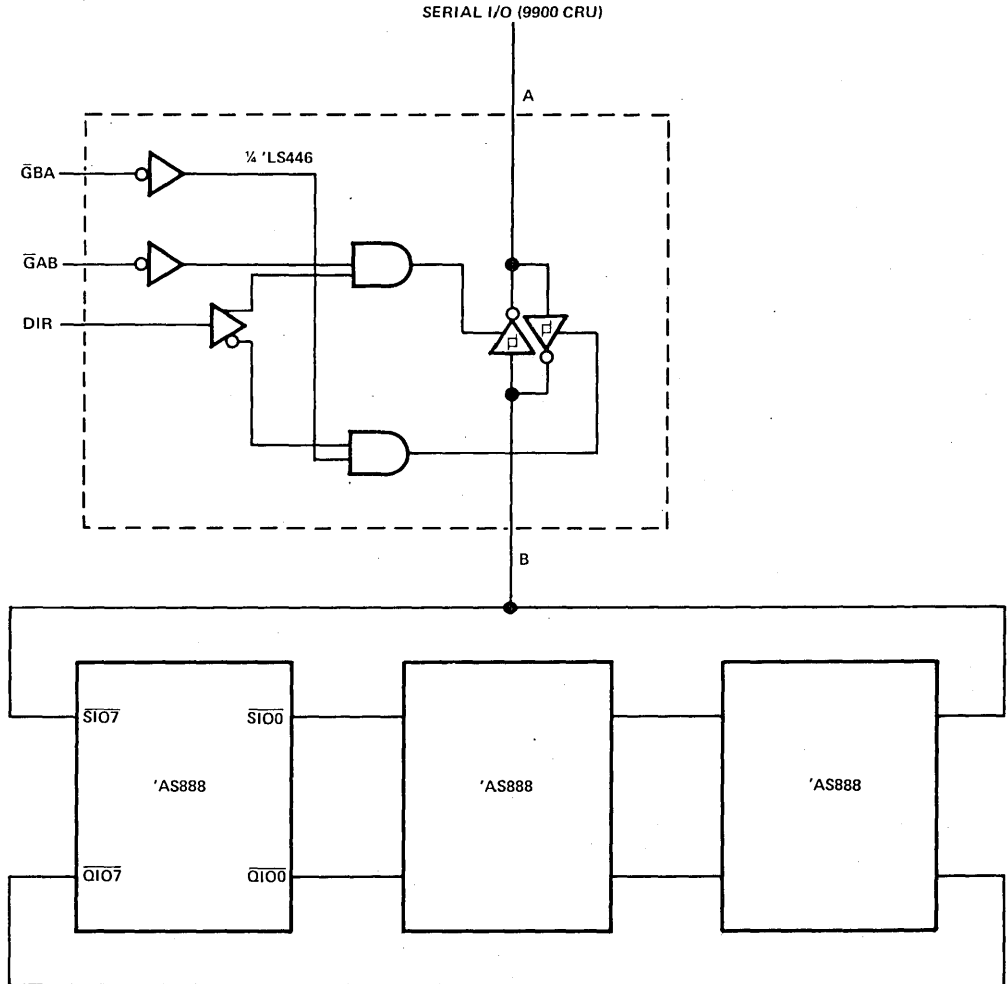


FIGURE 1. SERIAL I/O

The shift instructions are summarized in Table 4 and illustrated in Figure 2. In Figure 2 and all succeeding figures that illustrate instruction execution, the following definitions apply:

- CRF — CRC accumulator end fill.
- QBT — End fill for signed divide.
- MQF — End fill for unsigned divide.
- SRF — End fill for signed multiply and the arithmetic right shifts.

TABLE 4. SHIFT INSTRUCTIONS

OP CODE†	SHIFT FUNCTION‡	S107 · S100 WIRED VALUE	Q107 · Q100 WIRED VALUE
0N	Arithmetic Right Single	ALU-LSB Output	—
1N	Arithmetic Right Double	MQ-LSB Output	ALU-LSB Output
2N	Logical Right Single	Input to ALU-MSB	ALU-LSB Output
3N	Logical Right Double	Input to ALU-MSB	ALU-LSB Output
4N	Arithmetic Left Single	Input to ALU-LSB	ALU-MSB Output
5N	Arithmetic Left Double	Input to MQ-LSB	MQ-MSB Output
6N	Circular Left Single	ALU-MSB Output	—
7N	Circular Left Double	ALU-MSB Output	MQ-MSB Output
8N	Circular Right Single	ALU-LSB Output	—
9N	Circular Right Double	MQ-LSB Output	ALU-LSB Output
AN	Arithmetic Right (MQ only)	MQ-LSB Output	MQ-MSB Output
BN	Logical Right (MQ only)	MQ-LSB Output	Input to MQ-MSB
CN	Logical Left (MQ only)	Input to MQ-LSB	MQ-MSB Output
DN	Circular Left (MQ only)	MQ-MSB Output	MQ-MSB Output

†Op Code N ≠ 0, 8, or F; these select special instruction Groups 4, 3, and 5 respectively.

‡Shift I/O pins are active low. Therefore, inputs and outputs must be inverted if true logical values are required.

Status is set with the following results:

Arithmetic

- N → Result MSB equal one
- OVR → Signed arithmetic overflow†
- C_{n+8} → Carry out equal one
- Z → Result equal zero

Logic

- N → Result MSB equal one
- OVR → Zero
- C_{n+8} → Zero
- Z → Result equal zero

† For the SLA and SLAD instructions, OVR is set if signed arithmetic overflow or if the ALU result MSB XOR MSB-1 equals one.

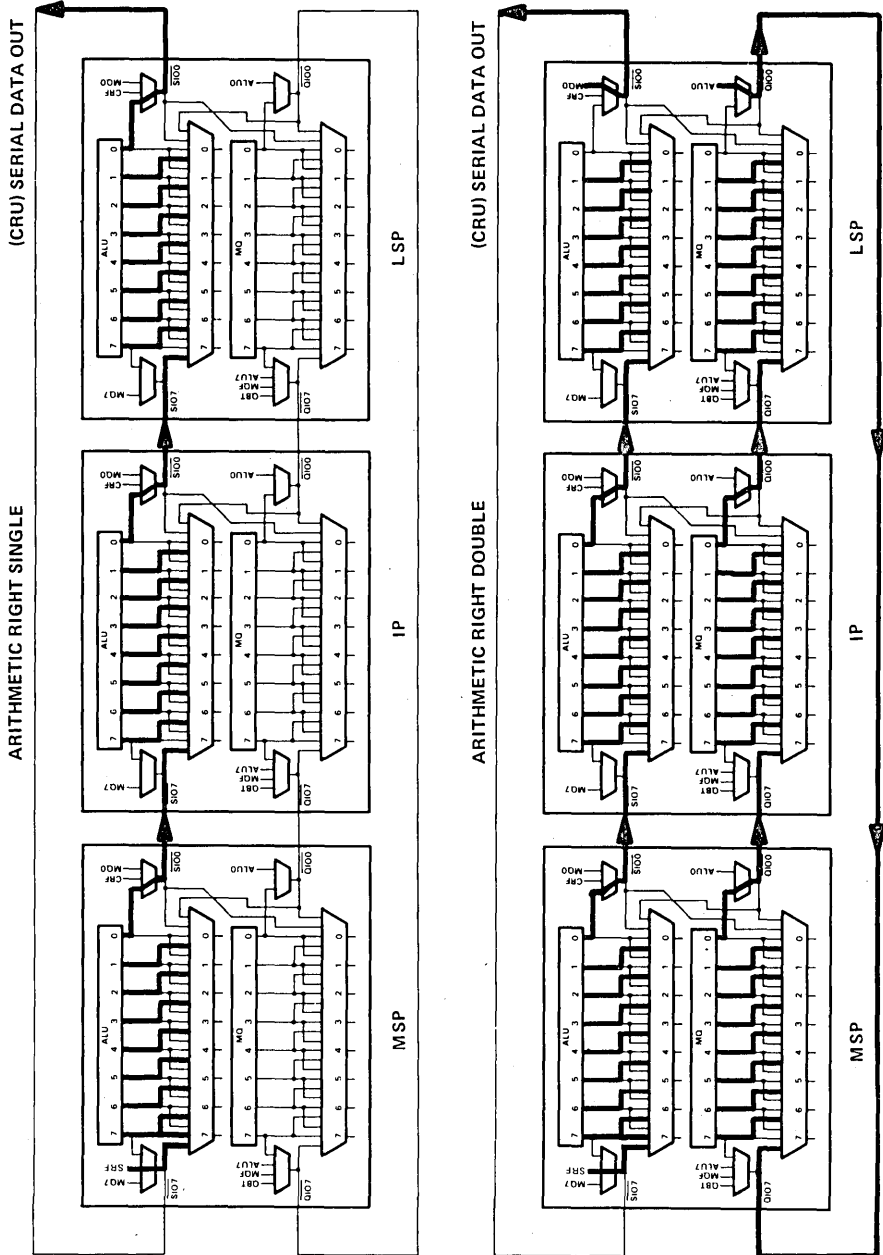


FIGURE 2. SHIFT INSTRUCTIONS

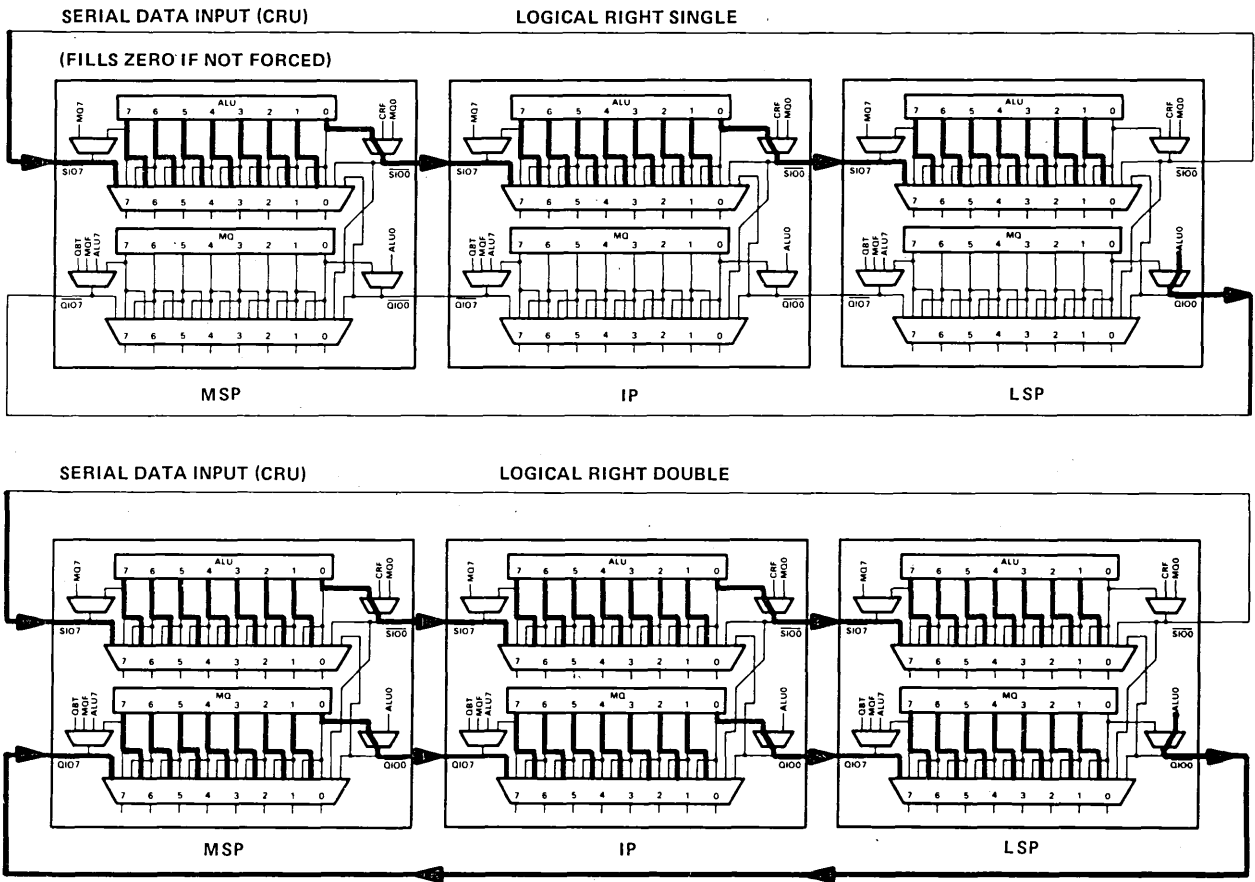


FIGURE 2. SHIFT INSTRUCTIONS (Continued)

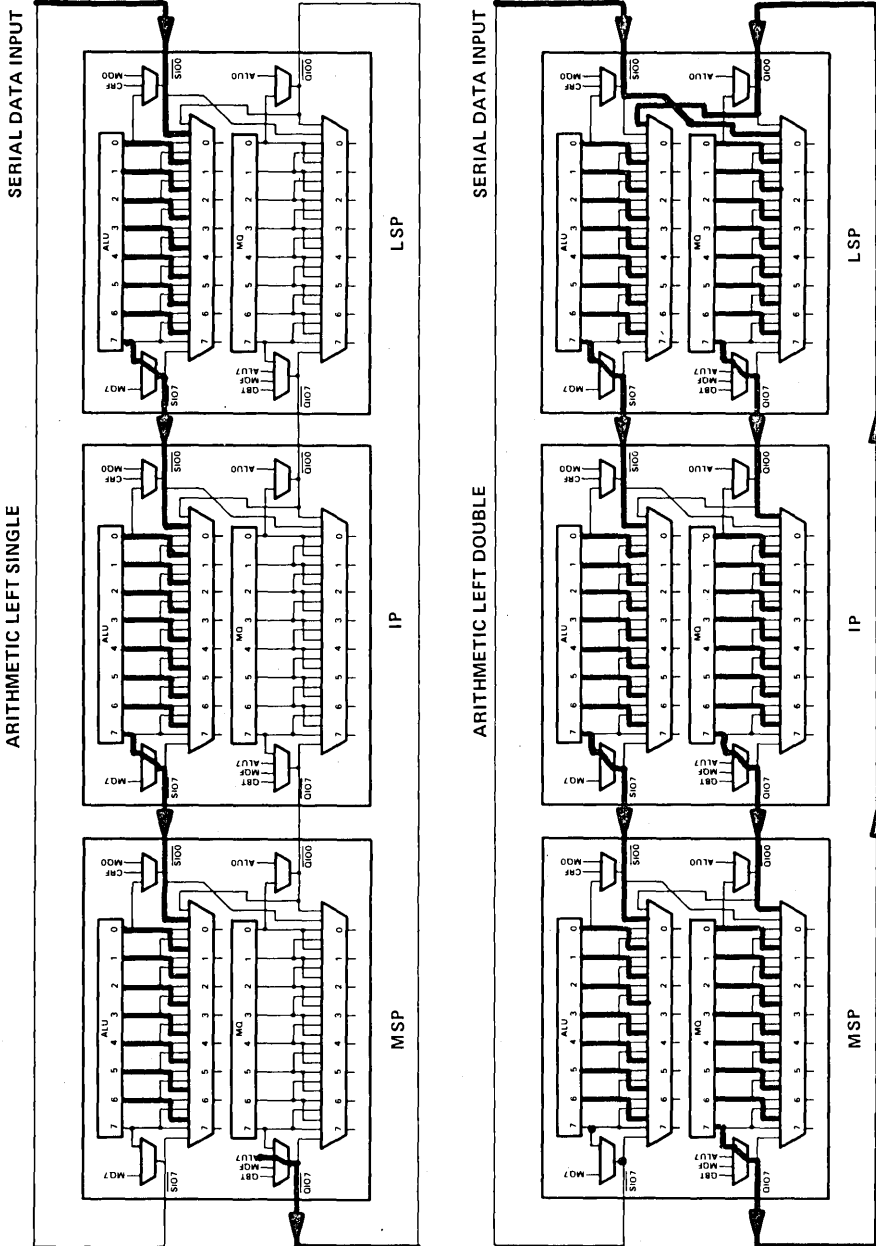


FIGURE 2. SHIFT INSTRUCTIONS (Continued)

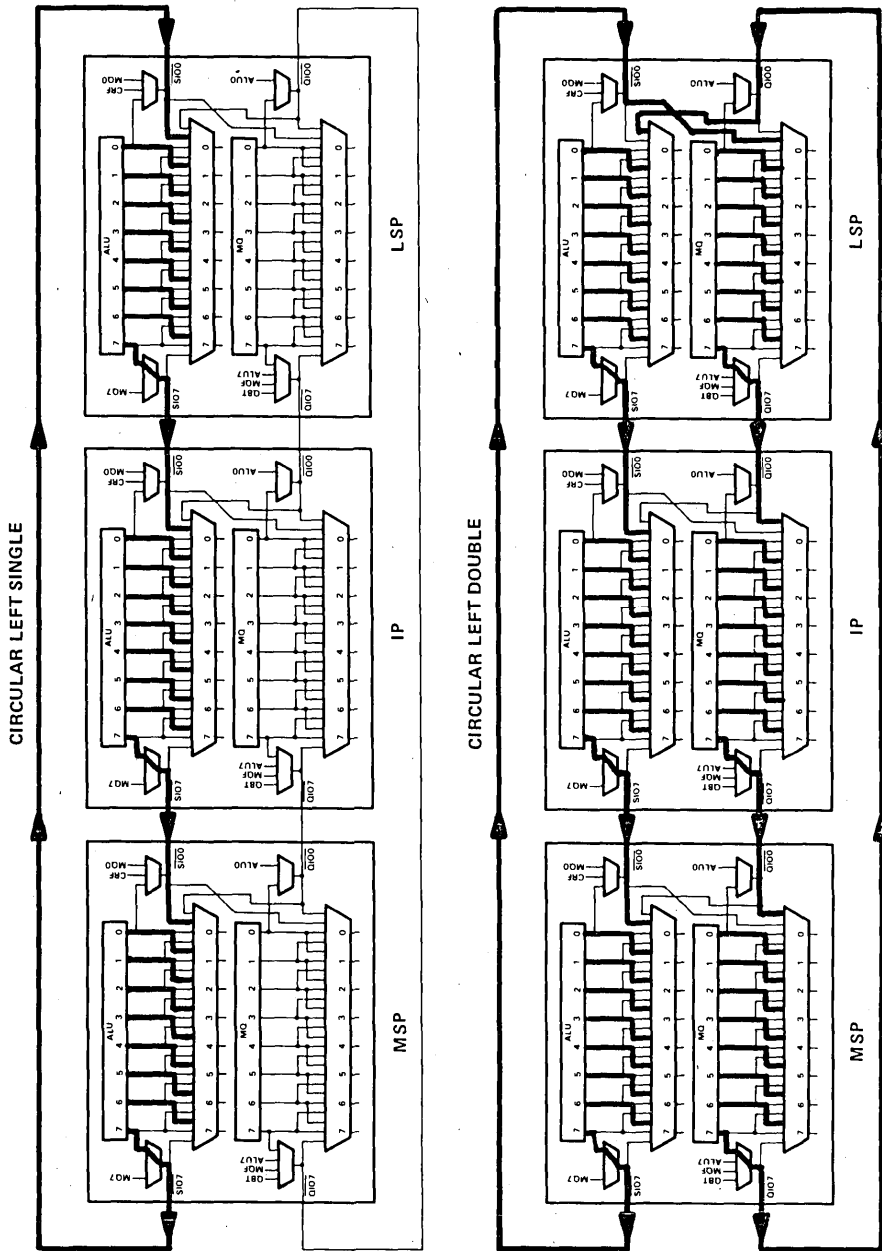


FIGURE 2. SHIFT INSTRUCTIONS (Continued)

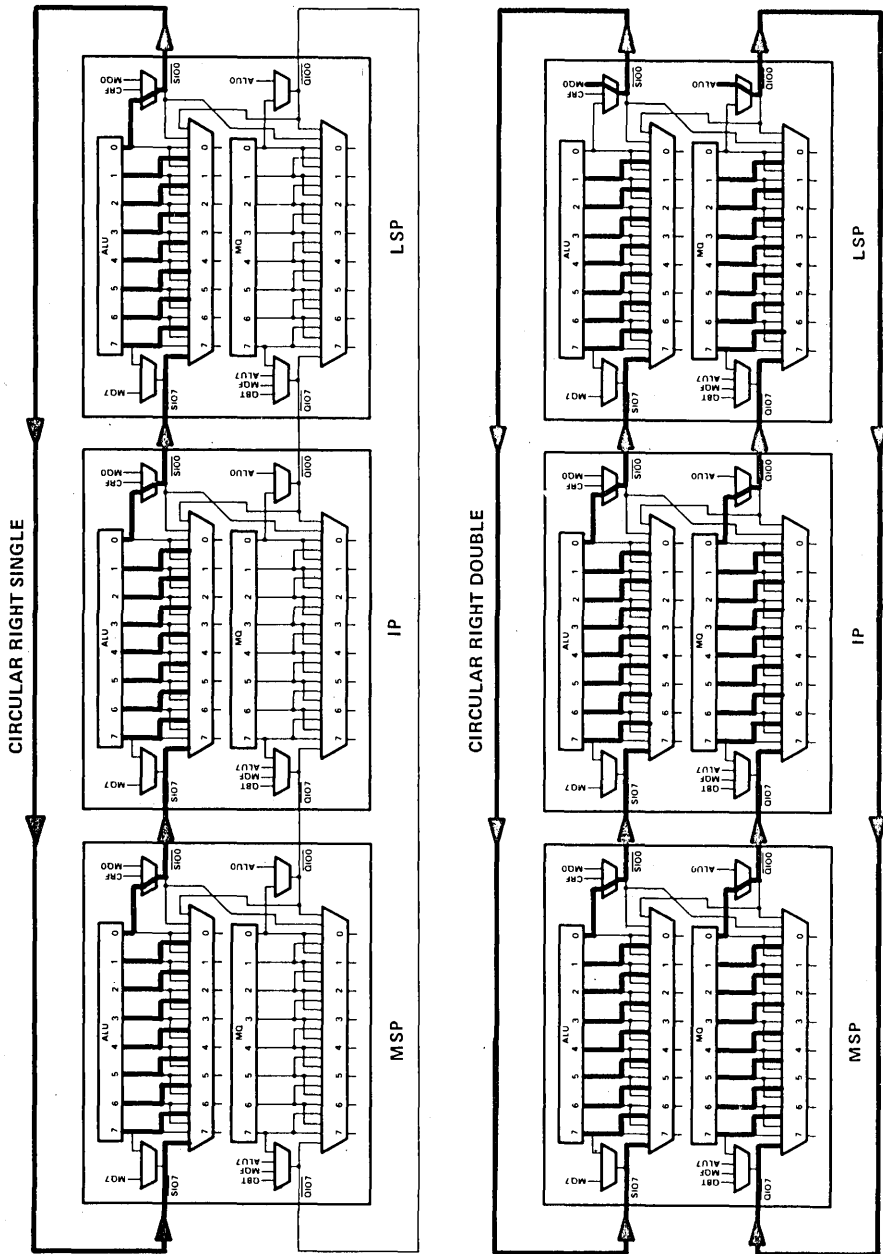


FIGURE 2. SHIFT INSTRUCTIONS (Continued)

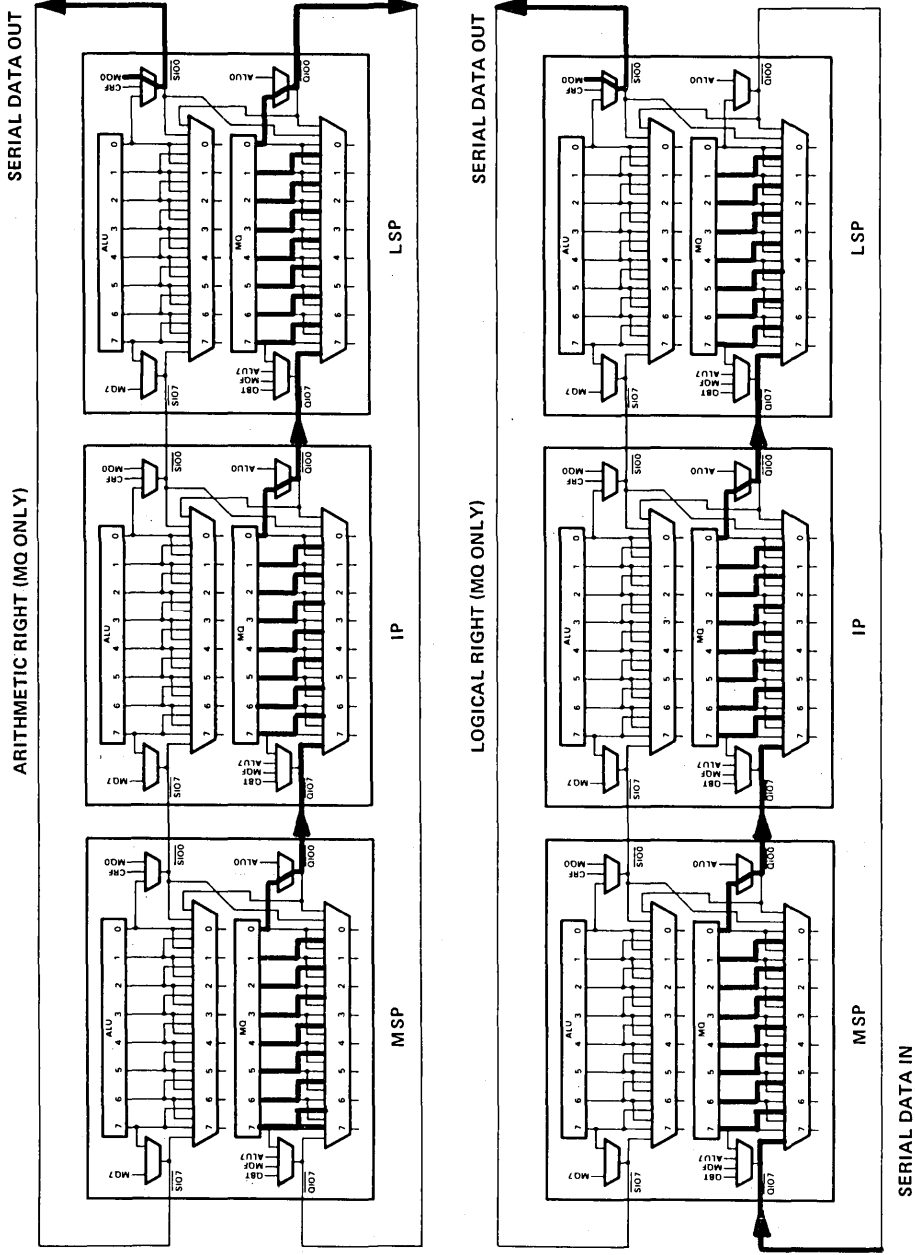


FIGURE 2. SHIFT INSTRUCTIONS (Continued)

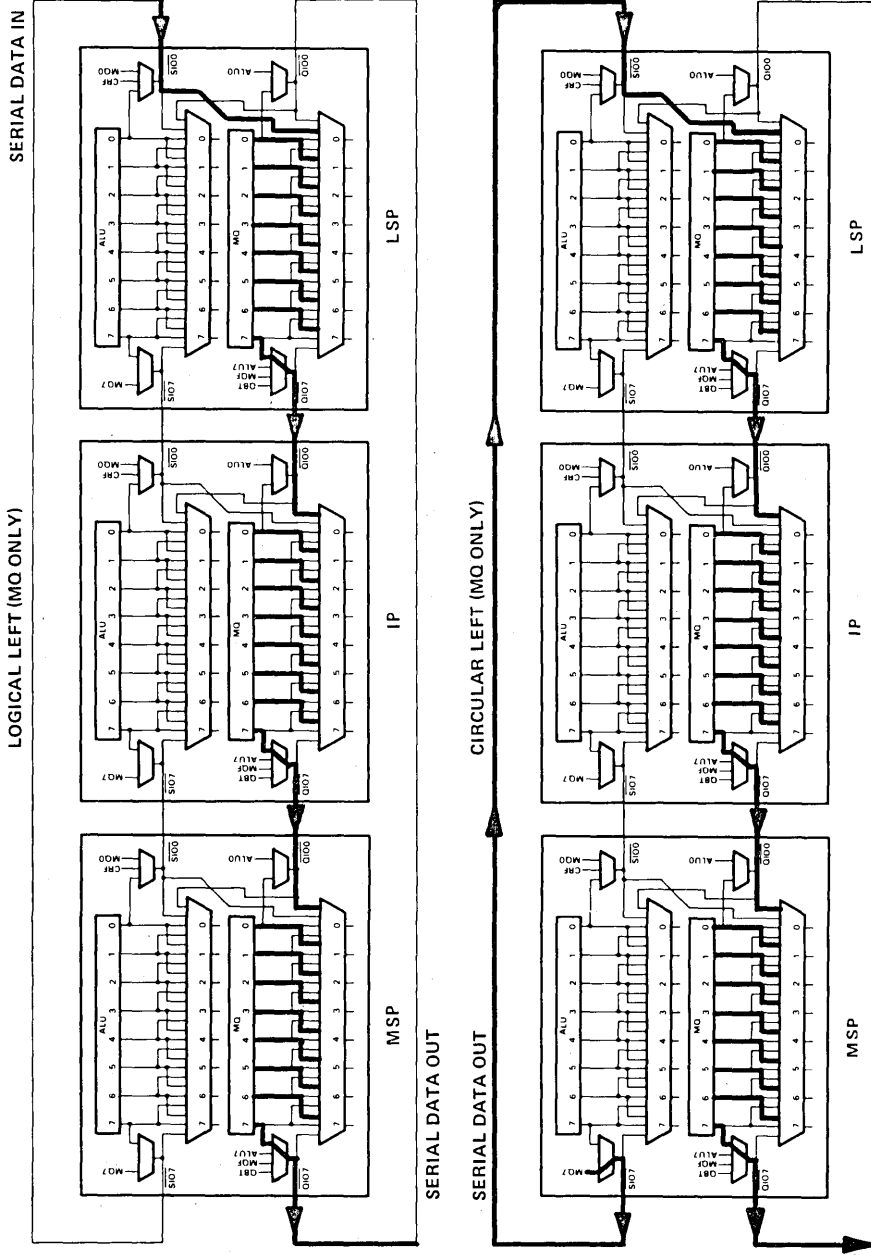


FIGURE 2. SHIFT INSTRUCTIONS (Concluded)



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SN54AS888, SN74AS888 8-BIT PROCESSOR SLICES

group 3 instructions

Hex code 8 of Group 1 instructions is used to access Group 3 instructions. Group 3 instructions are summarized in Table 5.

TABLE 5. GROUP 3 INSTRUCTIONS

INSTRUCTION BITS (I7-I0) OP CODE (HEX)	MNEMONIC	FUNCTION
08	SET1	Set Bit
18	SET0	Reset Bit
28	TB1	Test Bit (One)
38	TB0	Test Bit (Zero)
48	ABS	Absolute Value
58	SMTC	Sign Magnitude/Two's Complement
68	ADDI	Add Immediate
78	SUBI	Subtract Immediate
88	BADD	Byte Add R to S
98	BSUBS	Byte Subtract S from R
A8	BSUBR	Byte Subtract R from S
B8	BINCS	Byte Increment S
C8	BINCNS	Byte Increment Negative S
D8	BXOR	Byte XOR R and S
E8	BAND	Byte AND R and S
F8	BOR	Byte OR R and S

set bit instruction (set1): I7-I0 = 0816

This instruction (Figure 3) is used to force selected bits of a desired byte(s) to one (any combination of zero to eight bits). The desired bits are specified by an 8-bit mask (C3-C0):(A3-A0)[†] consisting of register file address ports that are not required to support this instruction. All bits in the selected byte(s) that are in the same bit positions as ones in the mask are forced to a logical one. The B3-B0 address field is used for both source and destination of this instruction. The desired byte is specified by forcing $\overline{S100}$ to a low value. Nonselected packages pass the byte through unaltered. The S bus is the source word for this instruction. The status set by the set bit instruction is as follows:

- N → None (force to zero)
- OVR → None (force to zero)
- C_n+8 → None (force to zero)
- Z → Result equal zero

[†] The symbol "::" is concatenation operator

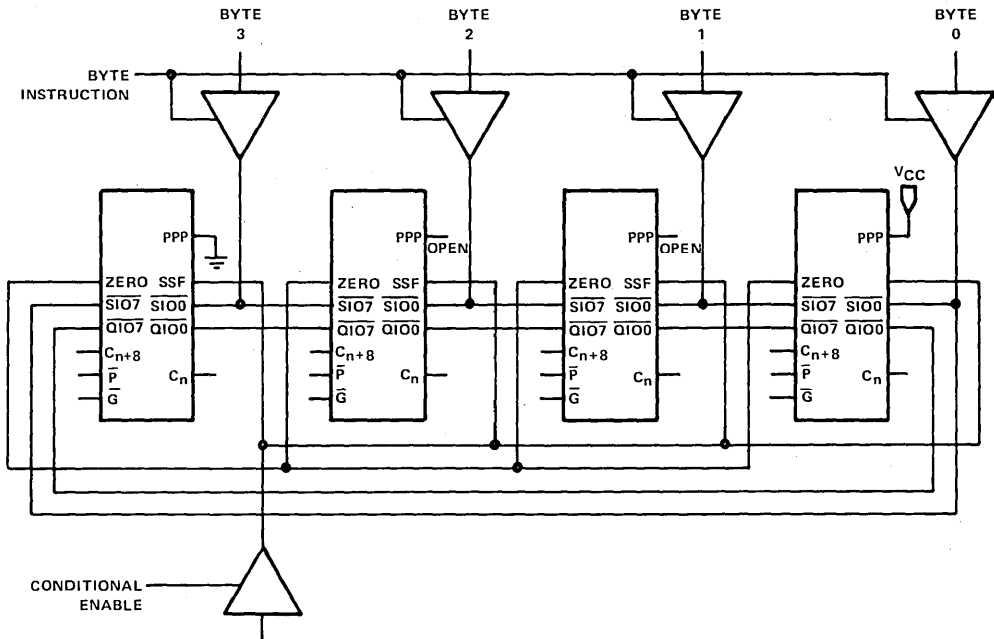


FIGURE 3. SET BIT (OR RESET BIT)

- NOTES: 1. Force $\overline{S100}$ low to select byte.
2. Bit mask (C3-C0):(A3-A0) will set desired bits to one.

reset bit instruction (set0): I7-I0 = 1816

This instruction (Figure 3) is used to force selected bits of a desired byte(s) to zero (any combination of one to eight bits). The desired bits are specified by an 8-bit mask (C3-C0):(A3-A0) consisting of register file address ports that are not required to support this instruction. All bits in the selected byte(s) that are in the same bit positions as ones in the mask are reset. The B3-B0 address field is used for both source

2
LSI Devices

SN54AS888, SN74AS888

8-BIT PROCESSOR SLICES

and destination of this instruction. The desired byte is specified by forcing $\overline{SIO0}$ to a low value. Nonselected packages pass the byte through unaltered. The S bus is the source word for this instruction. The status set by the reset bit instruction is as follows:

- N → None (force to zero)
- OVR → None (force to zero)
- C_{n+8} → None (force to zero)
- Z → Result equal zero

test bit (one) instruction (TB1): 17-10 = 2816

This instruction (Figure 4) is used to test selected bits of a desired byte(s) (any combination of one to eight bits). Bits to be tested are specified by an 8-bit mask (C3-C0)::(A3-A0) consisting of register file address ports that are not required to support this instruction. Write Enable (\overline{WE}) is internally disabled during this instruction. The desired byte is specified by forcing $\overline{SIO0}$ to a low value. The test will pass if the selected byte has ones at all bit locations specified by the ones of the mask (Figure 5). The S bus is the source word for this instruction. The status set by the test bit (one) instruction is as follows:

- N → None (force to zero)
- OVR → None (force to zero)
- C_{n+8} → None (force to zero)
- Z → Pass

2
LSI Devices

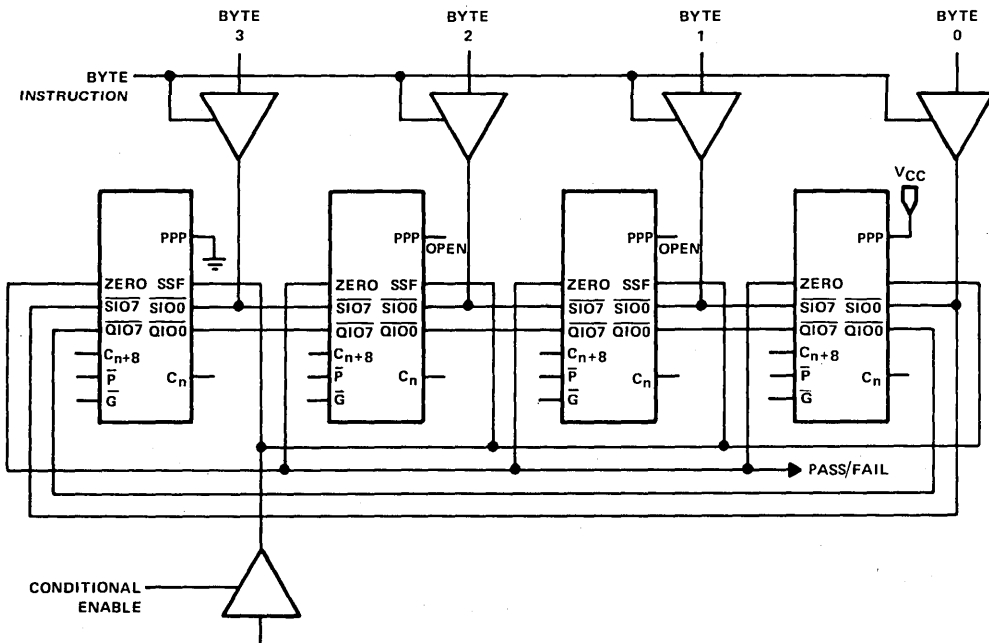


FIGURE 4. TEST BIT

- NOTES: 1. Force $\overline{SIO0}$ low to select byte.
 2. Bit mask (C3-C0)::(A3-A0) will define bits for testing.
 3. Pass/fail is indicated on Z output.

test bit (zero) instruction (TBO): I7-I0 = 3816

This instruction (Figure 4) is used to test selected bits of a desired byte(s) (any combination of one to eight bits). Bits to be tested are specified by an 8-bit mask (C3-C0):(A3-A0) consisting of register file address ports that are not required to support this instruction. Write Enable (\overline{WE}) is internally disabled during this instruction. The desired byte is specified by forcing $\overline{SIO0}$ to a low value. The test will pass if the selected byte has zeros at all bit locations specified by the ones of the mask (Figure 6). The S bus is the source word for this instruction. The status set by the test bit (zero) instruction is as follows:

- N → None (force to zero)
- OVR → None (force to zero)
- C_{n+8} → None (force to zero)
- Z → Pass

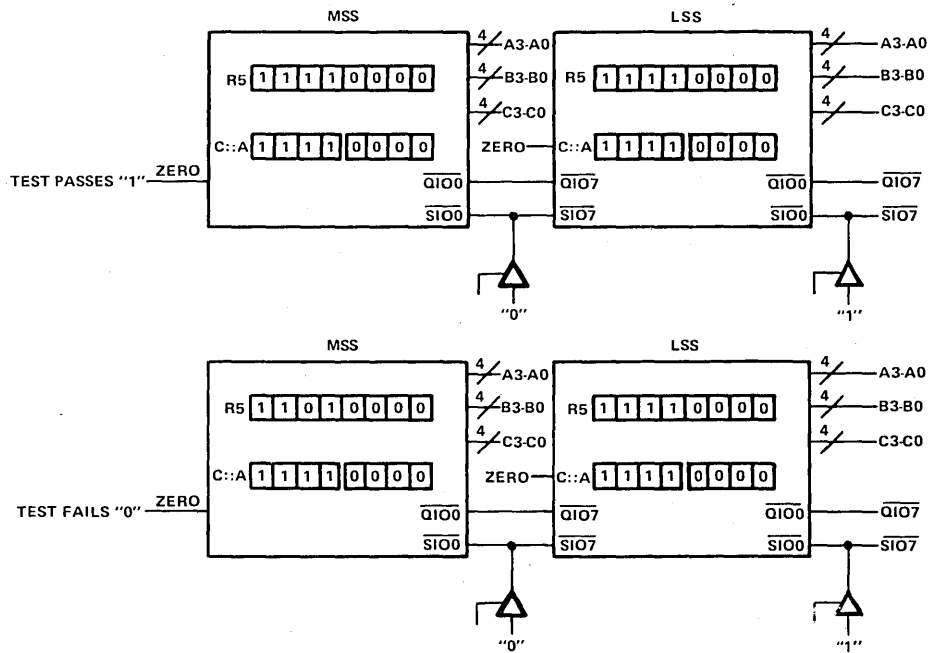


FIGURE 5. TEST BIT ONE EXAMPLES

SN54AS888, SN74AS888
8-BIT PROCESSOR SLICES

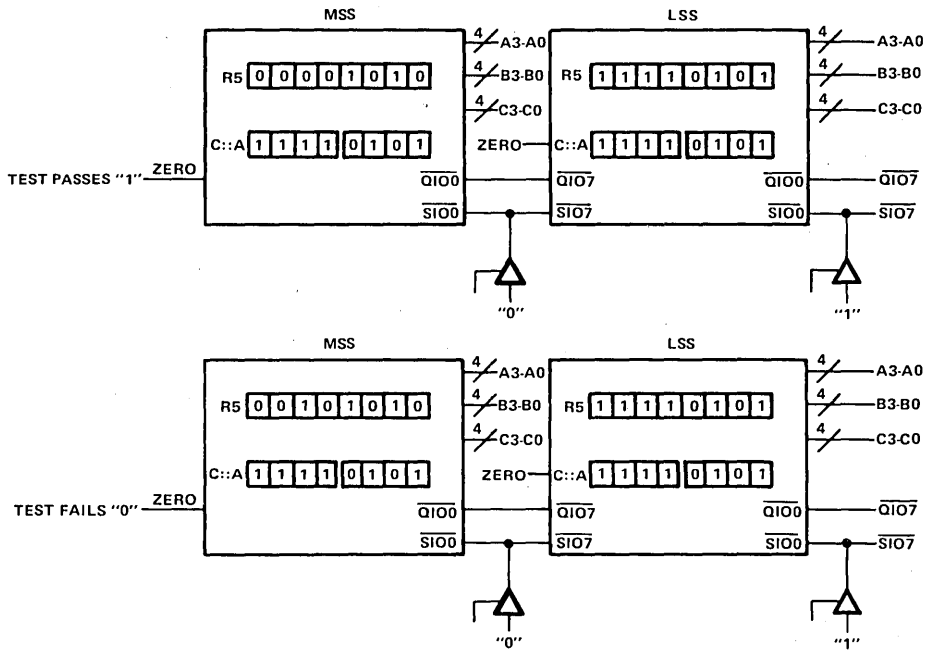


FIGURE 6. TEST BIT ZERO EXAMPLES

absolute value instruction (ABS): 17-10 = 4816

This instruction is used to convert two's complement numbers to their positive value. The operand placed on the S bus is the source for this instruction. The MSP will test the sign of the S bus and force the SSF pin to the proper value. All other packages use the SSF pin as input to determine instruction execution. The status set by the absolute value instruction is as follows:

- N → Input MSB equal one
- OVR → Input equal 8000 (hex)
- C_{n+8} → S = 0
- Z → Result equal zero

sign magnitude/two's complement instruction (SMTc): 17-10 = 5816

This instruction allows conversion from two's complement representation to sign magnitude representation, or vice-versa, in one clock cycle. The operand placed on the S bus is the source for this instruction.

When a negative zero (8000 hex) is converted, the result is 0000 with an overflow. If the input is in two's complement notation, the overflow indicates an illegal conversion. The status set by the sign magnitude/two's complement instruction is as follows:

- N → Result MSB equal one
- OVR → Input equal 8000 (hex)
- C_{n+8} → Input equal 0000 (hex)
- Z → Result equal zero

add immediate instruction (ADDI): 17-10 = 6816

This instruction is used to add a specified constant value to the operand placed on the S bus. The constant will be between the values of 0 and 15. The constant value is specified by the unused register file address (A port) not required to support this instruction. Forcing the carry input will add an additional one to the result. The status set by the add immediate instruction is as follows:

- N → Result MSB equal one
- OVR → Arithmetic signed overflow
- C_{n+8} → Carry out equal one
- Z → Result equal zero

subtract immediate instruction (SUBI): 17-10 = 7816

This instruction is used to subtract a specified constant value from the operand placed on the S bus. The constant value is specified by the unused register file address (A port) that is not required to support this instruction. The constant applied is the least significant four bits of a two's complement number. The device sign extends the constant over the entire word length. The status set by the subtract immediate instruction is as follows:

- N → Result MSB equal one
- OVR → Arithmetic signed overflow
- C_{n+8} → Carry out equal one
- Z → Result equal zero

byte instructions

There are eight byte instructions in Group 3. These instructions modify selected bytes of the operand on the S bus. A byte is selected by forcing \overline{SIOO} to a low value (same as SET1, SET0, TB1, and TBO instructions). Multiple bytes may be selected only if they are adjacent to one another.

NOTE: At least one byte must be nonselected during these instructions.

The nonselected bytes are passed through unaltered. Byte status is forced through the most significant package except for the sign of the result (N), which is forced to zero (low). The status set by the byte instructions is as follows:

(Most Significant Package)

- N → None (force to zero)
- OVR → Byte signed overflow
- C_{n+8} → Byte carry out equal one
- Z → Byte result equal to zero

(Selected BYTES—other than MSP)

- \overline{G} → Normal generate
- \overline{P} → Normal propagate
- C_{n+8} → Normal carry out
- Z → Result equal to zero

(Nonselected BYTES—other than MSP)

- \overline{G} → No generate (force to one)
- \overline{P} → Propagate (force to zero)
- C_{n+8} → C_n
- Z → None (force to one)

SN54AS888, SN74AS888
8-BIT PROCESSOR SLICES

group 4 instructions

Hex code 0 of Group 1 instructions is used to access Group 4 instructions. Group 4 instructions are summarized in Table 6.

TABLE 6. GROUP 4 INSTRUCTIONS

INSTRUCTION BITS (I7-I0) OP CODE (HEX)	MNEMONIC	FUNCTION
00		Reserved
10	SEL	Select S/R
20	SNORM	Single Length Normalize
30	DNORM	Double Length Normalize
40	DIVRF	Divide Remainder Fix
50	SDIVQF	Signed Divide Quotient Fix
60	SMULI	Signed Multiply Iterate
70	SMULT	Signed Multiply Terminate
80	SDIVIN	Signed Divide Initialize
90	SDIVIS	Signed Divide Start
A0	SDIVI	Signed Divide Iterate
B0	UDIVIS	Unsigned Divide Start
C0	UDIVI	Unsigned Divide Iterate
D0	UMULI	Unsigned Multiply Iterate
E0	SDIVIT	Signed Divide Terminate
F0	UDIVIT	Unsigned Divide Terminate

select S/R instruction (SEL): I7-I0 = 10₁₆

This instruction is used to pass either the S bus or the R bus to the output depending on the state of the SSF input pin. Normally, the preceding instruction would test the two operands and the resulting status information would be used to force the SSF input pin. SSF = 0 will output the R bus and SSF = 1 will output the S bus. The status set by the select S/R instruction is as follows:

- N → Result MSB equal one
- OVR → None (force to zero)
- C_n+8 → None (force to zero)
- Z → Result equal zero

single-length normalize instruction (SNORM): I7-I0 = 20₁₆

This instruction will cause the contents of the MQ register to shift toward the most significant bit. Zeros are shifted in via the $\overline{Q100}$ input. The number of shifts performed can be counted and stored in one of the register files by forcing a high at the C_n input. When the two most significant bits are of opposite value, normalization is complete. This condition is indicated on the microcycle that completes the normalization at the OVR output.

The chip contains conditional logic that inhibits the shift function (and also inhibits the register file increment) if the number within the MQ register is already normalized at the beginning of the instruction (Figure 7). The status set by the single-length normalize instruction is as follows:

- N → MSB of result
- OVR → MSB XOR 2nd MSB
- C_n+8 → Carry out equal one
- Z → Result equal zero

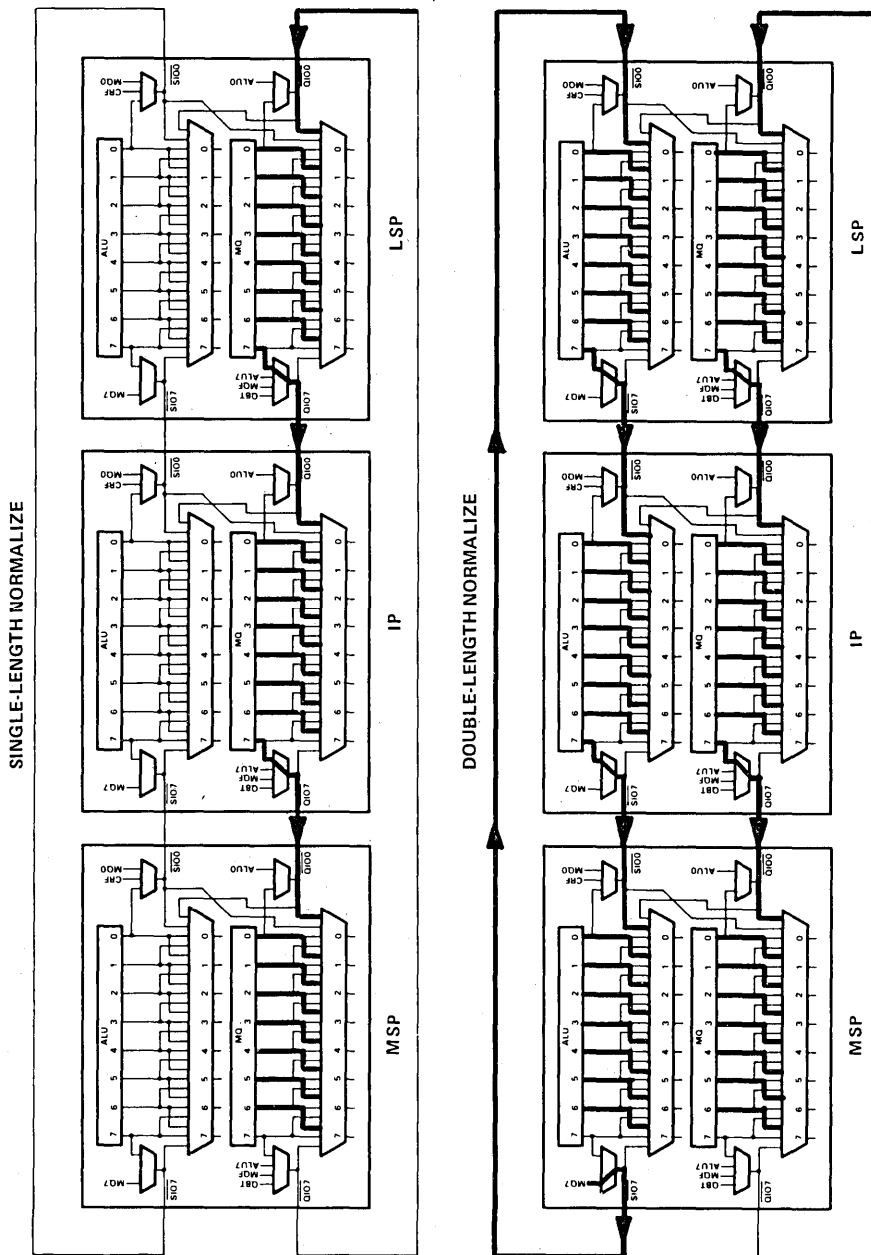


FIGURE 7. SINGLE- AND DOUBLE-LENGTH NORMALIZE

SN54AS888, SN74AS888

8-BIT PROCESSOR SLICES

double-length normalize instruction (DNORM): $17-10 = 30_{16}$

This instruction will cause the contents of a double-length word (register file contains the most significant half and the MQ register contains the least significant half) to shift toward the most significant bit. Zeros are shifted in via the $\overline{Q100}$ input. When the two most significant bits are of opposite value, normalization is complete. This condition is indicated on the microcycle that completes the normalization at the OVR output.

The chip contains conditional logic which inhibits the shift function if the number is already normalized at the beginning of the instruction (Figure 7). The most significant half of the operand must be placed on the S bus. The status set by the double-length normalize instruction is as follows:

N	→	MSB of result
OVR	→	MSB XOR 2nd MSB
C_{n+8}	→	None (force to zero)
Z	→	Result equal zero

multiply operations

The ALU performs three unique types of N by N multiplies each of which produces a 2N-bit result (Figure 8). All three types of multiplication proceed via the following recursion:

$$P(J+1) = 2[P(J) + \text{Multiplicand} \times M (8N-J)]$$

where

$$P(J) = \text{partial product at iteration number } J$$

$$N = \text{number of 'AS888 packages that are cascaded}$$

$$P(J+1) = \text{partial product at iteration number } J+1$$

J varies from 0 to 8N [N = 2 for 16×16 multiply]

$$M (8N-J) = \text{mode bit (unique to multiply type)}$$

2 denotes some type of shift (unique to multiply)

Notice that by proper choice of mode terms and shifting operations, signed, unsigned, and mixed multiplies (signed times unsigned) may be performed.

All multiplies assume that the multiplier is stored in MQ before the operation begins (in the case of mixed multiply, the unsigned number must be the multiplier).

The processor has the following multiply instructions:

1. SIGNED MULTIPLY ITERATE (SMULI): $17-10 = 60_{16}$
2. SIGNED MULTIPLY TERMINATE (SMULT): $17-10 = 70_{16}$
3. UNSIGNED MULTIPLY ITERATE (UMULI): $17-10 = D0_{16}$

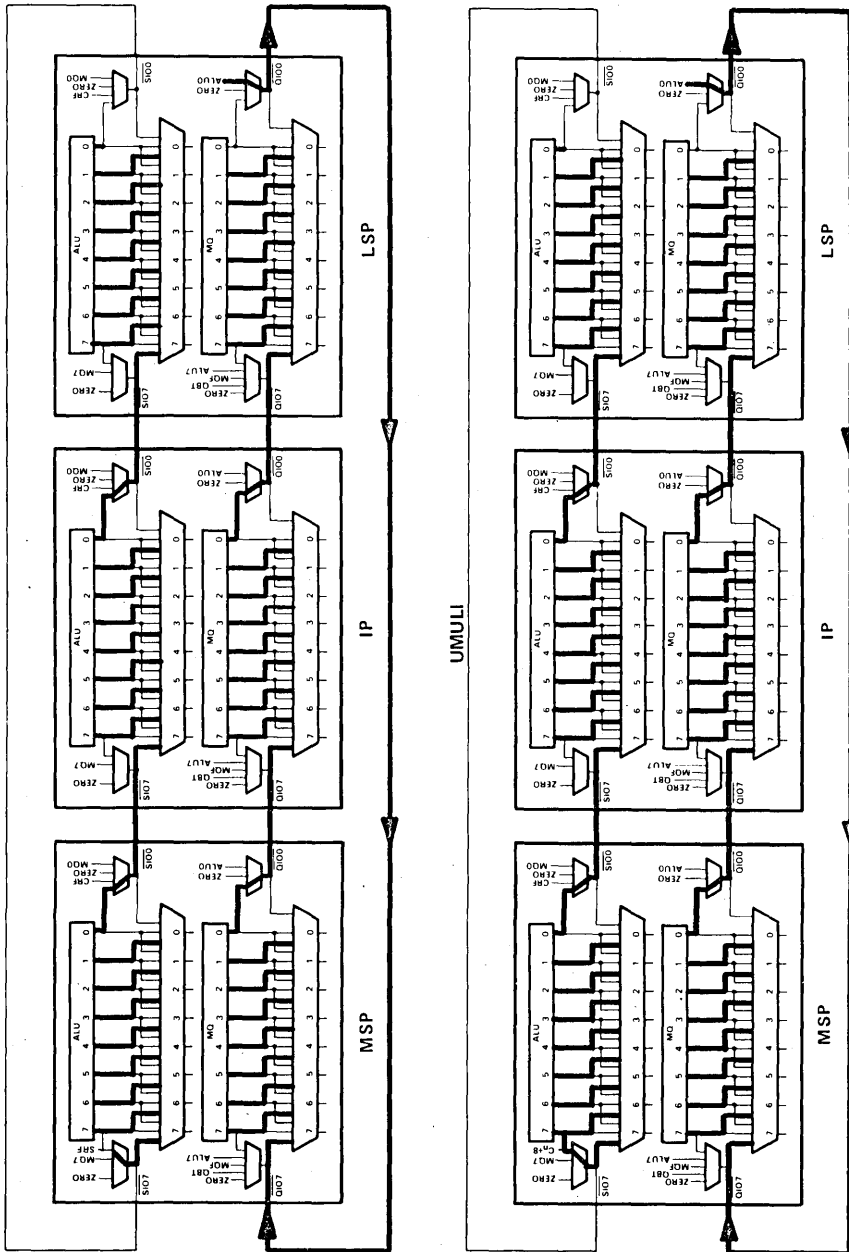


FIGURE 8. MULTIPLICATION OPERATIONS

SN54AS888, SN74AS888 8-BIT PROCESSOR SLICES

The signed multiply iterate (SMULI) instruction performs a signed times signed iteration. This instruction interprets M(8N-J) as the 8N-J bit of the multiplier. The shift is a double-precision right shift one bit. This instruction is repeated 15 times for a 16×16 signed multiply. This instruction will be used 16 consecutive times for a mixed multiplication.

The signed multiply terminate (SMULT) instruction provides correct (negative) weighting of the sign bit of a negative multiplier in signed multiplication. The instruction is identical to signed multiply iterate (SMULI) except that M(8N-J) is interpreted as -1 if the sign bit of the multiplier is 1, and 0 if the sign bit of the multiplier is 0.

The unsigned multiply iterate (UMULI) performs an unsigned multiplication iteration. This instruction interprets M(8N-J) as the 8N-J bit of the multiplier. The shift is a double-precision right shift with the carry out from the P(J) + Multiplicand \times M(8N-J) operation forced into bit 8N of P(J + 1). This instruction is used in unsigned and mixed multiplication.

signed multiplication

Signed multiplication performs an $8N + 2$ clock two's complement multiply. The instructions necessary to produce an algebraically correct result proceed in the following manner:

Zero register to be used for accumulator

Load MQ with multiplier

SMULI (repeat 8N-1 times)

S port = Accumulator
R port = Multiplicand
F port = Iteration result

SMULT

S port = Accumulator
R port = Multiplicand
F port = Product (MSH)

At completion, the accumulator will contain the 8N most significant bits and the MQ contains the 8N least significant bits of the product.

The status for the signed multiply iterate should not be used for any testing (overflow is not set by SMULI). The following status is set for the signed multiply terminate instruction:

N → Result MSB equal one
OVR → Forced to zero
 C_{n+8} → Carry out equal to one
Z → Double precision result is zero

unsigned multiplication

Unsigned multiplication produces an unsigned times unsigned product in $8N + 2$ clocks. The instructions necessary to produce an algebraically correct result proceed in the following manner:

Zero register to be used for accumulator

Load MQ with multiplier

UMULI (8N times)

S port = Accumulator
R port = Multiplicand
F port = Iteration result (product MSH on final result)

Upon completion, the accumulator will contain the 8N most significant bits and the MQ contains the 8N least significant bits of the product.

The status set by the unsigned multiply iteration is meaningless except on the final execution of the instruction. The status set by the unsigned multiply iteration instruction is as follows:

- N → Result MSB equal one
- OVR → Forced to zero
- C_{n+8} → Carry out equal to one
- Z → Double-precision result is zero

mixed multiplication

Mixed multiplication multiplies a signed multiplicand times an unsigned multiplier to produce a signed result in 8N + 2 clocks. The steps are as follows:

Zero register used for accumulator

Load MQ with unsigned multiplier

SMULI (8N times)

- S port = Accumulator
- R port = Multiplicand
- F port = Iteration result

Upon completion, the accumulator will contain the 8N most significant bits and the MQ will contain the 8N least significant bits of the product.

The following status is set by the last SMULI instruction:

- N → Result MSB equal one
- OVR → Forced to zero
- C_{n+8} → Carry out equal to one
- Z → Double-precision result is zero

divide operations

The divide uses a nonrestoring technique to perform both signed and unsigned division of a 16N bit integer dividend and an 8N bit integer divisor (Figure 9). It produces an 8N integer quotient and remainder.

The remainder and quotient will be such that the following equation is satisfied:

$$(\text{Quotient}) \times (\text{Divisor}) + \text{Remainder} = \text{Dividend}$$

The processor has the following divide instructions:

1. UNSIGNED DIVIDE START (UDIVIS): I7-I0 = B0₁₆
2. UNSIGNED DIVIDE ITERATE (UDIVI): I7-I0 = C0₁₆
3. UNSIGNED DIVIDE TERMINATE (UDIVIT): I7-I0 = F0₁₆
4. SIGNED DIVIDE INITIALIZE (SDIVIN): I7-I0 = 80₁₆
5. SIGNED DIVIDE OVERFLOW TEST (SDIVO): I7-I0 = AF₁₆
6. SIGNED DIVIDE START (SDIVIS): I7-I0 = 90₁₆
7. SIGNED DIVIDE ITERATE (SDIVI): I7-I0 = A0₁₆
8. SIGNED DIVIDE TERMINATE (SDIVIT): I7-I0 = E0₁₆
9. DIVIDE REMAINDER FIX (DIVRF): I7-I0 = 40₁₆
10. SIGNED DIVIDE QUOTIENT FIX (SDIVQF): I7-I0 = 50₁₆

SN54AS888, SN74AS888
8-BIT PROCESSOR SLICES

2

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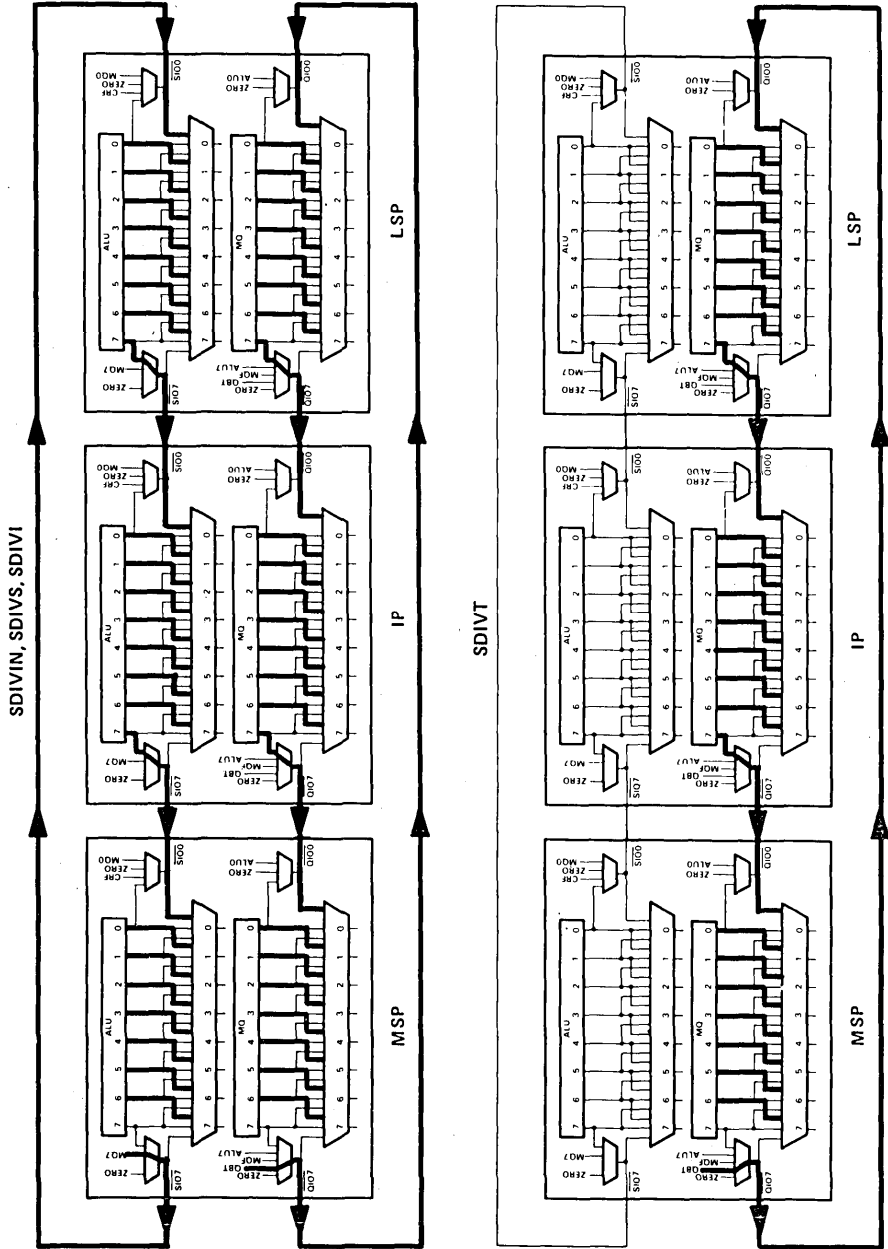


FIGURE 9. DIVIDE OPERATIONS

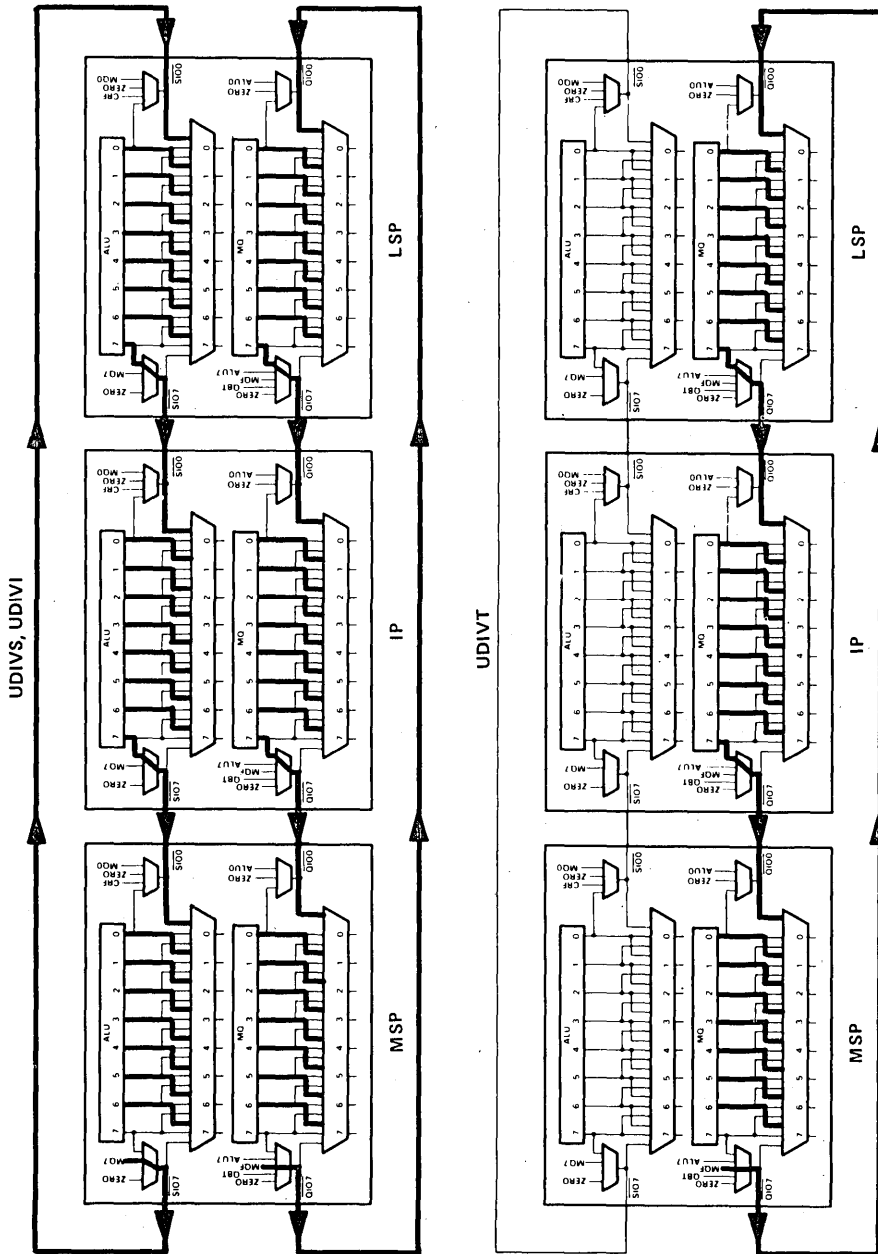


FIGURE 9. DIVIDE OPERATIONS (Continued)

SN54AS888, SN74AS888 8-BIT PROCESSOR SLICES

The unsigned divide iterate start (UDIVIS) instruction begins the iterate procedure while testing for overflow. Overflow is reported when the first subtraction of the divisor from the MSH of the dividend produces carry out. The test detects quotient overflow and divide by zero.

The unsigned divide iterate terminate (UDIVIT) instruction completes the iterate procedure generating the last quotient bit.

The signed divide initialize (SDIVIN) instruction prepares for iteration by shifting the dividend and storing the sign of the dividend for use in the following instructions and overflow tests.

The signed divide overflow test (SDIVO) checks for overflow possibilities. This instruction may be deleted from the divide operation if the OVR pin is ignored. If it is removed some overflow conditions will go undetected. \overline{WE} must be high (writing inhibited) when this instruction is used.

The signed divide iterate start (SDIVIS) instruction calculates the difference between the divisor and MSH of the dividend. Partial detection of overflow is also done during this instruction. Operations with like signs (positive quotient) and division by zero will overflow during this instruction (including zero divisor). Operations with unlike signs are tested for overflow during the signed divide quotient fix instruction (SDIVQF). Partial overflow results are saved and will be used during SDIVQF when overflow is reported.

The signed divide iterate (SDIVI) instruction forms the quotient and remainder through iterative subtract/add-shift operations of the divisor and dividend. One quotient bit is generated on each clock.

The signed divide iterate terminate (SDIVIT) instruction completes the iterate procedure, generating the last quotient bit. It also tests for a remainder equal to zero, which determines the action to be taken in the following correction (fix) instructions.

The divide remainder fix (DIVRF) instruction corrects the remainder. If a zero remainder was detected by the previous instructions, the remainder is forced to zero. For nonzero remainder cases where the remainder and dividend have the same sign, the remainder is correct. When the remainder and dividend have unlike signs, a correction add/subtract of the divisor to the remainder is performed.

The signed divide quotient fix (SDIVQF) instruction corrects the quotient if necessary. This correction requires adding one to the incorrect quotient. An incorrect quotient results if the signs of the divisor and dividend differ and the remainder is nonzero. An incorrect quotient also results if the sign of the divisor is negative and the remainder is zero.

Overflow detection is completed during this instruction. Overflow may be generated for differing signs of the dividend and divisor. The partial overflow test result performed during SDIVIS is ORed with this test result to produce a true overflow indication.

signed divide usage

The instructions necessary to perform an algebraically correct division of signed numbers are as follows:

Load MQ with the least significant half of the dividend

SDIVIN	S port = MSH of dividend
	R port = Divisor
	F port = Intermediate result
SDIVO	S port = Result of SDIVIN
	R port = Divisor
	F port = Test result
	(\overline{WE} must be high)
SDIVIS	S port = Result of SDIVIN
	R port = Divisor
	F port = Intermediate result

SDIVI (8N-2 times)	S port = Result of SDIVIS (or SDIVI) R port = Divisor F port = Intermediate result
SDIVIT	S port = Result of last SDIVI R port = Divisor F port = Intermediate result
DIVRF	S port = Result of SDIVIT R port = Divisor F port = Remainder
SDIVQF	S port = MQ register R port = Divisor F port = Quotient

The status of all signed divide instructions except SDIVIN, DIVRF, and SDIVQF is as follows:

N	→ Forced to zero
OVR	→ Forced to zero
C _{n+8}	→ Carry out equal to one
Z	→ Intermediate result is zero

The status of the SDIVIN instruction is as follows:

N	→ Forced to zero
OVR	→ Forced to zero
C _{n+8}	→ Forced to zero
Z	→ Divisor is zero

The status of the DIVRF instruction is as follows:

N	→ Forced to zero
OVR	→ Forced to zero
C _{n+8}	→ Carry out equal to one
Z	→ Remainder is zero

The status of the SDIVQF instruction is as follows:

N	→ Sign of quotient
OVR	→ Divide overflow
C _{n+8}	→ Carry out equal to one
Z	→ Quotient is zero

The quotient is stored in the MQ register and the remainder is stored in the register file location that originally held the most significant word of the dividend. If fractions are divided, the quotient must be shifted right one bit and the remainder right three bits to obtain the correct fractional representations.

The signed division algorithm is summarized in Table 7.

TABLE 7. SIGNED DIVISION ALGORITHM

OP CODE	MNEMONIC	CLOCK CYCLES	INPUT S PORT	INPUT R PORT	OUTPUT F PORT
E4	LOADMQ	1	Dividend (LSH)	—	Dividend (LSH)
80	SDIVN	1	Dividend (MSH)	Divisor	Remainder (N)
AF	SDIVO	1	Remainder (N)	Divisor	Test Result
90	SDIVIS	1	Remainder (N)	Divisor	Remainder (N)
A0	SDIVI	8N - 2†	Remainder (N)	Divisor	Remainder (N)
E0	SDIVIT	1	Remainder (N)	Divisor	Remainder (Unfixed)
40	DIVRF	1	Remainder (Unfixed)	Divisor	Remainder
50	SDIVQF	1	MQ Register	Divisor	Quotient

†N = Number of cascaded packages.

unsigned divide usage

The instructions necessary to perform an algebraically correct division of unsigned numbers are as follows:

Load MQ with the least significant half of the dividend

- UDIVIS S port = MSH of dividend
 R port = Divisor
 F port = Intermediate result
- UDIVI (8N-1 times) S port = Result of UDIVIS (OR UDIVI)
 R port = Divisor
 F port = Intermediate result
- UDIVIT S port = Result of last UDIVI
 R port = Divisor
 F port = Remainder (unfixed)
- DIVRF S port = Result of UDIVIT
 R port = Divisor
 F port = Remainder

The status of all unsigned divide instructions except UDIVIS is as follows:

- N → Forced to zero
- OVR → Forced to zero
- C_{n+8} → Carry out equal to one
- Z → Intermediate result is zero

The status of the UDIVIS instruction is as follows:

- N → Forced to zero
- OVR → Divide overflow
- C_{n+8} → Carry out equal to one
- Z → Intermediate result is zero

If fractions are divided, the remainder must be shifted right two bits to obtain the correct fractional representation. The quotient is correct as is. The quotient is stored in the MQ register at the completion of the divide.

The unsigned division algorithm is summarized in Table 8.

TABLE 8. UNSIGNED DIVISION ALGORITHM

OP CODE	MNEMONIC	CLOCK CYCLES	INPUT S PORT	INPUT R PORT	OUTPUT F PORT
E4	LOADMQ	1	Dividend (LSH)	—	Dividend (LSH)
B0	UDIVIS	1	Dividend (MSH)	Divisor	Remainder (N)
C0	UDIVI	8N - 1†	Remainder (N)	Divisor	Remainder (N)
F0	UDIVIT	1	Remainder (N)	Divisor	Remainder (Unfixed)
40	DIVRF	1	Remainder (Unfixed)	Divisor	Remainder

† N = Number of cascaded packages.

group 5 instructions

Hex code F of Group 1 instructions is used to access Group 5 instructions. Group 5 instructions are summarized in Table 9.

TABLE 9. GROUP 5 INSTRUCTIONS

INSTRUCTION BITS (I7-I0) OP CODE (HEX)	MNEMONIC	FUNCTION
0F	CLR	Clear
1F	CLR	Clear
2F	CLR	Clear
3F	CLR	Clear
4F	CLR	Clear
5F	CLR	Clear
6F	CLR	Clear
7F	BCDBIN	BCD to Binary
8F	EX3BC	Excess-3 Byte Correction
9F	EX3C	Excess-3 Word Correction
AF	SDIVO	Signed Divide Overflow Check
BF	CLR	Clear
CF	CLR	Clear
DF	BINEX3	Binary to Excess-3
EF	CLR	Clear
FF	NOP	No Operation

clear instructions (CLR)

There are 11 clear instructions listed in Table 9. The instructions force the ALU output to be zero and the BCD flip-flops to be cleared. The status set by the clear instruction is as follows:

- N → None (force to zero)
- OVR → None (force to zero)
- C_{n+8} → None (force to zero)
- Z → Active (one)

no operation instruction (NOP): I7-I0 = FF₁₆

This instruction is identical to the clear instructions except that the BCD flip-flops retain their old value.

SN54AS888, SN74AS888 8-BIT PROCESSOR SLICES

excess-3 correction instructions (EX3BC, EX3C)

Two excess-3 correction instructions are available:

1. Excess-3 byte correction (EX3BC): I7-I0 = 8F₁₆
2. Excess-3 word correction (EX3C): I7-I0 = 9F₁₆

One instruction supports the byte mode and the other supports the word mode. These instructions correct the excess-3 additions (subtractions) in either the byte or word mode. For correct excess-3 arithmetic, this instruction must follow each add/subtract. The operand must be on the S port.

NOTE: The previous arithmetic overflow should be ignored.

The status of the EX3C instruction is as follows:

N	→	MSB of result
OVR	→	Signed overflow
C _n +8	→	Carry out equal one
Z	→	None (force to one)

The status of the EX3BC instruction is as follows:

N	→	None (force to zero)
OVR	→	Byte signed overflow
C _n +8	→	Carry out equal one
Z	→	None (force to one)

radix conversions

Conversions between decimal and binary number representations are performed with the aid of two special instructions: BINEX3 and BCDBIN.

BCD to binary instructions (BCDBIN): I7-I0 = 7F₁₆

This instruction (Figure 10) allows the user to convert an N-digit BCD number to a 4N-bit binary number in 4(N-1) plus 8 clocks. This function sums the R bus, the S bus, and the C_n bit, performs an arithmetic left shift on the ALU result, and simultaneously circular shifts the MQ left. The status set by the BCD to binary instruction is as follows:

N	→	MSB of result
OVR	→	Signed arithmetic overflow [†]
C _n +8	→	Carry out equal one
Z	→	Result equal zero

[†] Overflow may be the result of an ALU operation or the arithmetic left shift operation.

The following code illustrates the BCD to binary conversion technique.

Let ACC be an accumulator register
Let NUM be the register which contains the BCD number
Let MSK be a mask register

```

M1:      LOADMQ NUM                ; LOAD MQ WITH BCD NUMBER
M2:      SUB ACC, ACC, SLCMQ        ; CLEAR ACC AND ALIGN MQ
M3:      SUB, MSK, MSK, SLCMQ      ; CLEAR MSK AND ALIGN MQ
M4:      SLCMQ                      ; ALIGN
M5:      SLCMQ                      ; ALIGN
M6:      ADDI ACC, MSK, 1510        ; MSK = 1510

; REPEAT L1 THRU L4
; N-1 TIMES (N = number of
; BCD digits)
L1:      AND MQ, MSK, R1, SLCMQ    ; EXTRACT ONE DIGIT
; ALIGN MQ
L2:      ADD, ACC, R1, R1, SLCMQ   ; ACC + DIGIT
; IS STORED IN R1
; ALIGN MQ
L3:      BCDBIN, R1, R1, ACC       ; 4 × (ACC + DIGIT)
; IS STORED IN ACC
; ALIGN MQ
L4:      BCDBIN, ACC, R1, ACC      ; 10 × (ACC + DIGIT)
; IS STORED IN ACC
; ALIGN MQ
M7:      AND MQ, MSK, R1           ; FETCH LAST DIGIT
M8:      ACC+R1 → ACC              ; ADD IN LAST DIGIT

```

The previous code generates a binary number by executing the standard conversion formula for a BCD number (shown for 32 bits).

$$ABCD = [(A \times 10 + B) \times 10 + C] \times 10 + D$$

Notice that the conversion begins with the most significant BCD digit and that the addition is performed in radix 2.

binary to excess-3 instructions (BINEX3): I7-I0 = DF16

This instruction (Figure 11) allows the user to convert an N-bit binary number to an N/4-bit excess-3 number representation in $2N + 3$ clocks. The data on the R and S ports are summed with the MSB of the MQ register. The MQ register is simultaneously shifted left circularly. The status set by the binary to excess-3 instruction is as follows:

N → MSB of result
OVR → Signed arithmetic overflow
 $C_n + 8$ → Carry out equal one
Z → Result equal zero

SN54AS888, SN74AS888
8-BIT PROCESSOR SLICES

2

LSI Devices

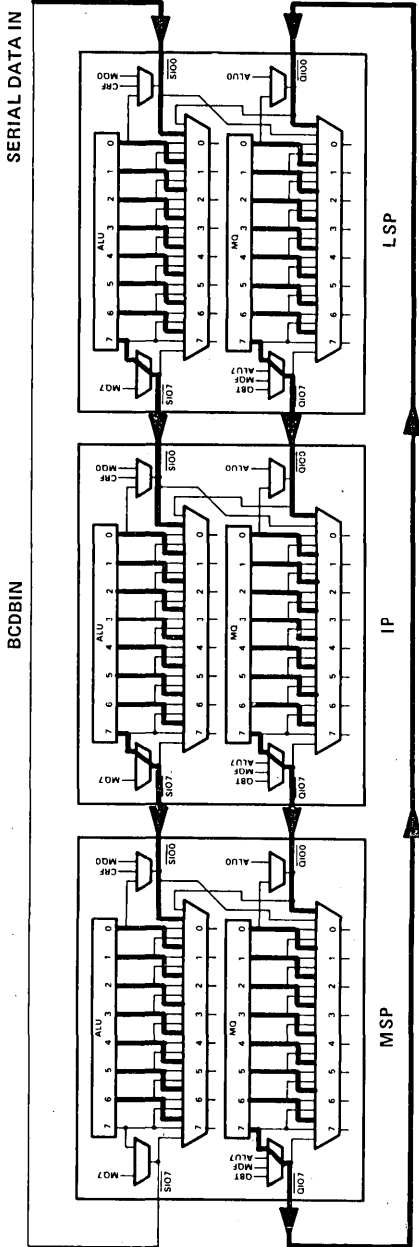


FIGURE 10. BCD TO BINARY

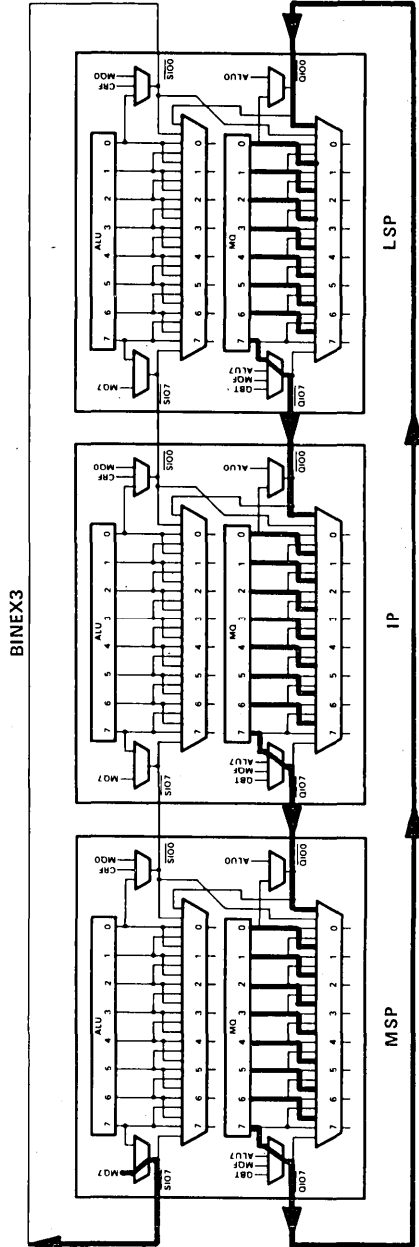


FIGURE 11. BINARY TO EXCESS-3

The following illustrates the binary to excess-3 conversion technique.

Let NUM be a register containing an unsigned binary number
Let ACC be an accumulator

M1:	LOADMQ NUM	; LOAD MQ WITH BINARY ; NUMBER
M2:	CLEAR ACC	; CLEAR ACC
M3:	SET1 ACC H/33/	; ACC → HEX/3333 . . .
L1:	BINEX3 ACC, ACC, ACC	; DOUBLE ACC AND ADD IN ; MSB OF MQ ; ALIGN MQ
L2:	EX3C ACC, ACC	; EXCESS 3 CORRECT ; REPEAT L1 AND L2 ; N-1 TIMES

The previous code generates an excess-3 number by executing the standard conversion formula for a binary number.

$$a_n 2^n + a_{n-1} 2^{n-1} + a_{n-2} 2^{n-2} + \dots + a_0 2^0 = [(2a_n + a_{n-1})2 + a_{n-2}]2 + \dots + a_0$$

Notice that the conversion begins with the most significant binary bit and that the addition is performed in radix-10 (excess-3).

decimal arithmetic

Decimal numbers are represented in excess-3 code. Excess-3 code numbers may be generated by adding three to each digit of a Binary Coded Decimal (BCD) number. The hardware necessary to implement excess-3 arithmetic is only slightly different from binary arithmetic. Carries from one digit to another during addition in BCD occur when the sum of the two digits plus the carry-in is greater than or equal to ten. If both numbers are excess-3, the sum will be excess-6, which will produce the proper carries. Therefore, every addition or subtraction operation may use the binary adder. To convert the result from excess-6 to excess-3, one must consider two cases resulting from a BCD digit add: (1) where a carry-out is produced, and (2) where a carry-out is not produced. If a carry-out is not produced, three must be subtracted from the resulting digit. If a carry is produced, the digit is correct as a BCD number. For example, if BCD 5 is added to BCD 6, the excess-3 result would be $8 + 9 = 1$ (with a carry). A carry rolls the number through the illegal BCD representations into a correct BCD representation. Binary 3 must be added to digit positions that produce a carry-out to correct the result to an excess-3 representation. Every addition and subtraction instruction stores the carry generated from each 4-bit digit location for use by the excess-3 correction functions. These correction instructions (word or byte) must be executed in the clock cycle immediately after the addition or subtraction operation.

Signed numbers may be represented in ten's complement form by complementing the excess-3 number. As an example, add the decimal number -423 to the decimal number 24, which will be represented by 8AA and 357 in excess-3, respectively.

8AA	
357	
C01	Sum
011	Carry
934	Excess-3 correct
-6CC	Complement
-399	Excess-3 to decimal

Complements of excess-3 numbers may be generated by subtracting the excess-3 number from an excess-3 zero followed by an excess-3 correct.

SN54AS888, SN74AS888 8-BIT PROCESSOR SLICES

excess-3 to USASCII conversion

Input/output devices or files represent numbers differently than high-speed central processing units. I/O devices handle all alphanumeric data similarly. CPUs handle more numeric data than alphabetic data and store numeric data in packed form to minimize calculation throughout and reduce memory requirements. To represent the cost of a shirt that was \$10.96, the I/O device would handle the six USASCII characters "\$", "1", "0", ".", "9", "6", which would require 6 bytes of storage. In packed BCD, this number could be stored as 1096 in two bytes of data. The 'AS888 may be programmed to perform data format conversions such as converting excess-3 BCD to USASCII.

The code below converts a packed word of excess-3 BCD to two unpacked words of USASCII code. Instruction "MAIN1" reads the input word from memory into Register O (R0). For illustrative purposes, suppose this data was 43C9, which represents the \$10.96 shirt in excess-3 code. "MAIN2" and "MAIN3" generate a constant of 2D2D₁₆, which is an offset constant to convert excess-3 numbers to USASCII. "MAIN4" copies R0 into R2 to set up the subroutine parameters and calls the subroutine "UNPACK", "UNPACK2" strips off the upper byte leaving OOC9 in R2. "UNPACK2" and "UNPACK3" together shift the contents of R2 one character position and places the result OC90 into R3. "UNPACK4" performs a logical OR operation to produce OCD9 in register 2. "UNPACK5" clears the most significant nibble in each byte to produce OC09 in R2. "UNPACK6" adds the constant 2D2D₁₆ to R2 to produce 3936 the USASCII representation of the numerals 96 and returns program control to "MAIN5". "MAIN5" through "MAIN9" align the two remaining characters and call UNPACK and the process repeats. Finally the USASCII representation of 1096 is stored into memory. (Note that no attempt was made to pack the "\$" or "." characters.)

Unpacking Excess-3 to USASCII:

```

MAIN1:  READ, RFA(0)                ; READ IN PACKED EXCESS-3
MAIN2:  XOR, RFA(4), RFB(4), RFC(4) ; CLEAR R4
MAIN3:  SET1, RFB(40), RDC(2), RFA(D), ; GENERATE HEXADECIMAL
        MSH, LSH                    ; 2D2D16
MAIN4:  MOVE, RFA(0), RFC(2), JSR(UNPACK) ; COPY RFA(0) INTO RFA(2),
        ; PROCEDURE CALL
MAIN5:  MOVE, RFA(2), RFC(1)        ; TWO CHARACTERS IN R1
MAIN6:  ADDR, RFB(0), RFA(0), RFC(0), SLC ; R0 SHIFTED 2
MAIN7:  ADDR, RFB(0), RFA(0), RFC(0), SLC ; R0 SHIFTED 4
MAIN8:  ADDR, RFB(0), RFA(0), RFC(0), SLC ; R0 SHIFTED 6
MAIN9:  ADDR, RFB(0), RFA(0), RFC(0), SLC ; R0 SHIFTED 8
        JSR (UNPACK)
MAIN10: STORE, RFA(1)                ; STORE USASCII, TWO
        ; CHARACTERS IN R2
MAIN11: STORE, RFA(2)                ; STORE USASCII
UNPACK1: SET0, RFB(2), RFC(F), MSH    ; CLEAR MSH
UNPACK2: ADDR, RFB(2), RFA(2), RFC(3), SLC ; SHIFT R2 TWO PLACES
UNPACK3: ADDR, RFB(3), RFA(3), RFC(3), SLC ; SHIFT R3 TWO PLACES
UNPACK4: OR, RFB(2), RFA(3), RFC(2)   ; OR R3 TO R2
UNPACK5: SET0, RFB(2), RFC(F), RFA(0), LSH, MSH ; CLEAR MOST SIGNIFICANT 4
        ; BITS IN EACH BYTE
UNPACK6: ADDR, RFB(2), RFB(4), RFC(2), RTS ; ADD HEX 2D, RETURN

```

SN54AS888, SN74AS888 8-BIT PROCESSOR SLICES

absolute maximum rating over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC1	7 V
Supply voltage, VCC2	3 V
Input voltage	7 V
High-level voltage applied to 3-state outputs	5.5 V
Operating case temperature range: SN54AS888	-55°C to 125°C
Operating free-air temperature range: SN74AS888, SN74AS888-1	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54AS888			SN74AS888 SN74AS888-1			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
VCC1	I/O supply voltage	4.5	5	5.5	4.5	5	5.5	V
VCC2	STL internal logic supply voltage	1.9	2	2.1	1.9	2	2.1	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage				0.8			V
I _{OH}	High-level output current				-1			mA
I _{OL}	Low-level output current	All output except \bar{G} and ZERO			8			mA
		\bar{G}			16			
		ZERO			48			
T _C	Operating case temperature	-55			125			°C
T _A	Operating free-air temperature				0			

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54AS888			SN74AS888 SN74AS888-1			UNIT
			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
V _{IK}		VCC1 = 4.5 V, I _I = -18 mA	-1.2			-1.2			V
V _{OH}	All outputs except ZERO	VCC1 = 4.5 V to 5.5 V, I _{OH} = -0.4 mA	V _{CC-2}			V _{CC-2}			V
		VCC1 = 4.5 V, I _{OH} = -1 mA	2.4			2.4			
		VCC1 = 4.5 V, I _{OH} = -2.6 mA							
I _{OH}	ZERO	VCC1 = 4.5 V, V _{OH} = 5.5 V	0.1			0.1			mA
V _{OL}	All outputs except \bar{G} and ZERO	VCC1 = 4.5 V, I _{OL} = 8 mA	0.5			0.5			V
		\bar{G}	0.5			0.5			
		ZERO	0.5			0.5			
I _I	I/O	VCC1 = 5.5 V, V _I = 5.5 V	0.1			0.1			mA
	All others	VCC1 = 5.5 V, V _I = 7 V	0.1			0.1			
I _{IH} [‡]		VCC1 = 5.5 V, V _I = 2.7 V	20			20			μA
I _{IL} [‡]		VCC1 = 5.5 V, V _I = 0.5 V	-0.4			-0.4			mA
I _O [§]		VCC1 = 5.5 V, V _O = 2.25 V	-30	-112	-30	-112	-112	mA	
I _{CC1}		VCC1 = 5.5 V	150			130			mA
I _{CC2}		VCC2 = 2.1 V	410			390			mA

[†]All typical values are at VCC = 5 V, T_A = 25°C.

[‡]For I/O ports, the parameters I_{IH} and I_{IL} include the off-state current.

[§]The output conditions have been chosen to produce a current that closely approximates one-half the true short-circuit current, I_{OS}.

2
LSI Devices

SN54AS888, SN74AS888

8-BIT PROCESSOR SLICES

SN54AS888 maximum switching characteristics, $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $T_C = -55^\circ\text{C to }125^\circ\text{C}$ (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)										UNIT
		Y	C_{n+8}	\bar{G}, \bar{P}	Z^\dagger	N	OVR	DA	DB	$\bar{Q}iO$	$\bar{S}iO$	
t_{pd}	A3-A0 B3-B0	62	42	48	69	62	60	18	18	65	66	ns
	DA7-DA0, DB7-DB0	47	28	28	58	50	42	-	-	50	50	
	C_n	25	14	-	32	24	18	-	-	32	32	
	EA	54	32	35	62	52	52	-	-	58	58	
	$\bar{E}B$	54	32	35	62	52	52	-	-	58	58	
	I7-I0	58	32	32	62	52	41	-	-	58	58	
	$\bar{O}E\bar{B}$	-	-	-	-	-	-	-	14	-	-	
	O $\bar{E}Y$	14	-	-	-	-	-	-	-	-	-	
	$\bar{Q}iO$ (n) Shift	15	-	-	24	-	-	-	-	-	-	
	$\bar{S}iO$ (n) Shift	15	-	-	24	22	-	-	-	-	-	
	CK	68	60	56	62	50	68	38	38	70	70	
	$\bar{O}E\bar{A}$	-	-	-	-	-	-	14	-	-	-	
	SSF ‡	-	-	-	-	-	14	-	-	-	-	

† Load resistor $R_1 = 100\ \Omega$.

‡ For byte instructions only.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN74AS888 maximum switching characteristics, $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $T_A = 0^\circ\text{C to }70^\circ\text{C}$ (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)										UNIT
		Y	C_{n+8}	\bar{G}, \bar{P}	Z^\dagger	N	OVR	DA	DB	$\bar{Q}iO$	$\bar{S}iO$	
t_{pd}	A3-A0 B3-B0	54	36	42	60	52	50	18	18	58	58	ns
	DA7-DA0, DB7-DB0	44	26	26	52	46	38	-	-	44	44	
	C_n	25	8	-	32	24	18	-	-	31	31	
	EA	49	29	29	58	49	47	-	-	54	54	
	$\bar{E}B$	49	29	29	58	49	47	-	-	54	54	
	I7-I0	55	30	30	60	49	39	-	-	54	54	
	$\bar{O}E\bar{B}$	-	-	-	-	-	-	-	12	-	-	
	O $\bar{E}Y$	12	-	-	-	-	-	-	-	-	-	
	$\bar{Q}iO$ (n) Shift	15	-	-	24	-	-	-	-	-	-	
	$\bar{S}iO$ (n) Shift	15	-	-	24	19	-	-	-	-	-	
	CK	58	55	52	61	52	62	35	35	60	60	
	$\bar{O}E\bar{A}$	-	-	-	-	-	-	12	-	-	-	
	SSF ‡	-	-	-	-	-	12	-	-	-	-	

† Load resistor $R_1 = 100\ \Omega$.

‡ For byte instructions only.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

**SN54AS888, SN74AS888
8-BIT PROCESSOR SLICES**

SN74AS888-1 maximum switching characteristics, $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $T_A = 0^\circ\text{C to }70^\circ\text{C}$ (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)										UNIT
		Y	C_n+8	\bar{G}, \bar{P}	Z \bar{T}	N	OVR	DA	DB	$\bar{Q}IO$	$\bar{S}IO$	
t_{pd}	A3-A0 B3-B0	44	30	36	50	44	44	17	17	48	48	ns
	DA7-DA0, DB7-DB0	36	24	24	46	41	32	—	—	40	40	
	C_n	22	8	—	27	21	16	—	—	25	25	
	$\bar{E}A$	40	25	25	49	41	41	—	—	44	44	
	$\bar{E}B$	40	25	25	49	41	41	—	—	44	44	
	I7-I0	46	27	27	50	42	35	—	—	45	45	
	$\bar{O}EB$	—	—	—	—	—	—	—	12	—	—	
	$\bar{O}EY$	12	—	—	—	—	—	—	—	—	—	
	$\bar{Q}IO$ (n) Shift	14	—	—	20	—	—	—	—	—	—	
	$\bar{S}IO$ (n) Shift	14	—	—	20	18	—	—	—	—	—	
	CK	50	46	46	50	50	50	30	30	50	50	
	$\bar{O}EA$	—	—	—	—	—	—	12	—	—	—	
SSF \ddagger	—	—	—	—	—	—	12	—	—	—		

\dagger Load resistor $R_1 = 100\ \Omega$.

\ddagger For byte instructions only.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

register file write setup and hold times

PARAMETER		SN54AS888		SN74AS888		SN74AS888-1		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{su}	C3-C0	8		7		6		ns
	DB \S	14		12		11		
	I7-I4	16		14		13		
	I3-I0	24		22		21		
	$\bar{O}EY$	4		3		3		
	Y7-Y0	2		2		2		
	$\bar{W}E$	8		6		6		
	$\bar{Q}IO$ (n), $\bar{S}IO$ (n)	6		5		5		
t_h	SELY	8		6		6		ns
	C3-C0	0		0		0		
	DB \S	0		0		0		
	I7-I4	0		0		0		
	I3-I0	0		0		0		
	$\bar{O}EY$	6		5		5		
	Y7-Y0	10		10		10		
	$\bar{W}E$	3		2		2		
$\bar{Q}IO$ (n), $\bar{S}IO$ (n)	0		0		0			
SELY	8		6		6			

\S DB (during select instruction) through Y port.

2
LSI Devices

SN54AS888, SN74AS888 8-BIT PROCESSOR SLICES

special instruction switching characteristics

During various special instructions, the SSF pin is used to pass required information between the 'AS888 packages which make up a total system.

For instance, during the multiplication process, the LSB of the multiplier determines whether an ADD/SHIFT or SHIFT operation is performed. During multiplication, the SSF pin of the least significant package (LSP) becomes an output pin while all other packages become input pins.

Similarly, during normalization, the required operation depends on whether the two data MSBs are the same or different. Therefore, during normalization the SSF pin of the most significant package (MSP) becomes an output pin while all other packages become input pins.

Tables 10, 11, and 12 list the instructions which force the SSF pin during their execution. The propagation delay from various inputs is also shown. The parameter which limits normal system performance is indicated by a dagger.

TABLE 10. SN54AS888 SSF PIN DELAYS AND SETUP TIMES

MNEMONIC	HEX CODE	SSF SOURCE		INPUT → SSF (ns)				SSF SETUP
		LSP	MSP	C _n	I _(n)	CK	B _(n)	TIME (ns)
CRC	00	X		—	29	58	40 [†]	20
SNORM	20		X	—	29 [†]	46	—	20
DNORM	30		X	—	29	55	40 [†]	20
DIVRF	40		X	—	29 [†]	46	—	20
SDIVQF	50		X	—	26 [†]	—	—	18
SMULI	60	X		—	26 [†]	43	—	0
SDIVIN	80		X	—	48	64	44 [†]	0
SDIVIS	90		X	26 [†]	51	64	55	0
SDIVI	A0		X	26 [†]	51	64	55	0
UDIVIS	B0		X	18 [†]	45	64	46	0
UDIVI	C0		X	18 [†]	50	54	40	0
UMULI	D0	X		—	25 [†]	48	—	0
SDIVIT	E0		X	26 [†]	50	56	54	0
ABX	48		X	—	34	62	39 [†]	20
SMTC	58		X	—	29	58	39 [†]	20
BINEX3	DF		X	—	29 [†]	58	—	18
LOADMQ (Arith)		X		23 [†]	34	62	40	0
LOADMQ (Log)		X		—	33	62	40 [†]	0
BADD	88	↑ SOURCE IS MOST SIGNIFICANT BYTE SELECTED ↓		18 [†]	58	62	49	—
BSUBS	98			18 [†]	58	62	49	—
BSUBR	A8			18 [†]	58	71	49	—
BINCS	B8			18 [†]	58	60	49	—
BINCNS	C8			18 [†]	58	71	49	—
BXOR	D8			—	58	—	—	—
BAND	E8			—	58	—	—	—
BOR	F8			—	58	—	—	—
EX3BC	8F			—	58	46	49 [†]	—

[†] This parameter limits normal system performance.

TABLE 11. SN74AS888 SSF PIN DELAYS AND SETUP TIMES

MNEMONIC	HEX CODE	SSF SOURCE		INPUT → SSF (ns)				SSF SETUP
		LSP	MSP	C _n	I _(n)	CK	B _(n)	TIME (ns)
CRC	00	X		—	26	52	37 [†]	17
SNORM	20		X	—	26 [†]	40	—	17
DNORM	30		X	—	26	52	37 [†]	17
DIVRF	40		X	—	26 [†]	40	—	17
SDIVQF	50		X	—	25 [†]	—	—	17
SMULI	60	X		—	25 [†]	40	—	0
SDIVIN	80		X	—	38	60	40 [†]	0
SDIVIS	90		X	24 [†]	48	60	52	0
SDIVI	A0		X	24 [†]	48	60	52	0
UDIVIS	B0		X	17 [†]	43	60	45	0
UDIVI	C0		X	17 [†]	44	52	37	0
UMULI	D0	X		—	26 [†]	40	—	0
SDIVIT	E0		X	25 [†]	46	52	49	0
ABX	48		X	—	32	60	38	17
SMTC	58		X	—	26	52	38 [†]	17
BINEX3	DF		X	—	26 [†]	40	—	17
LOADMQ (Arith)		X		22 [†]	32	50	38	0
LOADMQ (Log)		X		—	32	50	38 [†]	0
BADD	88	↑ SOURCE IS MOST SIGNIFICANT BYTE SELECTED ↓		17 [†]	52	55	46	—
BSUBS	98			17 [†]	52	55	46	—
BSUBR	A8			17 [†]	52	62	46	—
BINCS	B8			17 [†]	52	55	46	—
BINCNS	C8			17 [†]	52	62	46	—
BXOR	D8			—	52	—	—	—
BAND	E8			—	52	—	—	—
BOR	F8			—	52	—	—	—
EX3BC	8F	—	45	45	46 [†]	—		

[†] This parameter limits normal system performance.

SN54AS888, SN74AS888
8-BIT PROCESSOR SLICES

TABLE 12. SN74AS888-1 SSF PIN DELAYS AND SETUP TIMES

MNEMONIC	HEX	SSF SOURCE		INPUT → SSF (ns)				SSF SETUP TIME (ns)
	CODE	LSP	MSP	C _n	I _(n)	CK	B _(n)	
CRC	00	X		—	23	42	34 [†]	14
SNORM	20		X	—	23 [†]	28	—	14
DNORM	30		X	—	23	40	34 [†]	14
DIVRF	40		X	—	23 [†]	27	—	14
SDIVQF	50		X	—	23 [†]	—	—	14
SMULI	60	X		—	22 [†]	27	—	0
SDIVIN	80		X	—	35	46	35 [†]	0
SDIVIS	90		X	22 [†]	42	48	42	0
SDIVI	A0		X	22 [†]	42	46	42	0
UDIVIS	B0		X	16 [†]	42	46	38	0
UDIVI	C0		X	16 [†]	36	46	34	0
UMULI	D0	X		—	22 [†]	27	—	0
SDIVIT	E0		X	21 [†]	40	44	42	0
ABX	48		X	—	28	46	30 [†]	14
SMTC	58		X	—	24	44	30 [†]	14
BINEX3	DF		X	—	23 [†]	27	—	14
LOADMQ (Arith)		X		19 [†]	28	40	30	0
LOADMQ (Log)		X		—	28	35	30 [†]	0
BADD	88			16 [†]	42	42	40	—
BSUBS	98			16 [†]	42	40	40	—
BSUBR	A8			16 [†]	42	50	40	—
BINCS	B8			16 [†]	42	46	40	—
BINCNS	C8			16 [†]	42	54	42	—
BXOR	D8			—	42	—	—	—
BAND	E8			—	42	—	—	—
BOR	F8			—	42	—	—	—
EX3BC	8F			—	42	42	42 [†]	—

[†] This parameter limits normal system performance.

2 LSI Devices

SN54AS890, SN74AS890 MICROSEQUENCERS

D2662, NOVEMBER 1982—REVISED APRIL 1985

- 14 Bits Wide—Addresses up to 16,384 Words of Microcode with One Chip
- Selects Address from One of Eight Sources
- STL-AS Technology
- Independent Read Pointer for Aid in Microcode Diagnostics
- Supports Real-Time Interrupts
- Two Independent Loop Counters
- Supports 64 Powerful Instructions
- Dependable Texas Instruments Quality and Reliability

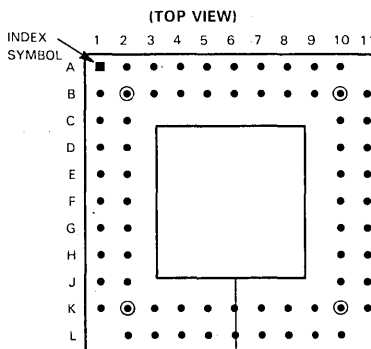
description

The 'AS890 is a powerful microsequencer that is the result of the implementation of TI's Advanced Schottky and Schottky Transistor Logic. Approximately 2400 Schottky gate equivalents are used to construct this high-performance sequencer. The 'AS890 can generate an address and provide register status in only 29 ns while typically requiring only 1.8 watts of power. All internal STL logic in these devices operates on a 2-volt power supply that must be supplied externally. The information generated by the internal STL logic is communicated in the rest of the system via 5-volt Advanced Schottky TTL-compatible I/O ports.

The microsequencers select a 14-bit microaddress from one of eight sources to provide the proper microinstruction sequence for bit-slice processor or other microcode based systems. These high-performance devices are capable of addressing 16,384 control store memory locations either sequentially or via conditional branching algorithms. This multiway branching capability, coupled with a nine-word deep FILO (first in, last out) stack, allows the microprogrammer to arrange his code in blocks so that microprograms may be structured in the same fashion as such high-level languages as ALGOL, Pascal, or Ada.

Both polled and real-time interrupt routines are supported by the 'AS890 to enhance system throughput capability. Vectored interrupts may occur during any instruction, including PUSHes and POPs.

SN74AS890 . . . GB PACKAGE



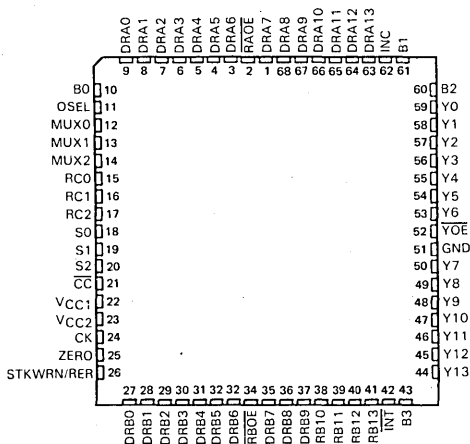
AS890

NO.	PIN	NAME	NO.	PIN	NAME	NO.	PIN	NAME	NO.	PIN	NAME
A-2	DRB10		B-9	STKWRN/RER	F-10	VCC1	K-4	DRA13			
A-3	DRB9		B-10	ZERO	F-11	MUX2	K-5	DRA11			
A-4	DRB8		B-11	CK	G-1	Y5	K-6	DRA8			
A-5	DRB7		C-1	Y13	G-2	VOE	K-7	DRA7			
A-6	DRB6		C-2	Y10	G-10	RC1	K-8	DRA0			
A-7	DRB5		C-10	CC	G-11	MUX1	K-9	DRA1			
A-8	DRB4		C-11	S1	H-1	Y4	K-10	DRA3			
A-9	DRB3		D-1	Y12	H-2	Y6	K-11	DRA2			
A-10	DRB1		D-2	Y9	H-10	B0	L-2	B2			
B-1	DRB13		D-10	S2	H-11	MUX0	L-3	INC			
B-2	INT		D-11	S0	J-1	Y3	L-4	DRA12			
B-3	DRB12		E-1	Y11	J-2	Y2	L-5	DRA10			
B-4	DRB11		E-2	Y8	J-10	RC2	L-6	DRA9			
B-5	B3		E-10	VCC2	J-11	OSEL	L-7	RAOE			
B-6	RBOE		E-11	RC0	K-1	Y1	L-8	DRA6			
B-7	DRB2		F-1	Y7	K-2	Y0	L-9	DRA5			
B-8	DRB0		F-2	GND	K-3	B1	L-10	DRA4			

SN54AS890 . . . FD PACKAGE

SN74AS890 . . . FN PACKAGE

(TOP VIEW)



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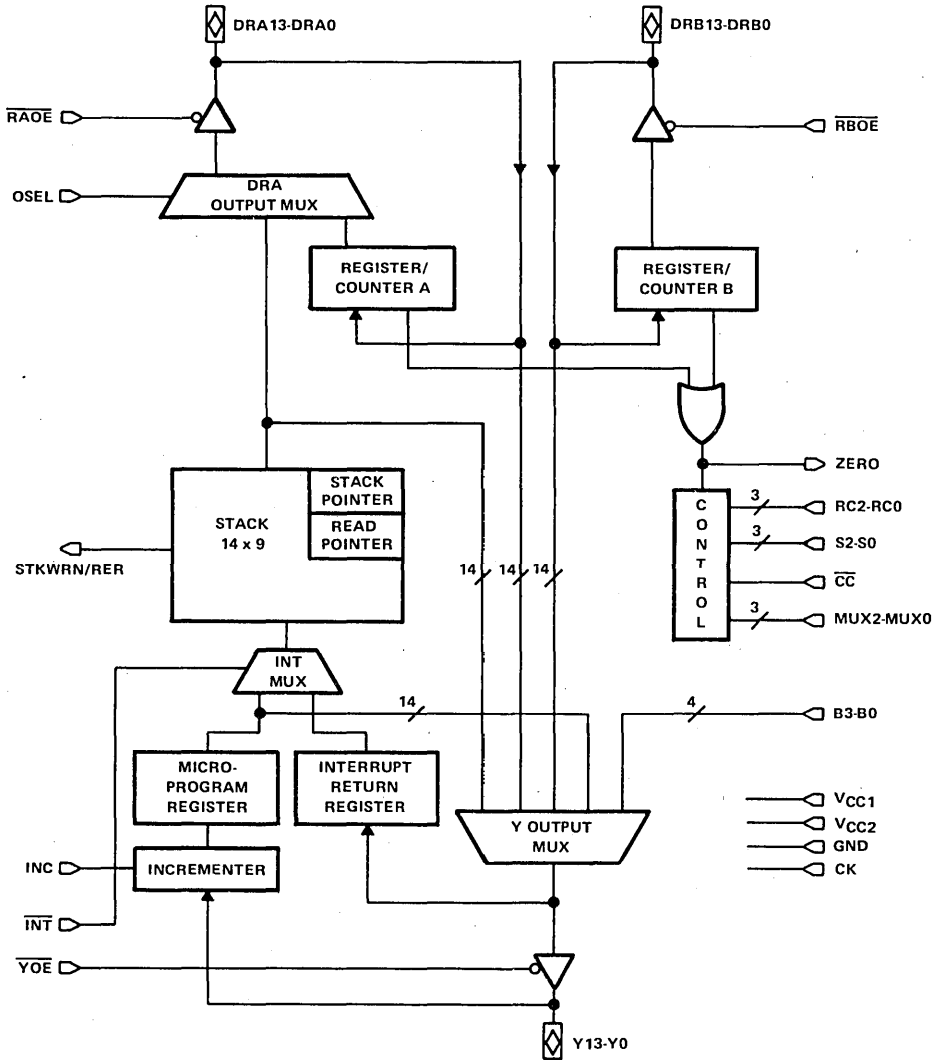
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**SN54AS890, SN74AS890
MICROSEQUENCERS**

functional block diagram



2

LSI Devices

pin descriptions

PIN NAME	I/O	PIN FUNCTION
\overline{RAOE}	In	Enables DRA output, active low
DRA6-DRA0	In/Out	Seven LSBs of the A direct data I/O port
OSEL	In	MUX control for the source to DRA. Low selects RA, high selects stack.
MUX2-MUX0	In	MUX control for Y output bus (see Table 1)
RC2-RC0	In	Register/counter controls (see Table 3)
S2-S0	In	Stack control (see Table 2)
\overline{CC}	In	Condition code
VCC1		5-volt supply for TTL compatible I/O
VCC2		2-volt supply for internal STL
CK	In	Clock
ZERO	Out	Zero detect flag for register A and B
STKWRN/RER	Out	Stack overflow, underflow/read error flag
DRB6-DRB0	In/Out	Seven LSBs of the B direct data I/O port (0 = LSB)
\overline{RBOE}	In	Enables DRB output, active low
DRB13-DRB7	In/Out	Seven MSBs of the B direct data I/O port
INT	In	Active low selects INT RT register to stack
Y13-Y8	In/Out	Six MSBs of bidirectional Y port
GND		Ground
Y7	In/Out	Seventh bit of bidirectional Y port
\overline{YOE}	In	Enables Y output bus, active low
Y6-Y0	In/Out	Seven LSBs of bidirectional Y port (0 = LSB)
INC	In	Incrementer control
DRA13-DRA7	In/Out	Seven MSBs of direct B data I/O port
B3-B0	In	16-way branch inputs on

description (continued)

Two 14-bit loadable registers/counters may be used for temporary storage of data or utilized as down counters for repetitive instructions such as multiplication and division or as loop counters when iterative routines are required.

An additional feature is a 24-bit port that appends four user-definable bits to the DRA or DRB address value for support of 16-way branches for the execution of relative branch addressing schemes.

Y output multiplexer

The Y output multiplexer of the 'AS890 is capable of selecting the next branch address from one of eight locations. Addresses may be sourced from:

1. The top of the 14-bit by 9-word address stack
2. An external input on the DRA port, potentially a pipeline register
3. An external input on the DRB port, potentially a pipeline register
4. Internal register/counter A
5. Internal register/counter B
6. An internal microprogram counter (MPC register)
7. An external input onto the bidirectional Y output port
8. A 16-way branch—4 bits appended to DRA, DRB, register/counter A or register/counter B.

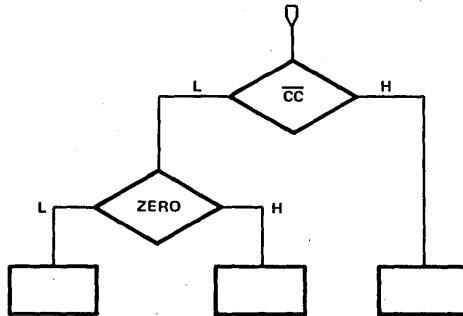
SN54AS890, SN74AS890 MICROSEQUENCERS

The source of the next address is dependent upon the previous state of the microsequencer, the MUX controls (MUX2-MUX0), the condition code (\overline{CC}) input, and the state of an internal status flag (status externally available at the ZERO output) that indicates that one of the on-chip registers is being decremented to zero.

The entire instruction set may be made conditional by manipulation of the condition code (\overline{CC}) input. Allowing the \overline{CC} value to vary as a result of data or status provides for state-dependent or data-dependent branching. Unconditional branches may be achieved by forcing \overline{CC} high when selecting control store addresses. Holding this pin low will provide for conditional or unconditional branches as dictated by the state of the zero-detect flag. The required control signals for selection of the Y output source are listed in Table 1. Note that the dependence of the 'AS890 on two variables for conditional branches and jumps allows a conditional branch or conditional jump to subroutine in any clock cycle. Also note that all multiplexer inputs are overridden when all of the stack control inputs are pulled low. This instruction resets the stack and read pointers to zero and places all lines of the Y output bus at the low level.

TABLE 1. Y OUTPUT CONTROL

MUX CONTROL			RESET*	Y OUTPUT SOURCE		Y OUTPUT SOURCE
MUX2	MUX1	MUX0		$\overline{CC} = L$		$\overline{CC} = H$
			ZERO = L		ZERO = H	
X	X	X	YES	ALL LOW	ALL LOW	ALL LOW
L	L	L	NO	STK	MPC	DRA
L	L	H	NO	STK	MPC	DRB
L	H	L	NO	STK	DRA	MPC
L	H	H	NO	STK	DRB	MPC
H	L	L	NO	DRA	MPC	DRB
H	L	H	NO	DRA' (16-WAY BRANCH)	MPC	DRB' (16-WAY BRANCH)
H	H	L	NO	DRA	STK	MPC
H	H	H	NO	DRB	STK	MPC



H = high level, L = low level, X = irrelevant.

*Reset command is implemented by setting S2-S0 = LLL.

14-bit by 9-word address stack

The positive-edge-triggered 14-bit address stack supplies on-board storage of nine control store addresses that support up to nine nested levels of microsubroutine, looping, and real-time interrupt functions. The stack pointer (SP), which operates as an up-down counter, is updated after the execution of each PUSH operation and before each POP. In a PUSH operation, the address stored in the MPC register is loaded into the stack location addressed by the stack pointer, and the stack pointer is incremented. This address is available at the DRA port by enabling DRA (RAOE low and OSEL high).

A POP operation causes the stack pointer to be decremented on the first rising clock edge following the arrival of the POP instruction at the S2-S0 pins. The value that was indexed by the stack pointer is effectively removed from the top of the stack. All PUSH and POP instructions are conditionally dependent upon the stack control inputs (S2-S0), the condition code (\overline{CC}), the input value, and the zero-detect status. The desired option may be selected using the stack control inputs listed in Table 2.

TABLE 2. STACK CONTROL

STACK CONTROL			STACK OPERATION, $\overline{CC} = L$			
S2	S1	S0	OSEL	ZERO = L	ZERO = H	$\overline{CC} = H$
L	L	L	X	RESET/CLEAR	RESET/CLEAR	RESET/CLEAR
L	L	H	X	CLEAR SP, RP	HOLD	HOLD
L	H	L	X	HOLD	POP	POP
L	H	H	X	POP	HOLD	HOLD
H	L	L	X	HOLD	PUSH	PUSH
H	L	H	X	PUSH	HOLD	HOLD
H	H	L	X	PUSH	HOLD	PUSH
H	H	H	H	READ	READ	READ
H	H	H	L	HOLD	HOLD	HOLD

The read pointer (RP) is a useful tool in debugging microcoded systems. A microprogrammer now has the ability to perform a nondestructive, sequential read of the stack contents from the DRA port. This capability provides the user with a method of backtracking through the address sequence to determine the cause of overflow without affecting program flow, the status of the stack-pointer or the internal data of the stack. Placing a high value on all of the stack inputs (S2-S0) and OSEL places the 'AS890 into the read mode. At each low-to-high clock transition, the value pointed to by the read pointer is available at the DRA port and the read pointer is decremented. Microcode diagnostics are simplified by the ability of the 'AS890 to sequentially dump the contents of its stack. The bottom of the stack is detected by monitoring the STKWWRN/RER (stack warning/read error) pin. A high will appear when the stack contains one word and a READ instruction is applied to the S2-S0 pins. This signifies that the last address has been read. The stack pointer and stack contents are unaffected by the READ operation. Under normal PUSH and POP operations the read pointer is updated with the stack pointer and contains identical information.

The STKWWRN/RER pin alerts the system to a potential stack overflow or underflow condition. STKWWRN/RER becomes active under two additional conditions. If seven of the nine stack locations (0-8) are full (the stack pointer is at 7) and a PUSH occurs, the STKWWRN/RER pin will produce a high-level signal to warn that the stack is approaching its capacity, and will be full after one more PUSH. Knowledge that overflow potential exists allows bit-slice-based systems to continuously process real-time interrupt vectors. This signal will remain high, if HOLD, PUSH, or POP instructions occur, until the stack pointer is decremented to 7.

The user may be protected from attempting to POP an empty stack by monitoring STKWWRN/RER before POP operations. A high level at this pin signifies that the last address has been removed from the stack (SP=0). This condition remains until an address is pushed onto the stack and the stack pointer is incremented to one.

Clearing the stack and read pointer is accomplished by placing low levels onto the stack control lines (S2-S0). This function overrides all of the Y output MUX controls and places the Y bus into a low state.

2
LSI Devices

register/counters

Two loadable 14-bit registers extend the looping and branching capabilities. Addresses may be loaded directly into register/counter A (RA) and register/counter B (RB) through the direct data ports DRA13-DRA0 and DRB13-DRB0. The values stored in these registers may either be held, decremented, or read as a result of the register control inputs (RC2-RC0), \overline{RAOE} , and \overline{RBOE} . All combinations of these functions are supported with the exception of a simultaneous decrement of both registers. Generation of iteration routines may be accomplished by loading RA and/or RB and operating them as a down counter. Loop termination is acknowledged by the ZERO output going high to indicate that a register contains a binary one and that a decrement is about to take place. Because of this facility, a "decrement and branch on loop" termination may be executed in the same clock cycle.

The contents of RA are accessible to the DRA port when OSEL is low and the output bus is enabled by \overline{RAOE} being low. Data from RB is available when DRB is enabled by \overline{RBOE} being low. Note that control of the registers is maintained while an external value is active on the DRA and DRB ports. A value being directed from the DRA and DRB buses to the output will not inhibit the decrement operation.

Register/counter controls are listed in Table 3.

TABLE 3. REGISTER CONTROL

RC2	RC1	RC0	REG A	REG B
L	L	L	HOLD	HOLD
L	L	H	DEC	HOLD
L	H	L	LOAD	HOLD
L	H	H	DEC	LOAD
H	L	L	LOAD	LOAD
H	L	H	HOLD	DEC
H	H	L	HOLD	LOAD
H	H	H	LOAD	DEC

microprogram register and increment

The microprogram register (MPC) and the incrementer (INC) provide the means for generating the next microprogram address for sequential addressing operations. The MPC may be loaded with either the outgoing address on the Y bus or may receive an external address for processing interrupt vectors.

The current address on the Y bus is passed to the MPC at each rising clock edge, either unaltered (INC low) for repeating statements, or incremented by one (INC high) for addressing sequential control store locations.

The MPC may also be externally loaded for subroutine and interrupt functions. Taking \overline{YOE} high and forcing the new address onto the bidirectional Y bus loads the MPC with the new address at the positive clock edge. This value may also be incremented prior to storage in the MPC for sequential addressing of subroutines or interrupt routines.

interrupts

Real-time vectored interrupt routines are supported for those applications where polling would impede system throughput. Any instruction, including PUSHes and POPs, may be interrupted. To process an interrupt, the following procedure should be followed:

1. The bidirectional Y bus is placed into the high-impedance state by forcing \overline{YOE} high.
2. The interrupt entry point vector is then forced onto the Y bus and incremented to become the second microinstruction of the interrupt routine. This is accomplished by making INC high.

3. At the following clock edge, the second microaddress is stored in the MPC and the interrupted address will be stored in the INT RT register which always contains the outgoing value on the Y bus. This edge also causes the processor to begin execution of the first instruction of the interrupt routine. This first instruction must PUSH the address stored in the INT RT register onto the stack so that the proper return linkage is maintained. This is accomplished by making $\overline{\text{INT}}$ low and performing a PUSH. If this instruction were to be interrupted, the process would be repeated and the proper return linkage preserved.

control inputs

A listing of the response of internal elements to various control inputs is given in Table 4.

TABLE 4. RESPONSE TO CONTROL INPUTS

PIN NAME	LOGIC LEVEL	
	HIGH	LOW
RAOE	DRA output in high-Z state	DRA output is active
RBOE	DRB output in high-Z state	DRB output is active
YOE	Y output in high-Z state	Y output is active
$\overline{\text{INT}}$	MPC to stack	INT RT register to stack
OSEL	Stack to DRA buffer input	RA to DRA buffer input
INC	Adds one to Y output and stores in MPC	Passes Y output to MPC unaltered
MUX2-MUX0	Table 1	Table 1
S2-S0	Table 2	Table 2
RC2-RC0	Table 3	Table 3

instruction set

Sixty-four microsequencing instructions enable the 'AS890 to generate micro-addresses for up to 16,384 locations. Any instruction can be made conditional depending upon the value of the externally applied condition code (CC) and the value stored in either of the internal register/counters.

The required signals for selection of the Y output source were listed in Table 1. Suggested methods for implementing a few commonly used instructions are given in Table 5 and flowcharts showing execution examples are illustrated in Figure 1.

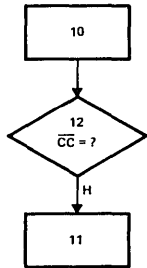
It should be noted that the term jump refers to a subroutine call that must be accompanied by a return instruction. The term branch implies that a deviation from the program flow is accomplished but no return is required.

SN54AS890, SN74AS890 MICROSEQUENCERS

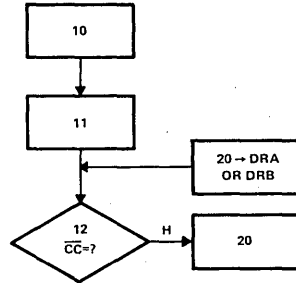
TABLE 5. SUGGESTED CODING FOR REPRESENTATIVE INSTRUCTIONS

FUNCTION	MNEMONIC	MUX2	MUX1	MUX0	S2	S1	S0	CC	FIGURE
Continue	CONT	X	H	X	H	H	H	H	1(a)
Unconditional branch	BR	L	L	X	H	H	H	H	1(b)
Conditional branch	CBR	H	H	X	H	H	H	V	1(c)
Three-way branch	BR2W	H	L	L	H	H	H	V	1(d)
Conditional loop on stack	LOOPS	L	L	X	L	H	L	L	1(e)
Repeat	REPEAT	L	L	X	H	H	H	L	1(f)
Loop on stack with exit	LSWE	L	L	X	L	H	L	V	1(g)
Conditional jump to subroutine	CJSR	H	H	X	H	L	H	V	1(h)
Jump to subroutine	JSR	L	L	X	H	L	H	H	1(i)
Two-way jump to subroutine	JSR2W	H	L	L	H	H	L	V	1(j)
Repeat until	UNTIL	L	H	X	L	H	L	V	1(k)
Return from subroutine	RTS	L	H	X	L	H	H	L	1(l)
Conditional return from subroutine	CRTS	L	H	X	L	H	H	V	1(m)
Conditional return from subroutine or branch	CRTSB	L	H	X	L	H	H	V	1(n)
Conditional branch and PUSH	CBRP	H	H	X	H	L	H	V	1(o)
Conditional branch and POP	CBRPO	H	H	X	L	H	H	V	1(p)
PUSH and continue	PUSH	L	H	X	H	L	L	H	1(q)
POP and continue	POP	X	H	X	L	H	L	H	1(r)
Exit from loop	EXITLP	L	L	X	L	H	L	V	1(s)
Reset and clear stack/read pointer	RESET	X	X	X	L	L	L	X	1(t)
32-way branch	BR32W	H	L	H	H	H	H	V	1(u)
Execute n times	NEX	L	L	X	L	H	L	L	1(v)

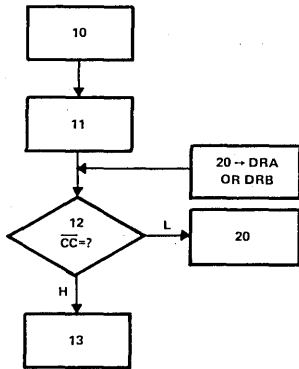
H = high level, L = low level, X = irrelevant, V = varies (condition code value is dependent upon machine and data status and will vary accordingly).



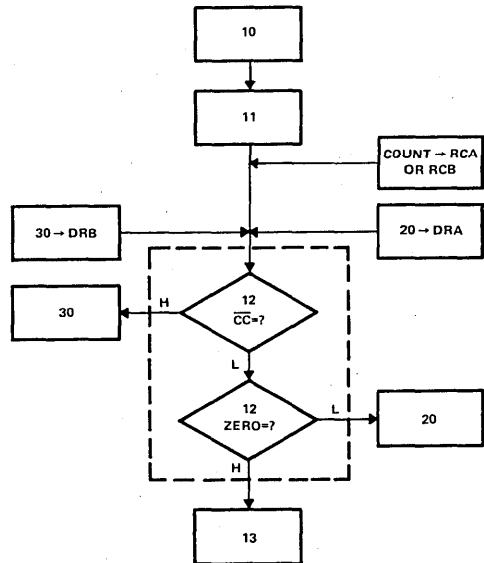
(a) CONTINUE
(CC FORCED)



(b) UNCONDITIONAL BRANCH
(CC FORCED)



(c) CONDITIONAL BRANCH
(DEC DISABLED)



(d) THREE-WAY BRANCH (DEC ENABLED)¹

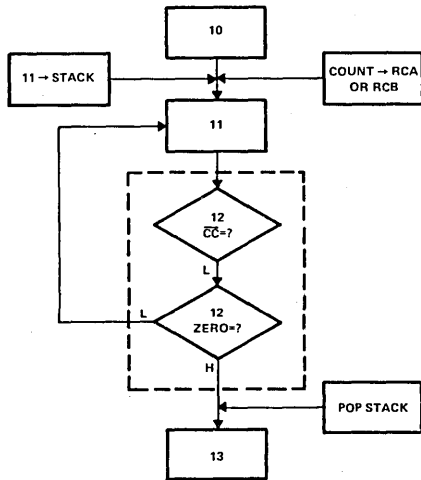
2

LSI Devices

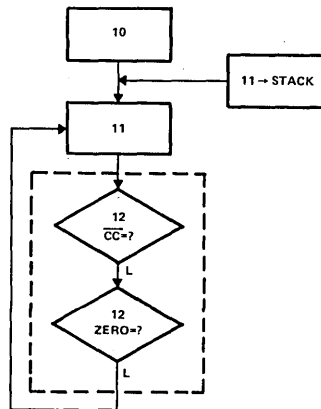
NOTE 1: \overline{CC} and ZERO are completed in the same clock cycle.

FIGURE 1. INSTRUCTION SET FLOWCHARTS

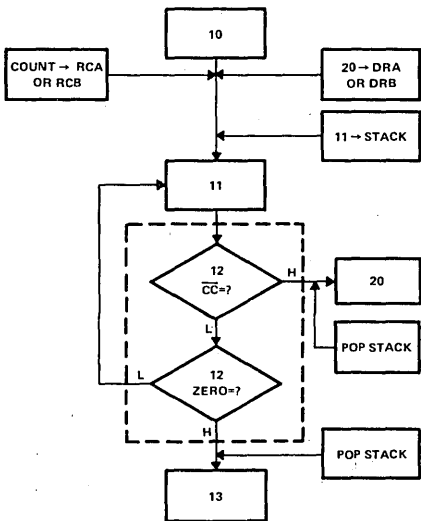
**SN54AS890, SN74AS890
MICROSEQUENCERS**



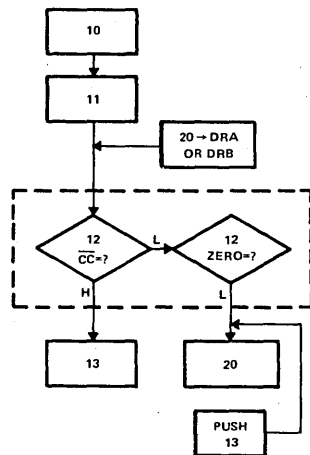
(e) CONDITIONAL LOOP ON STACK
(\overline{CC} FORCED, DEC ENABLED)¹



(f) REPEAT (\overline{CC} FORCED, DEC DISABLED)¹



(g) CONDITIONAL LOOP ON STACK
WITH EXIT (DEC ENABLED)¹



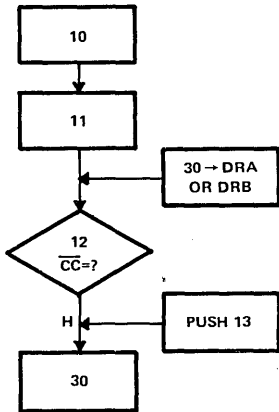
(h) CONDITIONAL JUMP TO SUBROUTINE
(DEC DISABLED)¹

NOTE 1: \overline{CC} and ZERO are completed in the same clock cycle.

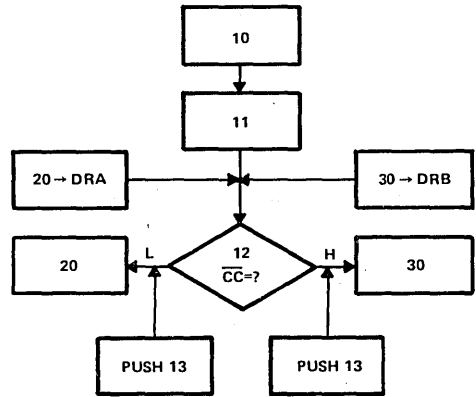
FIGURE 1. INSTRUCTION SET FLOWCHARTS (continued)

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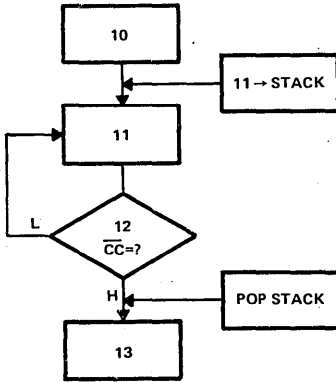
LSI Devices



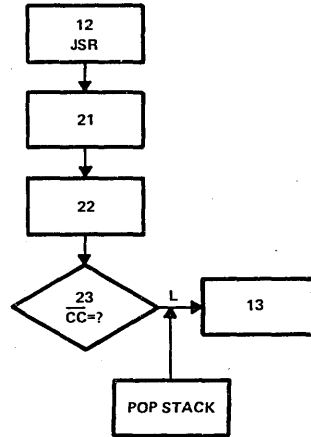
(i) JUMP TO SUBROUTINE
(\overline{CC} FORCED)



(j) TWO-WAY JUMP TO SUBROUTINE
(DEC DISABLED)



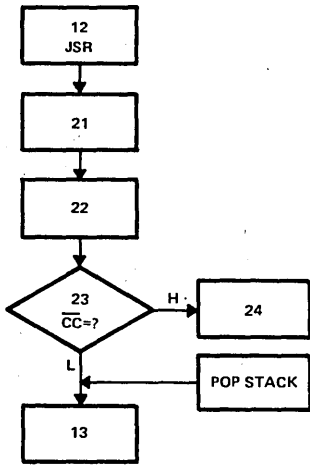
(k) REPEAT UNTIL
(DEC DISABLED)



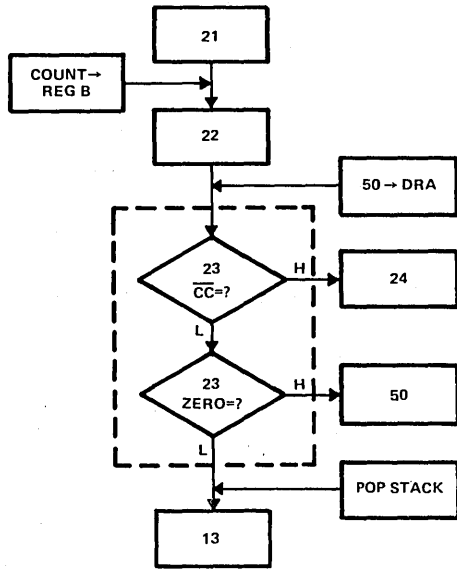
(l) RETURN FROM SUBROUTINE
(\overline{CC} FORCED, DEC DISABLED)

FIGURE 1. INSTRUCTION SET FLOWCHARTS (continued)

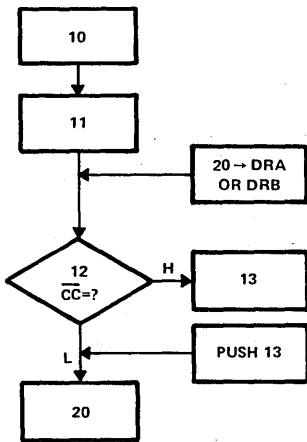
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LSI Devices



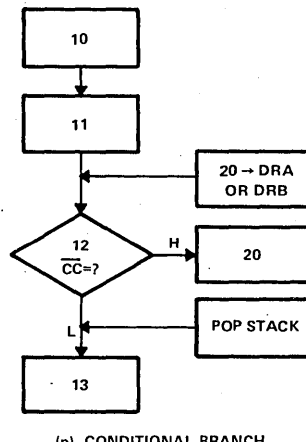
(m) CONDITIONAL RETURN FROM SUBROUTINE (DEC DISABLED)



(n) CONDITIONAL RETURN FROM SUBROUTINE OR BRANCH (DEC ENABLED)¹



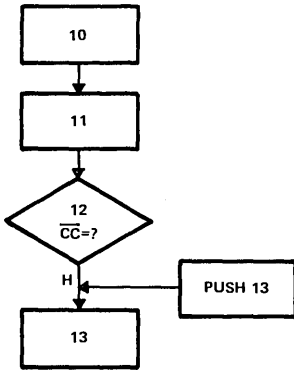
(o) CONDITIONAL BRANCH AND PUSH (DEC DISABLED)



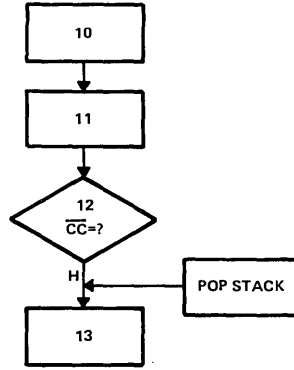
(p) CONDITIONAL BRANCH AND POP (DEC DISABLED)

NOTE 1: \overline{CC} and ZERO are completed in the same clock cycle.

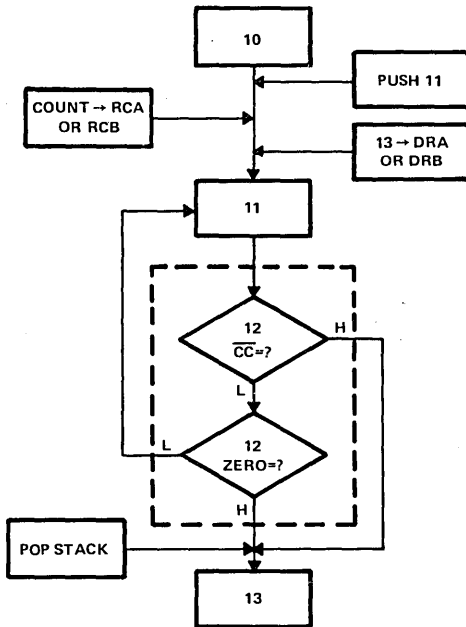
FIGURE 1. INSTRUCTION SET FLOWCHARTS (continued)



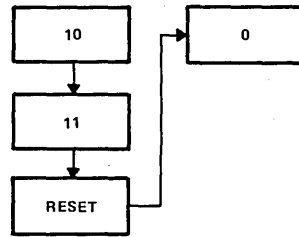
(q) PUSH AND CONTINUE
(\overline{CC} FORCED)



(r) POP AND CONTINUE
(\overline{CC} FORCED)



(s) EXIT FROM LOOP
(DEC ENABLED)¹

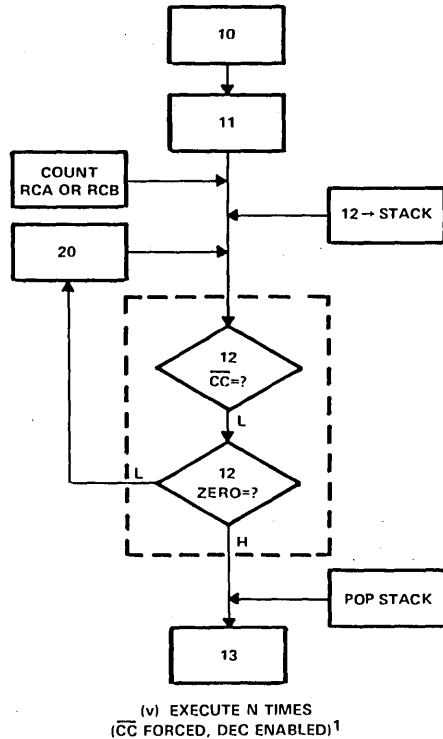
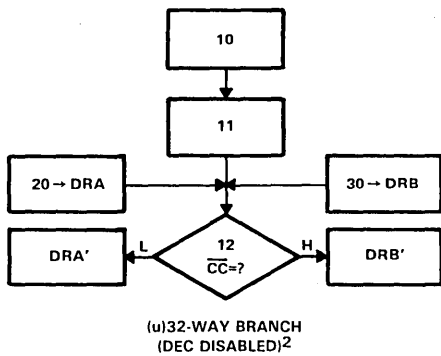


(t) RESET AND CLEAR

NOTE 1: \overline{CC} and ZERO are completed in the same clock cycle.

FIGURE 1. INSTRUCTION SET FLOWCHARTS (continued)

2
LSI Devices



NOTES: 1. \overline{CC} and ZERO are completed in the same clock cycle.

2. The least significant four bits, DRA and DRB, will be stripped off and four new bits appended to them from the B3-B0 port.

FIGURE 1. INSTRUCTION SET FLOWCHARTS (concluded)

SN54AS890, SN74AS890 MICROSEQUENCERS

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage, V_{CC1}	7 V
Supply voltage, V_{CC2}	3 V
Input voltage: All inputs	7 V
I/O ports	5.5 V
Operating case temperature range, SN54AS890	-55°C to 125°C
Operating free-air temperature range, SN74AS890	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54AS890			SN74AS890			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX		
V_{CC1}	I/O supply voltage	4.5	5	5.5	4.5	5	5.5	V	
V_{CC2}	STL internal logic supply voltage	1.9	2	2.1	1.9	2	2.1	V	
V_{IH}	High-level input voltage	2			2			V	
V_{IL}	Low-level input voltage				0.8			V	
I_{OH}	High-level output current				-1			mA	
I_{OL}	Low-level output current	All outputs except Y13-Y0		8		8		mA	
		Y13-Y0		12		12			
T_C	Operating case temperature	-55			125			°C	
T_A	Operating free air temperature				0			70	°C

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS890			SN74AS890			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		$V_{CC1} = 4.5$ V,	$I_I = -18$ mA	-1.2			-1.2			V
V_{OH}		$V_{CC1} = 4.5$ V to 5.5 V,	$I_{OH} = -0.4$ mA	$V_{CC}-2$			$V_{CC}-2$			V
		$V_{CC1} = 4.5$ V,	$I_{OH} = -1$ mA	2.4			3.4			
		$V_{CC1} = 4.5$ V,	$I_{OH} = -2.6$ mA				2.4			
V_{OL}	All outputs except Y13-Y0	$V_{CC1} = 4.5$ V,	$I_{OL} = 8$ mA	0.5			0.5			V
	Y13-Y0	$V_{CC1} = 4.5$ V,	$I_{OL} = 12$ mA	0.5			0.5			
I_I	Inputs	$V_{CC1} = 5.5$ V,	$V_I = 7$ V	0.1			0.1			mA
	I/O ports	$V_{CC1} = 5.5$ V,	$V_I = 5.5$ V	0.1			0.1			
I_{IH}	Inputs	$V_{CC1} = 5.5$ V,	$V_I = 2.7$ V	20			20			µA
	I/O ports‡			40			40			
I_{IL}^{\ddagger}		$V_{CC1} = 5.5$ V,	$V_I = 0.4$ V	-0.4			-0.4			mA
I_O^{\S}		$V_{CC1} = 5.5$ V,	$V_O = 2.25$ V	-30	-112	-30	-112	mA		
I_{CC1}		$V_{CC1} = 5.5$ V		185			178			mA
I_{CC2}		$V_{CC2} = 2.1$ V		420			400			mA

†All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

‡For I/O ports, the parameters I_{IH} and I_{IL} include output current I_{OZL} and I_{OZL} , respectively.

§The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS} .

2

LSI Devices

SN54AS890 MICROSEQUENCERS

SN54AS890 maximum switching characteristics: $V_{CC1} = 4.5\text{ V to }5.5\text{ V}$, $V_{CC2} = 1.9\text{ V to }2.1\text{ V}$, $T_C = 55^\circ\text{C to }125^\circ\text{C}$ (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)					UNIT	
		Y	ZERO	DRA	DRB	STKWRN		
t_{pd}	\overline{CC}	32					ns	
	CK	32		30	30	30		
		53 [†]	42 [†]					
	DRA13-DRA0	16						ns
	DRB13-DRB0	16						
	MUX2-MUX0	36						
	RC2-RC0	32	14					
	S2-S0	32						
B2-B0	22							
OSEL			24			ns		
\overline{YOE}	16							
\overline{RAOE}			16					
t_{dis}	\overline{RBOE}			16			ns	
	\overline{YOE}	16						

[†] Decrementing Register/Counter A or B and sensing a zero.

NOTE 2: Load circuit and voltage waveforms are shown in Section 1

SN54AS890 setup and hold times

PARAMETER	FROM	TO (DESTINATION)	MIN	MAX	UNIT
t_{su}	\overline{CC}	Stack	10		ns
	DRA13-DRA0	RCA, INT RT	5		
	DRB13-DRB0	RCB, INT RT	5		
	INC	MPC	10		
	INT	Stack	10		
		Stack	16		
	RC2-RC0	RCA, RCB	10		
		INT RT	14		
	S2-S0	Stack	10		
		INT RT	10		
	MUX2-MUX0	INT RT	14		
B3-B0	INT RT	14			
Y13-Y0	MPC	12			
t_h	Any Input	Any Destination	2		

SN54AS890 minimum clock requirements (see Note 3)

PARAMETER	MIN	MAX	UNIT
$t_{wL}(CK)$ Pulse duration, clock low	10		ns
$t_{wH}(CK)$ Pulse duration, clock high	20		
$t_c(CK)$ Clock cycle time	55 [†]	45	

[†] Decrementing Register/Counter A or B and sensing a zero.

NOTE 3: The total clock period of clock high and clock low must not be less than clock cycle time. The minimum pulse durations specified are only for clock high or clock low, but not for both simultaneously.

SN74AS890 maximum switching characteristics: $V_{CC1} = 4.5\text{ V to }5.5\text{ V}$, $V_{CC2} = 1.9\text{ V to }2.1\text{ V}$, $T_A = 0^\circ\text{C to }70^\circ\text{C}$ (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)					UNIT
		Y	ZERO	DRA	DRB	STKWRN	
t_{pd}	\overline{CC}	29					ns
	CK	29		29	29	29	
		50 [†]	39 [†]				
	DRA13-DRA0	15					
	DRB13-DRB0	15					
	MUX2-MUX0	35					
	RC2-RC0	30	13				
	S2-S0	28					
B2-B0	20						
OSEL			18				
t_{en}	YOE	15					ns
	RAOE			15			
	RBOE				15		
t_{dis}	YOE	16					ns
	RAOE			16			
	RBOE				16		

[†] Decrementing Register/Counter A or B and sensing a zero.

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

SN74AS890 setup and hold times

PARAMETER	FROM	TO (DESTINATION)	MIN	MAX	UNIT
t_{su}	\overline{CC}	Stack	10		ns
	DRA13-DRA0	RCA, INT RT	5		
	DRB13-DRB0	RCB, INT RT	5		
	INC	MPC	10		
	INT	Stack	10		
	RC2-RC0	Stack	14		
		RCA, RCB	10		
		INT RT	12		
	S2-S0	Any Destination	10		
	MUX2-MUX0	INT RT	12		
	B3-B0	INT RT	14		
Y13-Y0	MPC	10			
t_h	Any Input	Any Destination	2		

SN74AS890 minimum clock requirements (see Note 3)

PARAMETER	MIN	MAX	UNIT
$t_{wL}(CK)$ Pulse duration, clock low	10		ns
$t_{wH}(CK)$ Pulse duration, clock high	20		
$t_c(CK)$ Clock cycle time	50 [†]		
	36		

[†] Decrementing Register/Counter A or B and sensing a zero.

NOTE 3: The total clock period of clock high and clock low must not be less than clock cycle time. The minimum pulse durations specified are only for clock high or clock low, but not for both simultaneously.

2
LSI Devices

SN74AS890-1 MICROSEQUENCERS

SN74AS890-1 maximum switching characteristics: $V_{CC1} = 4.5\text{ V to }5.5\text{ V}$, $V_{CC2} = 1.9\text{ V to }2.1\text{ V}$,
 $T_A = 0^\circ\text{C to }70^\circ\text{C}$ (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)					UNIT
		Y	ZERO	DRA	DRB	STKWRN	
t_{pd}	CC	25					ns
	CK	25		25	25	25	
		42 [†]	34 [†]				
	DRA13-DRA0	14					
	DRB13-DRB0	14					
	MUX2-MUX0	31					
	RC2-RC0	26	12				
	S2-S0	25					
B2-B0	19					ns	
OSEL			17				
YOE	15						
t_{en}	RAOE			15			ns
	RBOE				15		
t_{dis}	YOE	16					ns
	RAOE			16			
	RBOE				16		

[†] Decrementing Register/Counter A or B and sensing a zero.

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

SN74AS890-1 setup and hold times

PARAMETER	FROM	TO (DESTINATION)	MIN	MAX	UNIT
t_{su}	CC	Stack	10		ns
	DRA13-DRA0	RCA, INT RT	5		
	DRB13-DRB0	RCB, INT RT	5		
	INC	MPC	10		
	INT	Stack	10		
		Stack	14		
	RC2-RC0	RCA, RCB	10		
		INT RT	12		
	S2-S0	Any Destination	10		
	MUX2-MUX0	INT RT	12		
	B3-B0	INT RT	14		
Y13-Y0	MPC	10		ns	
t_h	Any Input	Any Destination	2		

SN74AS890-1 minimum clock requirements (see Note 3)

PARAMETER	MIN	MAX	UNIT
$t_{wL}(CK)$ Pulse duration, clock low	10		ns
$t_{wH}(CK)$ Pulse duration, clock high	20		
$t_c(CK)$ Clock cycle time	42 [†]		
	34		

[†] Decrementing Register/Counter A or B and sensing a zero.

NOTE 3: The total clock period of clock high and clock low must not be less than clock cycle time. The minimum pulse durations specified are only for clock high or clock low, but not for both simultaneously.

SN54AS895, SN74AS895 8-BIT MEMORY ADDRESS GENERATORS

NOVEMBER 1985—REVISED APRIL 1986

- STL-AS Technology
- Parallel 8-Bit ALU with Expansion Inputs and Outputs
- 13 Arithmetic and Logic Functions
- 8 Conditional Shifts (Single and Double Length)
- 9 Instructions that Manipulate Bytes
- 4 Instructions that Manipulate Bits
- Add and Subtract Immediate Instructions
- Absolute Value Instruction
- Signed Magnitude to/from Two's Complement Conversion
- Single- and Double-Length Normalize
- Select Functions
- Signed and Unsigned Divides with Overflow Detection; Input does not Need to be Prescaled
- Signed, Mixed, and Unsigned Multiplies
- Three-Operand, 16-Word Register File
- Full Carry Look Ahead Support
- Sign, Carry Out, Overflow, and Zero-Detect Status Capabilities
- Excess-3 BCD Arithmetic
- MQ Register is Externally Available through the DB Port
- Internal Shift Multiplexers that Eliminate the Need for External Shift Control Parts
- ALU Bypass Path to Increase Speeds of Multiply, Divide, and Normalize Instructions and to Provide New Instructions such as Bit Set, Bit Reset, Bit Test, Byte Subtract, Byte Add, and Byte Logical
- 3-Operand Register Files to Allow an Operation and a Move Instruction to be Combined
- Byte Select Controlled by External 3-State Buffers that may be Eliminated if Bit and Byte Manipulation are not Needed
- Bit and Byte Masks that are Shared with Register Address Fields to Minimize Control Store Word Width
- 3 Data Input/Output Paths to Maximize Data Throughput

description

These 8-bit Advanced Schottky TTL integrated circuits are designed to implement high performance digital computers or controllers. An architecture and instruction set has been chosen that supports a fast system clock, a narrow micro-code word width, and a high system throughput. The powerful instruction set allows high-speed system architecture to be implemented and also allows an existing system's performance to be upgraded while protecting software investments. These processors are designed to be cascadable to any word width 16 bits or greater.

The only difference between the 'AS888 Bit-Slice Processor and the 'AS895 Memory Address Generators is the function of the DB port. The 'AS888 DB port outputs the register file. The 'AS895 DB port can be used to read the MQ register result during the same clock cycle that the ALU result is available at the Y port.

The SN54AS895 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AS895 and SN74AS895-1 are characterized for operation from 0°C to 70°C .

Package options include both plastic and ceramic chip carriers in addition to a 68-pin grid array ceramic package.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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INSTRUMENTS

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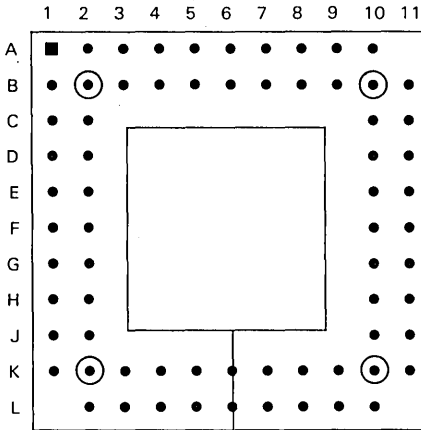
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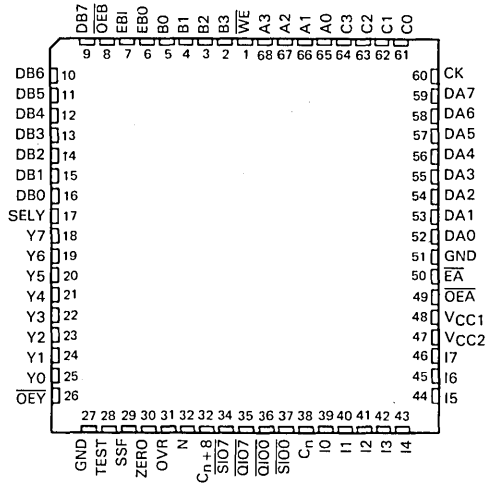
LSI Devices

SN54AS895, SN74AS895 8-BIT MEMORY ADDRESS GENERATORS

SN54AS895, SN74AS895 . . . GB PACKAGE
(TOP VIEW)



SN54AS895 . . . FK PACKAGE
SN74AS895 . . . FN PACKAGE
(TOP VIEW)



GB PACKAGE PIN ASSIGNMENTS

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
A-2	C_n	B-9	\overline{OEY}	F-10	Y3	K-4	C2
A-3	$\overline{SIO0}$	B-10	Y0	F-11	DB2	K-5	A0
A-4	$\overline{QIO0}$	B-11	Y1	G-1	DA2	K-6	A3
A-5	$\overline{QIO7}$	C-1	I5	G-2	DA0	K-7	\overline{WE}
A-6	C_n+8	C-2	V_{CC2}	G-10	DB0	K-8	DB7
A-7	$\overline{G/N}$	C-10	Y4	G-11	DB3	K-9	\overline{OEB}
A-8	$\overline{P/OVR}$	C-11	Y6	H-1	DA3	K-10	EBO
A-9	ZERO	D-1	I6	H-2	DA1	K-11	EB1
A-10	PPP	D-2	V_{CC1}	H-10	DB6	L-2	CK
B-1	I2	D-10	Y5	H-11	DB4	L-3	C1
B-2	I3	D-11	Y7	J-1	DA4	L-4	C3
B-3	I1	E-1	I7	J-2	DA5	L-5	A1
B-4	I0	E-2	\overline{OEA}	J-10	SELY	L-6	A2
B-5	I4	E-10	Y2	J-11	DB5	L-7	B3
B-6	$\overline{SIO7}$	E-11	DB1	K-1	DA6	L-8	B2
B-7	SSF	F-1	\overline{EA}	K-2	DA7	L-9	B1
B-8		F-2	GND	K-3	CO	L-10	B0

2

LSI Devices

SN54AS895, SN74AS895
8-BIT MEMORY ADDRESS GENERATORS

PIN GRID ARRAY	CHIP CARRIER	NAME	I/O	DESCRIPTION
A-10	28	PPP	I	Package position pin. Tri-level input used to define package significance during instruction execution. Leave open for intermediate positions, tie to V _{CC} for most significant package, and tie to GND for least significant package.
B-7	29	SSF	I/O	Special shift function. Used to transfer required information between packages during special instruction execution.
A-9	30	ZERO	I/O	Device zero detection, open collector. Input during certain special instructions.
A-8	31	\overline{P}/OVR	O	ALU propagate/instruction overflow for most significant package, low active.
A-7	32	\overline{G}/N	O	ALU generate/negative result for most significant package, low active.
A-6	33	C _{n+8}	O	ALU ripple carry output.
B-6	34	$\overline{\text{S}}\text{I}07$	I/O	Bidirectional shift pin, low active.
A-5	35	$\overline{\text{Q}}\text{I}07$	I/O	
A-4	36	$\overline{\text{Q}}\text{I}00$	I/O	
A-3	37	$\overline{\text{S}}\text{I}00$	I/O	
A-2	38	C _n	I	ALU carry input.
B-4	39	I0	I	Instruction input.
B-3	40	I1	I	
B-1	41	I2	I	
B-2	42	I3	I	
B-5	43	I4	I	
C-1	44	I5	I	
D-1	45	I6	I	
E-1	46	I7	I	
C-2	47	V _{CC2}		Low voltage power supply (2 V).
D-2	48	V _{CC1}		I/O interface supply voltage (5 V).
E-2	49	$\overline{\text{O}}\text{E}\text{A}$	I	DA bus enable, low active.
F-1	50	$\overline{\text{E}}\text{A}$	I	ALU input operand select. High state selects external DA bus and low state selects register file.
F-2	51	GND		Ground pin.
G-2	52	DA0	I/O	A port data bus. Outputs register file data ($\overline{\text{E}}\text{A} = 0$) or inputs external data ($\overline{\text{E}}\text{A} = 1$).
H-2	53	DA1	I/O	
G-1	54	DA2	I/O	
H-1	55	DA3	I/O	
J-1	56	DA4	I/O	
J-2	57	DA5	I/O	
K-1	58	DA6	I/O	
K-2	59	DA7	I/O	
L-2	60	CK	I	Clocks all synchronous registers on positive edge.
K-3	61	C0	I	Register file write address select.
L-3	62	C1	I	
K-4	63	C2	I	
L-4	64	C3	I	
K-5	65	A0	I	Register file A port read address select.
L-5	66	A1	I	
L-6	67	A2	I	
K-6	68	A3	I	

2

LSI Devices



SN54AS895, SN74AS895
8-BIT MEMORY ADDRESS GENERATORS

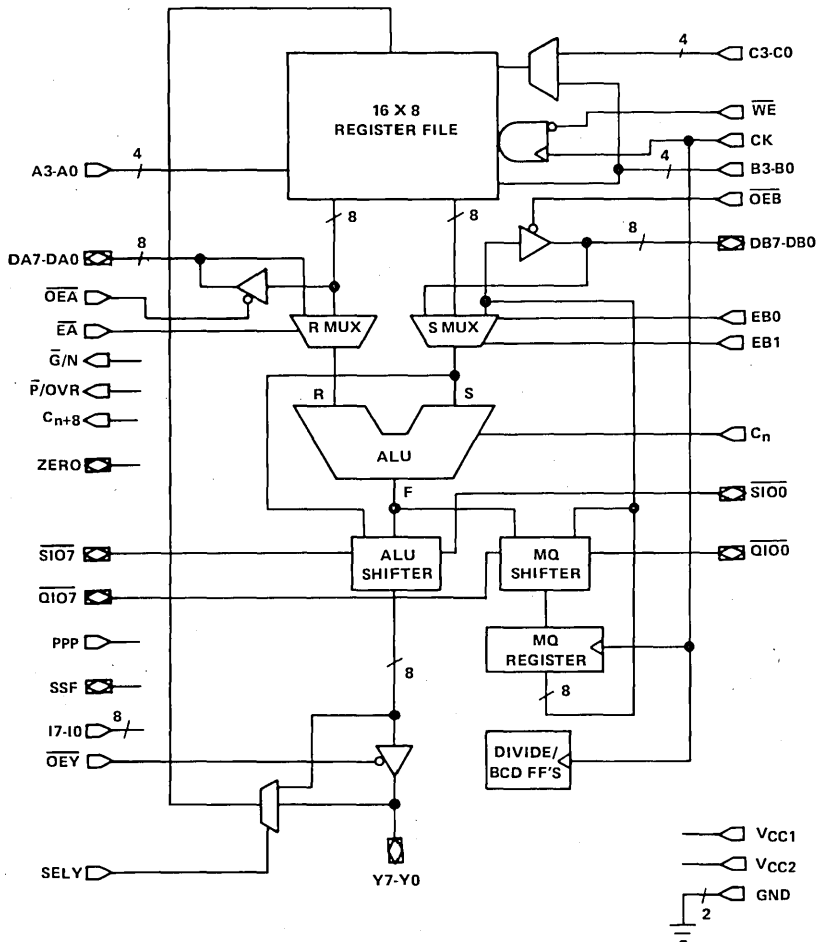
PIN GRID ARRAY	CHIP CARRIER	NAME	I/O	DESCRIPTION
K-7	1	WE	I	Register file (RF) write enable. Data is written into RF when WE is low and a low-to-high clock transition occurs. RF write is inhibited when WE is high.
L-7	2	B3	I	Register file B port read address select. (0 = LSB).
L-8	3	B2	I	
L-9	4	B1	I	
L-10	5	B0	I	
K-10	6	EBO	I	ALU input operand select. EBO and EB1 selects the source of data that the S multiplexer provides for the S bus. Independent control of the DB bus and data path selection allow the user to isolate the DB bus while the ALU continues to process data.
K-11	7	EB1	I	
K-9	8	OE \overline{B}	I	DB bus enable, low active.
K-8	9	DB7	I/O	B port data bus. Outputs MQ register data ($\overline{OE\overline{B}}$ = 0) or used to input external data ($\overline{OE\overline{B}}$ = 1), (0 = LSB).
H-10	10	DB6	I/O	
J-11	11	DB5	I/O	
H-11	12	DB4	I/O	
G-11	13	DB3	I/O	
F-11	14	DB2	I/O	
E-11	15	DB1	I/O	
G-10	16	DB0	I/O	
J-10	17	SELY	I	Y bus select, high active.
D-11	18	Y7	I/O	Y port data bus. Outputs instruction results ($\overline{OE\overline{Y}}$ = 0) or used to put external data into register file ($\overline{OE\overline{Y}}$ = 1).
C-11	19	Y6	I/O	
D-10	20	Y5	I/O	
C-10	21	Y4	I/O	
F-10	22	Y3	I/O	
E-10	23	Y2	I/O	
B-11	24	Y1	I/O	
B-10	25	Y0	I/O	
B-9	26	OE \overline{Y}	I	Y bus output enable, low active.
F-2	27	GND		Ground pin

2

LSI Devices

SN54AS895, SN74AS895
8-BIT MEMORY ADDRESS GENERATORS

functional block diagram



2

LSI Devices

SN54AS895, SN74AS895 8-BIT MEMORY ADDRESS GENERATORS

architectural elements

3-port register file

Working registers consist of 128 storage elements organized into sixteen 8-bit words. These storage elements appear to the user as 16 positive edge-triggered registers. The three port addresses, one write (C) and two reads (A and B), are completely independent of each other to implement a 3-operand register file. Data is written into the register file when \overline{WE} is low and a low-to-high clock transition occurs. The ADD and SUBTRACT immediate instructions require only one source operand. The B address is used as the source address, and the bits of the A address are used to provide a constant field. The SET, RESET, and TEST BIT instructions use the B addressed register as both the source and destination register while the A and C addresses are used as masks. These instructions are explained in more detail in the instruction section.

S multiplexer

The S multiplexer selects the ALU operand, as follows:

EB1	EB0	S bus
Low	Low	RF data
Low	High	MQ data
High	Low	DB data
High	High	MQ data

DB port

The 8-bit bidirectional DB port inputs external data to the ALU or outputs the MQ register. If \overline{OEB} is low, the DB bus is active; if \overline{OEB} is high, the DB bus is in the high impedance state. Notice that the DB port may be isolated at the same time that MQ register data is passed to the ALU.

R multiplexer

The R multiplexer selects the other operand of the ALU. Except for those instructions that require constants or masks, the R bus will contain DA if \overline{EA} is high or the RF data pointed to by A if \overline{EA} is low.

DA port

The 8-bit bidirectional DA port inputs external data to the ALU or outputs the register file. If \overline{OEA} is low, the DA bus is active; if \overline{OEA} is high, the DA bus is in the high-impedance state. Notice that the DA bus may be isolated while register file data is passed to the ALU.

ALU

The shift instructions are summarized in Table 4 and illustrated in Figure 2. The ALU can perform seven arithmetic and six logical instructions on two 8-bit operands. It also supports multiplication, division, normalization, bit set, reset, test, byte operations, and excess-3 BCD arithmetic. These source operands are the outputs of the S and R multiplexers.

ALU and MQ shifters

ALU and MQ shifters perform all of the shift, multiply, divide, and normalize functions. Table 4 shows the value of the $\overline{SIO7}$ and $\overline{QIO7}$ pins of the most significant package. The standard shifts may be made into conditional shifts and the serial data may be input or output with the aid of two three-state gates. These capabilities are discussed further in the arithmetic and logic section.

MQ register

The multiplier-quotient (MQ) register has specific functions in multiplication, division, and normalization. This register may also be used as a temporary storage register. The MQ register may be loaded if the instruction code on pins I7-I0 is E1-E7 or E9-EE (See Table 1).

Y bus

The Y bus contains the output of the ALU shifter if \overline{OEY} is low and is a high impedance input if \overline{OEY} is high. SELY must be low to pass the internal ALU shift bus and must be high to pass the external Y bus to the register file.

status

Four status pins are available on the most significant package, overflow (OVR), sign (N), carry out ($C_n + 8$), and zero (ZERO). The $C_n + 8$ line signifies the ALU result while OVR, ZERO, and N refer the status after the ALU shift has occurred. Notice that the ZERO pin cannot be used to detect whether an input placed on a high impedance Y bus is zero.

divide BCD flip-flops

The multiply-divide flip-flops contain the status of the previous multiply or divide instruction. They are affected by the following instructions:

DIVIDE REMAINDER FIX	SIGNED DIVIDE ITERATE
SIGNED DIVIDE QUOTIENT FIX	UNSIGNED DIVIDE START
SIGNED MULTIPLY	UNSIGNED DIVIDE ITERATE
SIGNED MULTIPLY TERMINATE	UNSIGNED MULTIPLY
SIGNED DIVIDE INITIALIZE	SIGNED DIVIDE TERMINATE
SIGNED DIVIDE START	UNSIGNED DIVIDE TERMINATE

The excess-3 BCD flip-flops are affected by all instructions except NOP. The clear function clears these flip-flops. They preserve the carry from each nibble (4-bits) in excess-3/BCD operations.

package position pin (PPP)

The position of the processor in the system is defined by the voltage level applied to the package position pin (PPP). Intermediate positions are selected by leaving the pin open. Tying the pin to V_{CC} makes the processor the most significant package and tying the pin to GND makes the processor the least significant package.

special shift function (SSF) pin

Conditional shifting algorithms may be implemented via control of the SSF pin. The applied voltage to this pin may be set as a function of a potential overflow condition (the two most significant bits are not equal) or any other condition (see Group 1 instructions).

instruction set

The 'AS895 bit-slice processor uses bits I7-I0 as instruction inputs. A combination of bits I3-I0 (Group 1 instructions) and bits I7-I4 (Group 2-5 instructions) are used to develop the 8-bit op code for a specific instruction. Group 1 and Group 2 instructions can be combined to perform arithmetic or logical functions plus a shift function in one instruction cycle. A summary of the instruction set is given in Table 1.



SN54AS895, SN74AS895
8-BIT MEMORY ADDRESS GENERATORS

TABLE 1. INSTRUCTION SET

GROUP 1 INSTRUCTIONS		
INSTRUCTION BITS (I3-I0) HEX CODE	MNEMONIC	FUNCTION
0		Accesses Group 4 instructions
1	ADD	$R + S + C_n$
2	SUBR	$\bar{R} + S + C_n$
3	SUBS	$R + \bar{S} + C_n$
4	INCS	$S + C_n$
5	INCNS	$\bar{S} + C_n$
6	INCR	$R + C_n$
7	INCNR	$\bar{R} + C_n$
8		Accesses Group 3 instructions
9	XOR	$\bar{R} \text{ XOR } S$
A	AND	$R \text{ AND } S$
B	OR	$R \text{ OR } S$
C	NAND	$R \text{ NAND } S$
D	NOR	$R \text{ NOR } S$
E	ANDNR	$\bar{R} \text{ AND } S$
F		Accesses Group 5 instructions
GROUP 2 INSTRUCTIONS		
INSTRUCTION BITS (I7-I4) HEX CODE	MNEMONIC	FUNCTION
0	SRA	Arithmetic Right Single
1	SRAD	Arithmetic Right Double
2	SRL	Logical Right Single
3	SRLD	Logical Right Double
4	SLA	Arithmetic Left Single
5	SLAD	Arithmetic Left Double
6	SLC	Circular Left Single
7	SLCD	Circular Left Double
8	SRC	Circular Right Single
9	SRCD	Circular Right Double
A	MQSRA	Pass (F→Y) and Arithmetic Right MQ
B	MQSRL	Pass (F→Y) and Logical Right MQ
C	MQSLL	Pass (F→Y) and Logical Left MQ
D	MQSLC	Pass (F→Y) and Circular Left MQ
E	LOADMQ	Pass (F→Y) and Load MQ (F=MQ)
F	PASS	Pass (F→Y)

2

LSI Devices

SN54AS895, SN74AS895
8-BIT MEMORY ADDRESS GENERATORS

TABLE 1. INSTRUCTION SET (Continued)

GROUP 3 INSTRUCTIONS		
INSTRUCTION BITS (I7-I0) HEX CODE	MNEMONIC	FUNCTION
08	SETI	Set Bit
18	SETO	Reset Bit
28	TB1	Test Bit (One)
38	TBO	Test Bit (Zero)
48	ABS	Absolute Value
58	SMTC	Sign Magnitude/Two's Complement
68	ADDI	Add Immediate
78	SUBI	Subtract Immediate
88	BADD	Byte Add R to S
98	BSUBS	Byte Subtract S from R
A8	BSUBR	Byte Subtract R from S
B8	BINCS	Byte Increment S
C8	BINCS	Byte Increment Negative S
D8	BXOR	Byte XOR R and S
E8	BAND	Byte AND R and S
F8	BOR	Byte OR R and S
GROUP 4 INSTRUCTIONS		
INSTRUCTION BITS (I7-I0) HEX CODE	MNEMONIC	FUNCTION
00		Reserved
10	SEL	Select S/R
20	SNORM	Single Length Normalize
30	DNORM	Double Length Normalize
40	DIVRF	Divide Remainder Fix
50	SDIVQF	Signed Divide Quotient Fix
60	SMULI	Signed Multiply Iterate
70	SMULT	Signed Multiply Terminate
80	SDIVIN	Signed Divide Initialize
90	SDIVIS	Signed Divide Start
A0	SDIVI	Signed Divide Iterate
B0	UDIVIS	Unsigned Divide Start
C0	UDIVI	Unsigned Divide Iterate
D0	UMULI	Unsigned Multiply Iterate
E0	SDIVIT	Signed Divide Terminate
F0	UDIVIT	Unsigned Divide Terminate

2
LSI Devices

**SN54AS895, SN74AS895
8-BIT MEMORY ADDRESS GENERATORS**

TABLE 1. INSTRUCTION SET (Concluded)

GROUP 5 INSTRUCTIONS

INSTRUCTION BITS (I7-I0) HEX CODE	MNEMONIC	FUNCTION
0F	CLR	Clear
1F	CLR	Clear
2F	CLR	Clear
3F	CLR	Clear
4F	CLR	Clear
5F	CLR	Clear
6F	CLR	Clear
7F	BCDBIN	BCD to Binary
8F	EX3BC	Excess-3 Byte Correction
9F	EX3C	Excess-3 Word Correction
AF	SDIVO	Signed Divide Overflow Check
BF	CLR	Clear
CF	CLR	Clear
DF	BINEX3	Binary to Excess-3
EF	CLR	Clear
FF	NOP	No Operation

2

LSI Devices

group 1 instructions

TABLE 2. GROUP 1 INSTRUCTIONS

INSTRUCTION BITS (I3-I0) HEX CODE	MNEMONIC	FUNCTION
0		Accesses Group 4 instructions
1	ADD	$R + S + C_n$
2	SUBR	$\bar{R} + S + C_n$
3	SUBS	$R + \bar{S} + C_n$
4	INCS	$S + C_n$
5	INCNS	$\bar{S} + C_n$
6	INCR	$R + C_n$
7	INCNR	$\bar{R} + C_n$
8		Accesses Group 3 instructions
9	XOR	R XOR S
A	AND	R AND S
B	OR	R OR S
C	NAND	R NAND S
D	NOR	R NOR S
E	ANDNR	\bar{R} AND S
F		Accesses Group 5 instructions

Group 1 instructions (excluding hex codes 0, 8, and F), shown in Table 2, may be used in conjunction with Group 2 shift instructions to perform arithmetic or logical functions plus a shift function[†] in one instruction cycle (hex codes 0, 8, and F are used to access Group 4, 3, and 5 instructions, respectively). Each shift may be made into a conditional shift by forcing the special shift function (SSF) pin into the proper state. If the SSF pin is high or floating, the shifted ALU output will be sent to the output buffers. If the SSF pin is pulled low externally, the ALU result will be passed directly to the output buffers. Conditional shifting is useful for scaling inputs in data arrays or in signal processing algorithms.

These instructions set the BCD flip-flop for the excess-3 correct instruction. The status is set with the following results (C_{n+8} is ALU carry out and is independent of shift operation; others are evaluated after shift operation).

[†]Double-precision shifts involve both the ALU and MQ register.

Status is set with the following results:

Arithmetic

- N → MSB of result
- OVR → Signed arithmetic overflow
- C_{n+8} → Carry out equal one
- Z → Result equal zero

Logic

- N → MSB of result
- OVR → None (force to zero)
- C_{n+8} → None (force to zero)
- Z → Result equal zero

group 2 instructions

TABLE 3. GROUP 2 INSTRUCTIONS

INSTRUCTION BITS (I7-I4) HEX CODE	MNEMONIC	FUNCTION
0	SRA	Arithmetic Right Single
1	SRAD	Arithmetic Right Double
2	SRL	Logical Right Single
3	SRLD	Logical Right Double
4	SLA	Arithmetic Left Single
5	SLAD	Arithmetic Left Double
6	SLC	Circular Left Single
7	SLCD	Circular Left Double
8	SRC	Circular Right Single
9	SRCD	Circular Right Double
A	MQSRA	Pass (F→Y) and Arithmetic Right MQ
B	MQSRL	Pass (F→Y) and Logical Right MQ
C	MQSLL	Pass (F→Y) and Logical Left MQ
D	MQSLC	Pass (F→Y) and Circular Left MQ
E	LOADMQ	Pass (F→Y) and Load MQ (F = MQ)
F	PASS	Pass (F→Y)

SN54AS895, SN74AS895 8-BIT MEMORY ADDRESS GENERATORS

The processor's shift instructions are implemented by a combination of Group 2 instructions (Table 3) and certain wired connections on the packages used. The following external connections are required.

On intermediate packages:

$\overline{SIO7}$ is connected to $\overline{SIO0}$ of the next most significant package
 $\overline{QIO7}$ is connected to $\overline{QIO0}$ of the next most significant package
 $\overline{SIO0}$ is connected to $\overline{SIO7}$ of the next least significant package
 $\overline{QIO0}$ is connected to $\overline{QIO7}$ of the next least significant package

On the two end packages:

$\overline{SIO7}$ on the most significant package is connected to $\overline{SIO0}$ of the least significant package.
 $\overline{QIO7}$ on the most significant package is connected to $\overline{QIO0}$ of the least significant package.

The connections are the same on all instructions including multiply, divide, and normalization functions.

Single- and double-precision shifts are supported. Double-precision shifts assume the most significant half has come through the ALU and will be placed (if \overline{WE} is low) into the register file on the rising edge of the clock and the least significant half lies in the MQ register. All Group 2 shifts may be made conditional (see previous page).

The following definitions apply to Group 2 shift instructions:

Arithmetic right shifts copy the sign of the number if no overflow occurs from the ALU calculation; if overflow occurs, the sign bit is inverted.

Arithmetic left shifts do not retain the sign of the number if an overflow occurs. A zero is filled into the LSB if not forced externally.

Logical right shifts fill a zero in the MSB position if not forced externally.

Logical left shifts fill a zero in the LSB position if not forced externally.

Circular right shifts fill the LSB in the MSB position.

Circular left shifts fill the MSB in the LSB position.

Shifting left is defined as moving a bit position towards the MSB (doubling).

Shifting right is defined as moving a bit towards the LSB (halving).

Serial input may be performed using the circuitry shown in Figure 1. A single-/or double-precision arithmetic left or logical right shift fills the complement of the data on $\overline{SIO0}$ and $\overline{SIO7}$ into the LSB or MSB of the data word(s). Note that if $\overline{SIO0}$ and $\overline{SIO7}$ are floating (HI-Z), a zero will be filled as an end condition.

Serial output may be performed with circular instructions.

SN54AS895, SN74AS895
8-BIT MEMORY ADDRESS GENERATORS

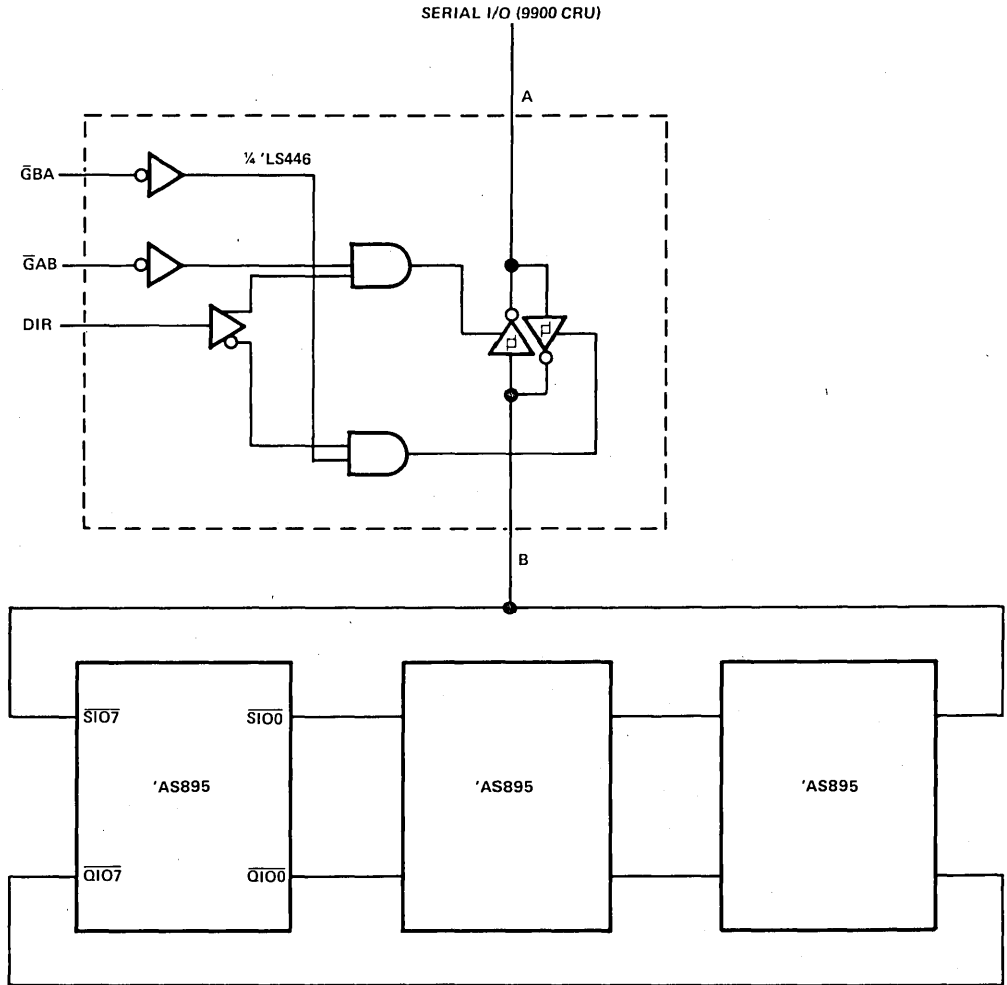


FIGURE 1. SERIAL I/O

SN54AS895, SN74AS895 8-BIT MEMORY ADDRESS GENERATORS

The shift instructions are summarized in Table 4 and illustrated in Figure 2. In Figure 2 and all succeeding figures that illustrate instruction execution, the following definitions apply:

- QBT — End fill for signed divide.
- MQF — End fill for unsigned divide.
- SRF — End fill for signed multiply and the arithmetic right shifts.

TABLE 4. SHIFT INSTRUCTIONS

OP CODE†	SHIFT FUNCTION‡	SIO7 • SIO0 WIRED VALUE	QIO7 • QIO0 WIRED VALUE
0N	Arithmetic Right Single	ALU-LSB Output	—
1N	Arithmetic Right Double	MQ-LSB Output	ALU-LSB Output
2N	Logical Right Single	Input to ALU-MSB	ALU-LSB Output
3N	Logical Right Double	Input to ALU-MSB	ALU-LSB Output
4N	Arithmetic Left Single	Input to ALU-LSB	ALU-MSB Output
5N	Arithmetic Left Double	Input to MQ-LSB	MQ-MSB Output
6N	Circular Left Single	ALU-MSB Output	—
7N	Circular Left Double	ALU-MSB Output	MQ-MSB Output
8N	Circular Right Single	ALU-LSB Output	—
9N	Circular Right Double	MQ-LSB Output	ALU-LSB Output
AN	Arithmetic Right (MQ only)	MQ-LSB Output	MQ-LSB Output
BN	Logical Right (MQ only)	MQ-LSB Output	Input to MQ-MSB
CN	Logical Left (MQ only)	Input to MQ-LSB	MQ-MSB Output
DN	Circular Left (MQ only)	MQ-MSB Output	MQ-MSB Output

†Op Code N ≠ 0, 8, or F; these select special instruction Groups 4, 3, and 5 respectively.

‡Shift I/O pins are active low. Therefore, inputs and outputs must be inverted if true logical values are required.

Status is set with the following results:

Arithmetic

- N → Result MSB equal one
- OVR → Signed arithmetic overflow†
- C_{n+8} → Carry out equal one
- Z → Result equal zero

Logic

- N → Result MSB equal one
- OVR → Zero
- C_{n+8} → Zero
- Z → Result equal zero

† For the SLA and SLAD instructions, OVR is set if signed arithmetic overflow or if the ALU result MSB XOR MSB-1 equals one.

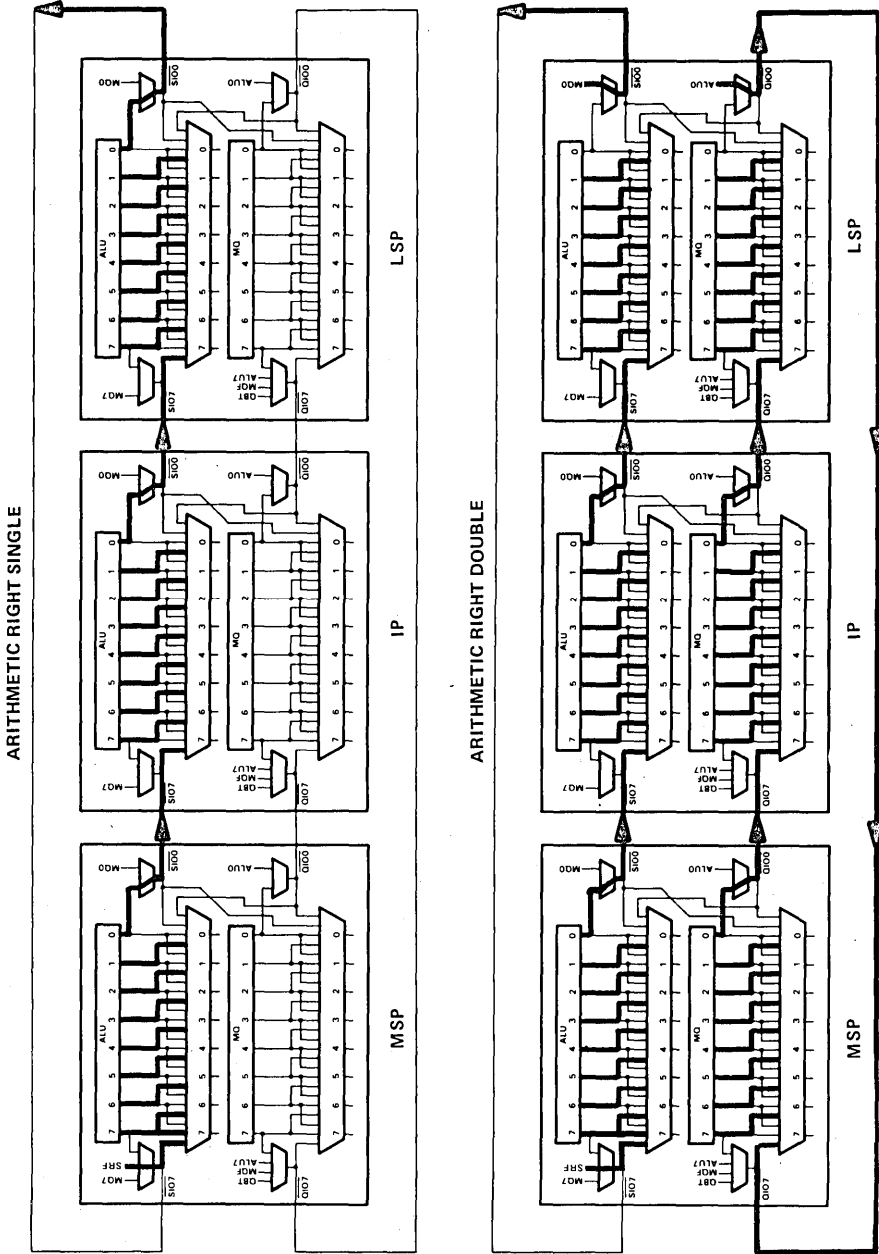


FIGURE 2. SHIFT INSTRUCTIONS

SN54AS895, SN74AS895
8-BIT MEMORY ADDRESS GENERATORS

2

LSI Devices

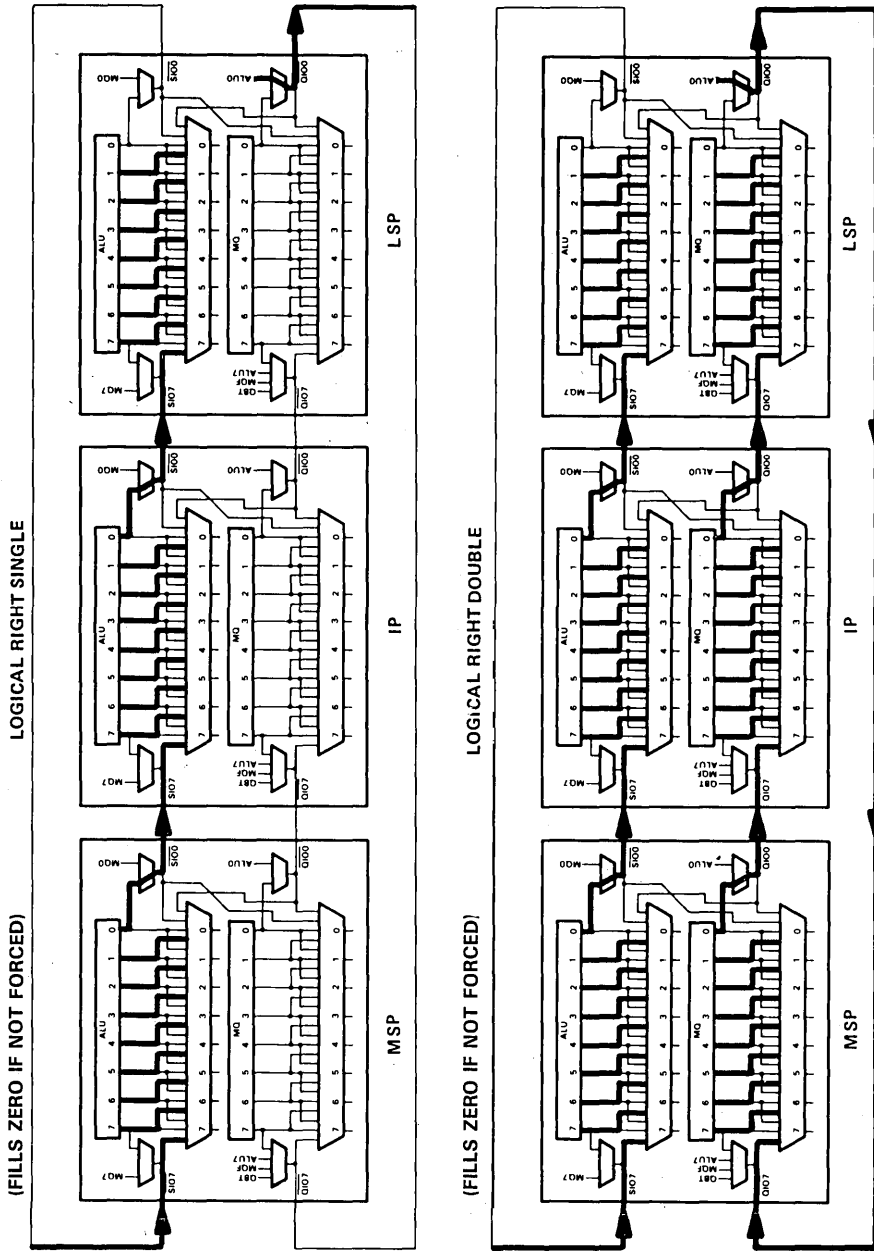


FIGURE 2. SHIFT INSTRUCTIONS (Continued)

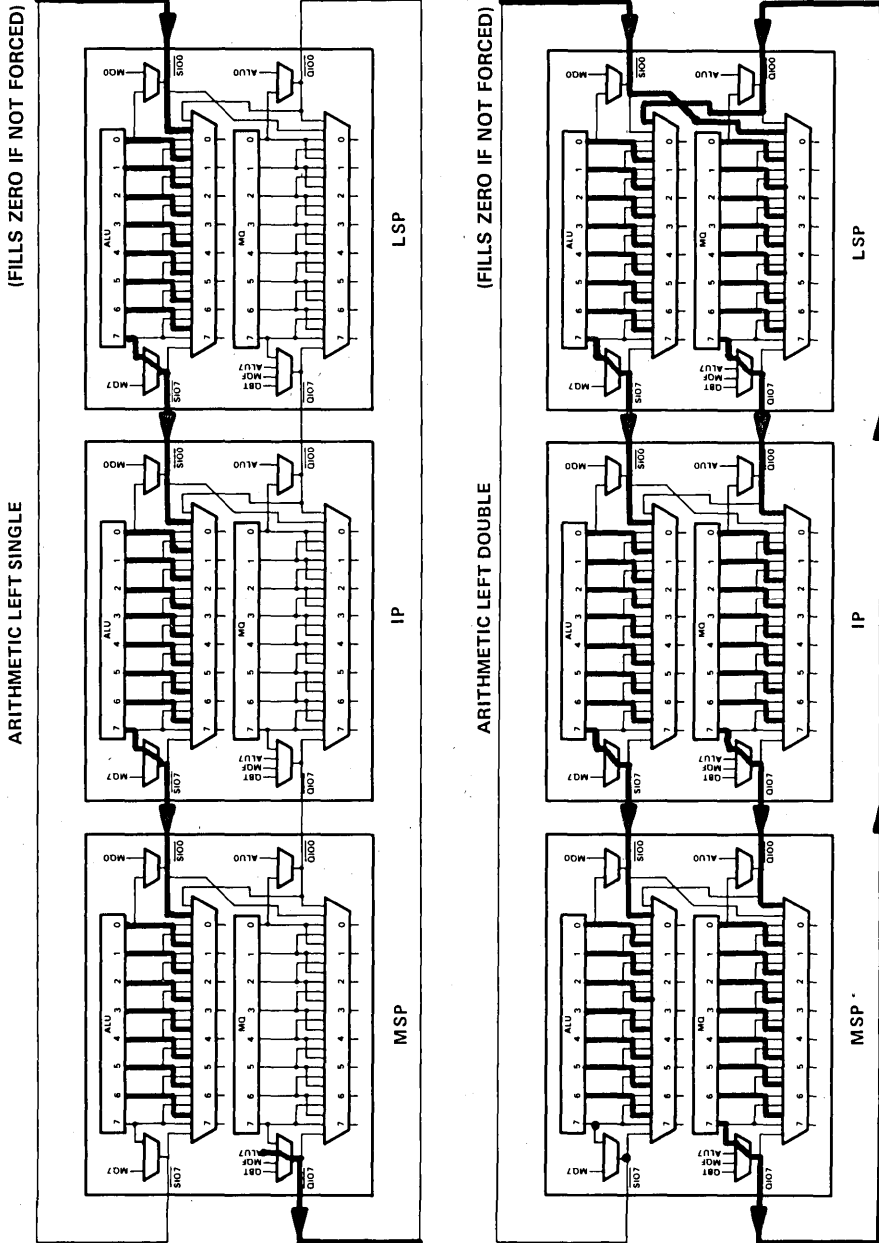


FIGURE 2. SHIFT INSTRUCTIONS (Continued)

SN54AS895, SN74AS895
8-BIT MEMORY ADDRESS GENERATORS

2

LSI Devices

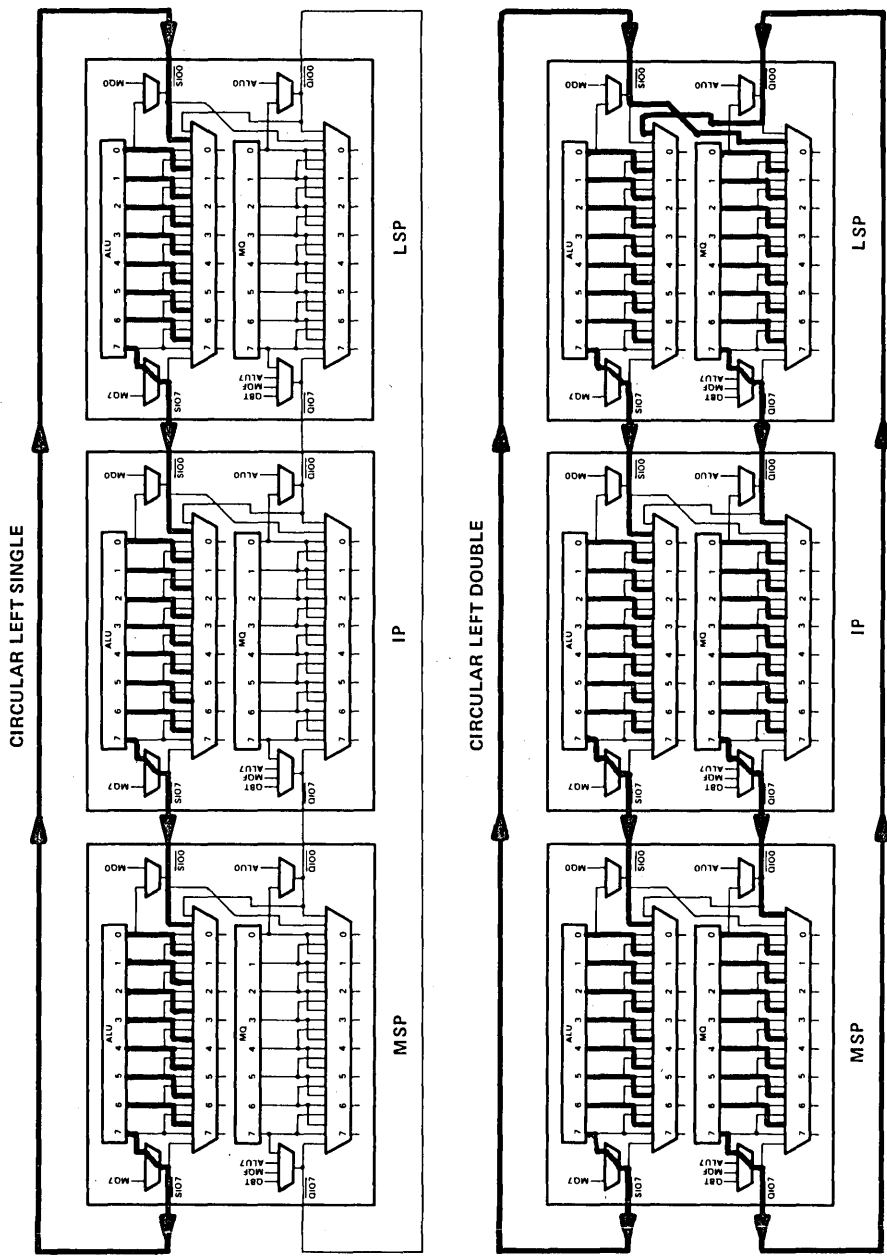


FIGURE 2. SHIFT INSTRUCTIONS (Continued)

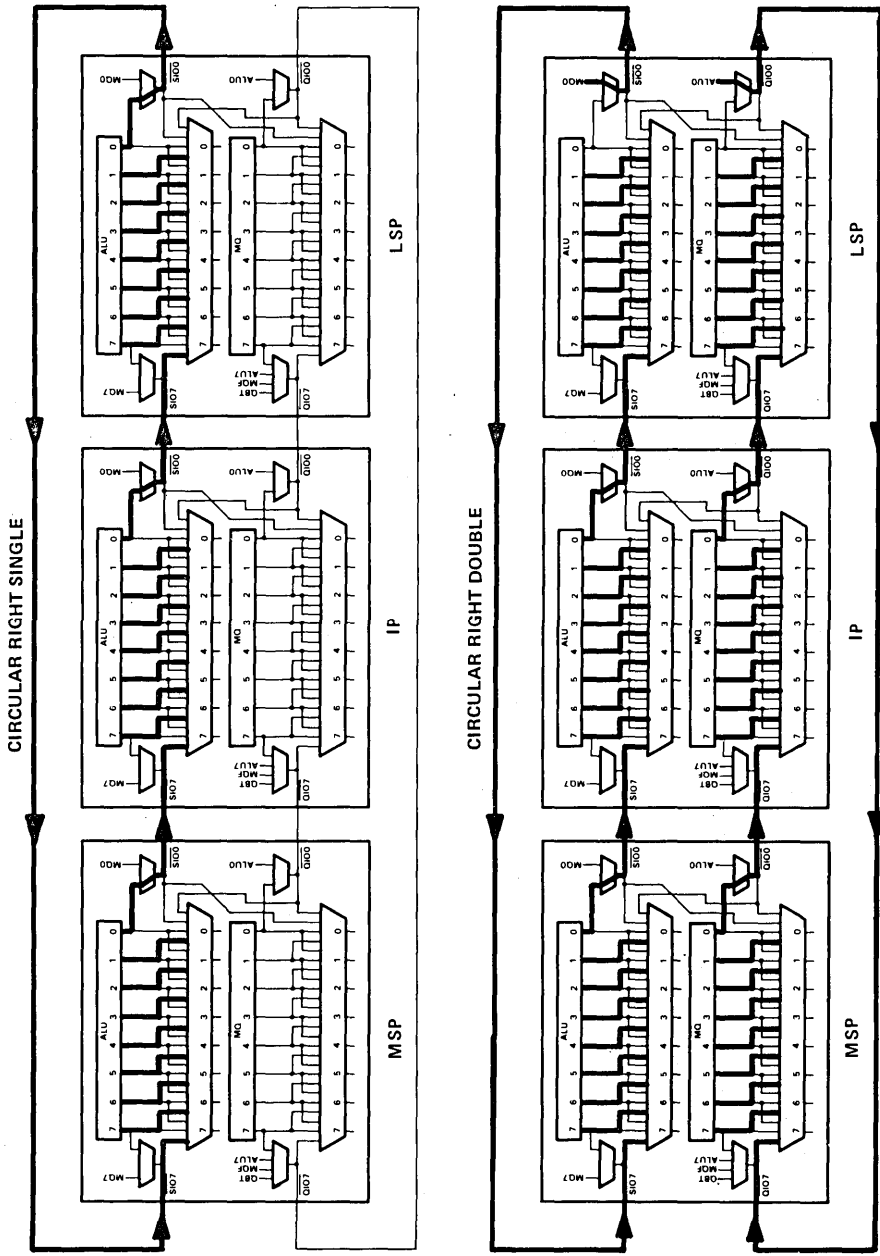


FIGURE 2. SHIFT INSTRUCTIONS (Continued)

SN54AS895, SN74AS895
8-BIT MEMORY ADDRESS GENERATORS

2 LSI Devices

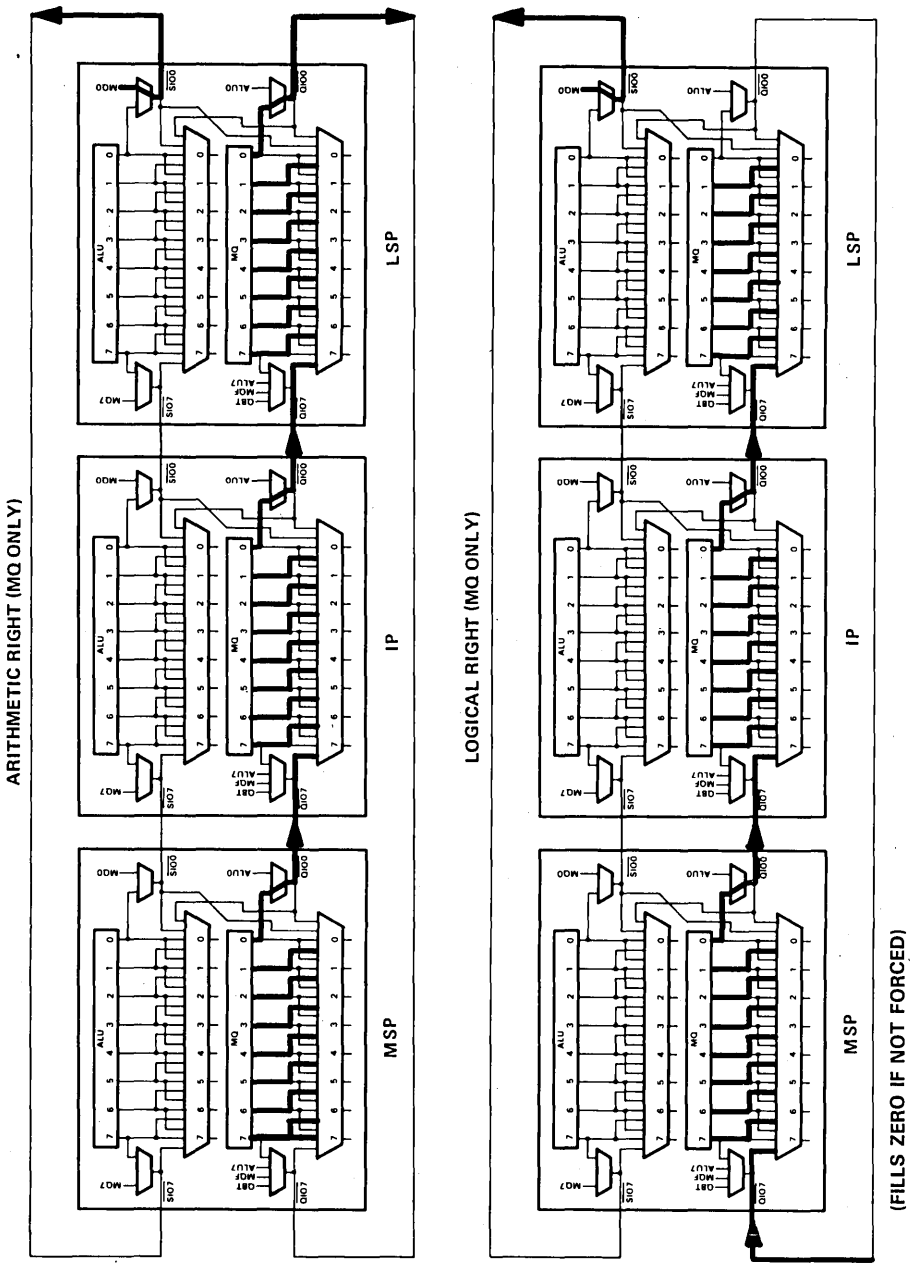


FIGURE 2. SHIFT INSTRUCTIONS (Continued)

(FILLS ZERO IF NOT FORCED)

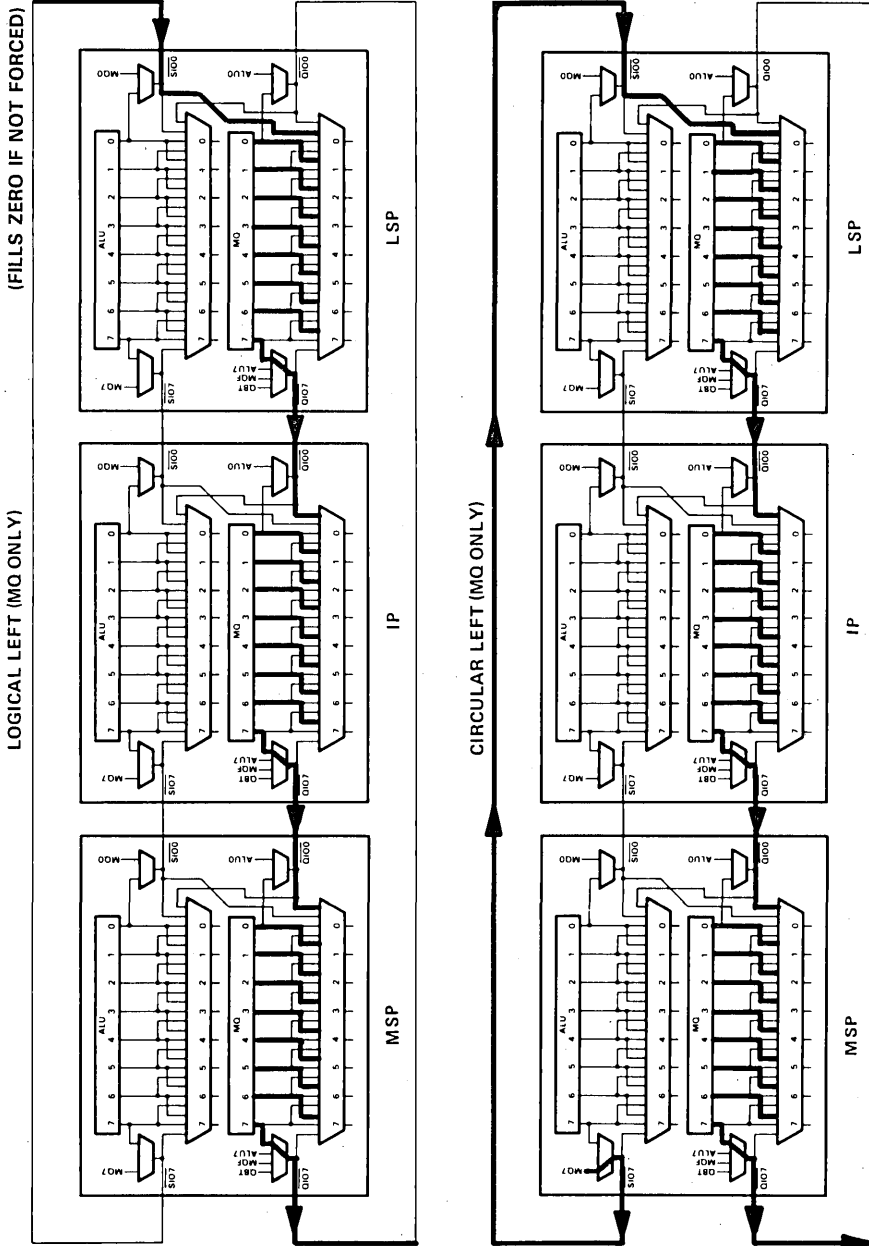


FIGURE 2. SHIFT INSTRUCTIONS (Concluded)

SN54AS895, SN74AS895
8-BIT MEMORY ADDRESS GENERATORS

group 3 instructions

Hex code 8 of Group 1 instructions is used to access Group 3 instructions. Group 3 instructions are summarized in Table 5.

TABLE 5. GROUP 3 INSTRUCTIONS

INSTRUCTION BITS (I7-I0) OP CODE (HEX)	MNEMONIC	FUNCTION
08	SET1	Set Bit
18	SET0	Reset Bit
28	TB1	Test Bit (One)
38	TB0	Test Bit (Zero)
48	ABS	Absolute Value
58	SMTC	Sign Magnitude/Two's Complement
68	ADDI	Add Immediate
78	SUBI	Subtract Immediate
88	BADD	Byte Add R to S
98	BSUBS	Byte Subtract S from R
A8	BSUBR	Byte Subtract R from S
B8	BINCS	Byte Increment S
C8	BINCNS	Byte Increment Negative S
D8	BXOR	Byte XOR R and S
E8	BAND	Byte AND R and S
F8	BOR	Byte OR R and S

SN54AS895, SN74AS895 8-BIT MEMORY ADDRESS GENERATORS

set bit instruction (set1): I7-I0 = 0816

This instruction (Figure 3) is used to force selected bits of a desired byte(s) to one. The desired bits are specified by an 8-bit mask (C3-C0)::(A3-A0)[†] consisting of register file address ports that are not required to support this instruction. All bits in the selected byte(s) that are in the same bit positions as ones in the mask are forced to a logical one. The B3-B0 address field is used for both source and destination of this instruction. The desired byte is specified by forcing S100 to a low value. Nonselected packages pass the byte through unaltered. The S bus is the source word for this instruction. The status set by the set bit instruction is as follows:

- N → None (force to zero)
- OVR → None (force to zero)
- C_n+8 → None (force to zero)
- Z → Result equal zero

[†] The symbol "::" is concatenation operator

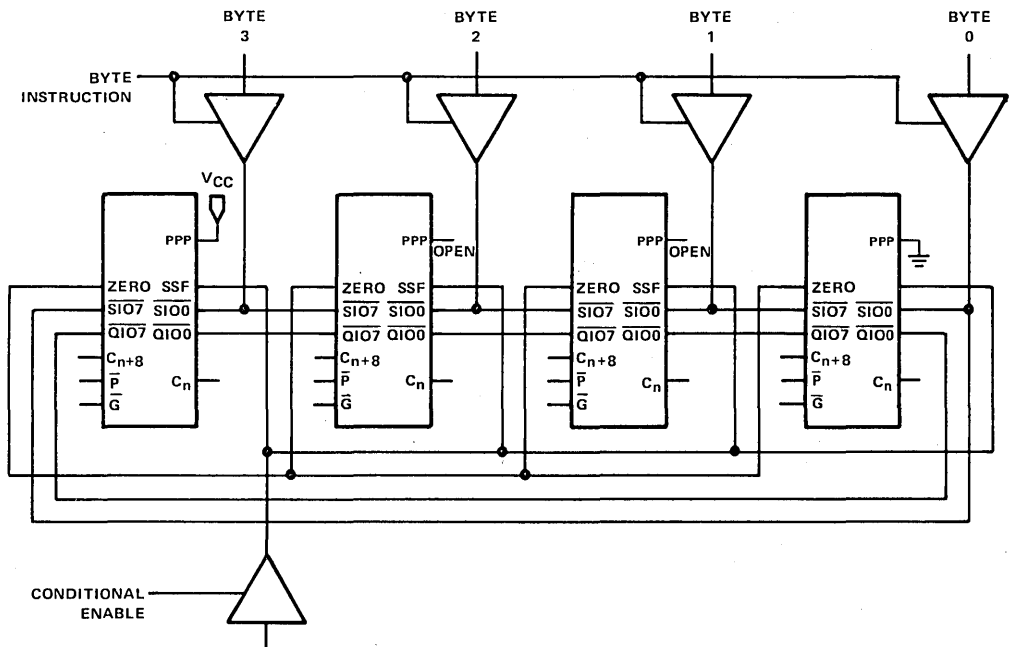


FIGURE 3. SET BIT (OR RESET BIT)

- NOTES: 1. Force S100 = low to select byte.
2. Bit mask (C3-C0)::(A3-A0) will set desired bits to one.

reset bit instruction (set0): I7-I0 = 1816

This instruction (Figure 3) is used to force selected bits of a desired byte(s) to zero. The desired bits are specified by an 8-bit mask (C3-C0)::(A3-A0) consisting of register file address ports that are not required to support this instruction. All bits in the selected byte(s) that are in the same bit positions as ones in the mask are reset. The B3-B0 address field is used for both source and destination of this instruction.

SN54AS895, SN74AS895 8-BIT MEMORY ADDRESS GENERATORS

The desired byte is specified by forcing $\overline{S100}$ to a low value. Nonselected packages pass the byte through unaltered. The S bus is the source word for this instruction. The status set by the reset bit instruction is as follows:

- N → None (force to zero)
- OVR → None (force to zero)
- C_n+8 → None (force to zero)
- Z → Result equal zero

test bit (one) instruction (TB1): 17-10 = 2816

This instruction (Figure 4) is used to test selected bits of a desired byte(s). Bits to be tested are specified by an 8-bit mask (C3-C0)::(A3-A0) consisting of register file address ports that are not required to support this instruction. Write Enable (WE) is internally disabled during this instruction. The desired byte is specified by forcing $\overline{S100}$ to a low value. The test will pass if the selected byte has ones at all bit locations specified by the ones of the mask (Figure 5). The S bus is the source word for this instruction. The status set by the test bit (one) instruction is as follows:

- N → None (force to zero)
- OVR → None (force to zero)
- C_n+8 → None (force to zero)
- Z → Pass

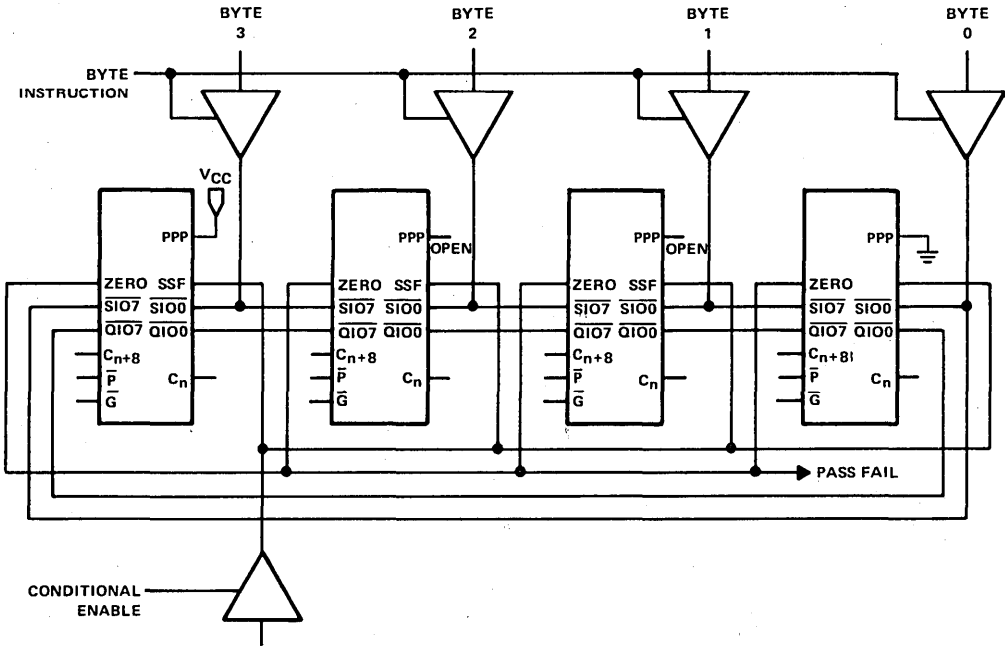


FIGURE 4. TEST BIT

- NOTES: 1. Force $\overline{S100}$ = low to select byte.
 2. Bit mask (C3-C0)::(A3-A0) will define bits for testing.
 3. Pass/fail is indicated on Z output.

test bit (zero) instruction (TBO): 17-10 = 3816

This instruction (Figure 4) is used to test selected bits of a desired byte(s). Bits to be tested are specified by an 8-bit mask (C3-C0):(A3-A0) consisting of register file address ports that are not required to support this instruction. Write Enable (\overline{WE}) is internally disabled during this instruction. The desired byte is specified by forcing $\overline{SIO0}$ to a low value. The test will pass if the selected byte has zeros at all bit locations specified by the ones of the mask (Figure 6). The S bus is the source word for this instruction. The status set by the test bit (zero) instruction is as follows:

- N → None (force to zero)
- OVR → None (force to zero)
- C_{n+8} → None (force to zero)
- Z → Pass

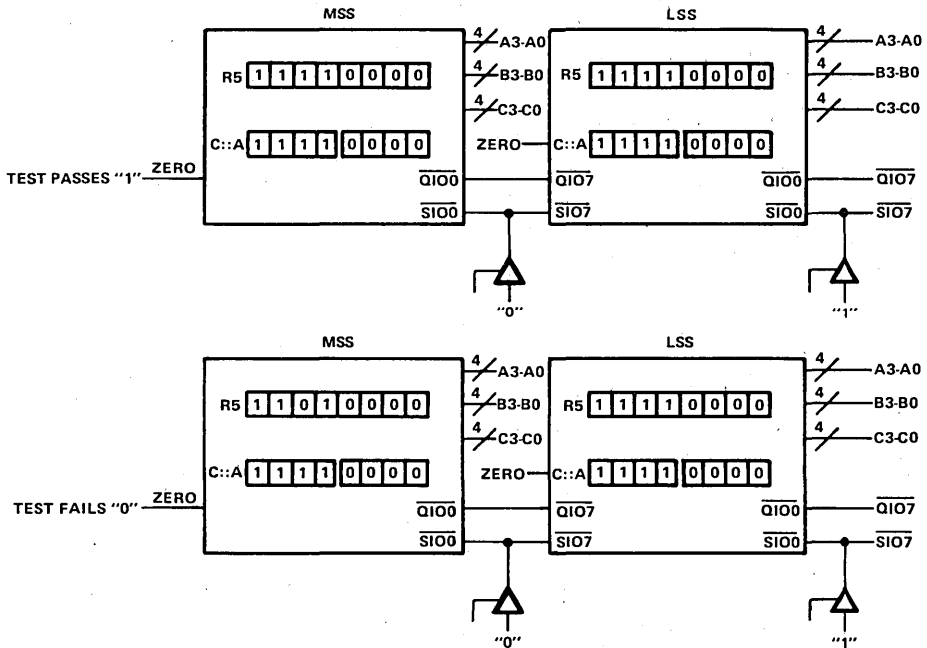


FIGURE 5. TEST BIT ONE EXAMPLES

SN54AS895, SN74AS895 8-BIT MEMORY ADDRESS GENERATORS

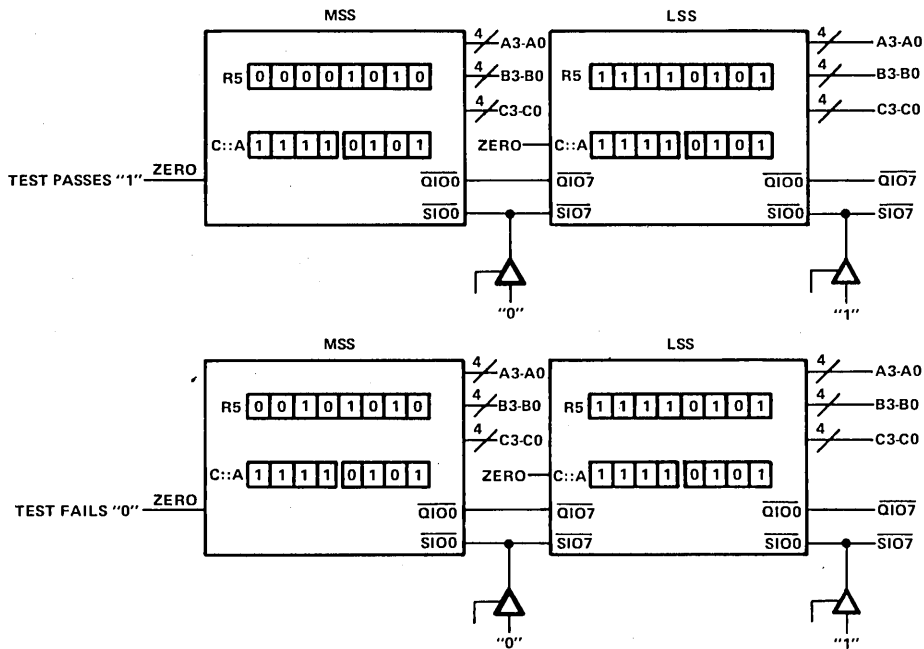


FIGURE 6. TEST BIT ZERO EXAMPLES

absolute value instruction (ABS): 17-10 = 4816

This instruction is used to convert two's complement numbers to their positive value. The operand placed on the S bus is the source for this instruction. The MSP will test the sign of the S bus and force the SSF pin to the proper value. All other packages use the SSF pin as input to determine instruction execution. The status set by the absolute value instruction is as follows:

- N → Input MSB equal one
- OVR → Input equal 8000 (hex)
- C_{n+8} → S = 0
- Z → Result equal zero

sign magnitude/two's complement instruction (SMTC): 17-10 = 5816

This instruction allows conversion from two's complement representation to sign magnitude representation, or vice-versa, in one clock cycle. The operand placed on the S bus is the source for this instruction.

When a negative zero (8000 hex) is converted, the result is 0000 with an overflow. If the input is in two's complement notation, the overflow indicates an illegal conversion. The status set by the sign magnitude/two's complement instruction is as follows:

- N → Result MSB equal one
- OVR → Input equal 8000 (hex)
- C_{n+8} → Input equal 0000 (hex)
- Z → Result equal zero

add immediate instruction (ADDI): 17-10 = 68₁₆

This instruction is used to add a specified constant value to the operand placed on the S bus. The constant will be between the values of 0 and 15. The constant value is specified by the unused register file address (A port) not required to support this instruction. Forcing the carry input will add an additional one to the result. The status set by the add immediate instruction is as follows:

- N → Result MSB equal one
- OVR → Arithmetic signed overflow
- C_{n+8} → Carry out equal one
- Z → Result equal zero

subtract immediate instruction (SUBI): 17-10 = 78₁₆

This instruction is used to subtract a specified constant value from the operand placed on the S bus. The constant value is specified by the unused register file address (A port) that is not required to support this instruction. The constant applied is the least significant four bits of a two's complement number. The device sign extends the constant over the entire word length. The status set by the subtract immediate instruction is as follows:

- N → Result MSB equal one
- OVR → Arithmetic signed overflow
- C_{n+8} → Carry out equal one
- Z → Result equal zero

byte instructions

There are eight byte instructions in Group 3. These instructions modify selected bytes of the operand on the S bus. A byte is selected by forcing SIOO to a low value (same as SET1, SET0, TB1, and TBO instructions). Multiple bytes may be selected only if they are adjacent to one another.

NOTE: At least one byte must be nonselected during these instructions.

The nonselected bytes are passed through unaltered. Byte status is forced through the most significant package except for the sign of the result (N), which is forced to zero (low). The status set by the byte instructions is as follows:

(Most Significant Package)

- N → None (force to zero)
- OVR → Byte signed overflow
- C_{n+8} → Byte carry out equal one
- Z → Byte result equal to zero

(Selected BYTES—other than MSP)

- G → Normal generate
- P → Normal propagate
- C_{n+8} → Normal carry out
- Z → Result equal to zero

(Nonselected BYTES—other than MSP)

- G → No generate (force to one)
- P → Propagate (force to zero)
- C_{n+8} → C_n
- Z → None (force to one)

SN54AS895, SN74AS895 8-BIT MEMORY ADDRESS GENERATORS

group 4 instructions

Hex code 0 of Group 1 instructions is used to access Group 4 instructions. Group 4 instructions are summarized in Table 6.

TABLE 6. GROUP 4 INSTRUCTIONS

INSTRUCTION BITS (I7-I0) OP CODE (HEX)	MNEMONIC	FUNCTION
00		Reserved
10	SEL	Select S/R
20	SNORM	Single Length Normalize
30	DNORM	Double Length Normalize
40	DIVRF	Divide Remainder Fix
50	SDIVQF	Signed Divide Quotient Fix
60	SMULI	Signed Multiply Iterate
70	SMULT	Signed Multiply Terminate
80	SDIVIN	Signed Divide Initialize
90	SDIVIS	Signed Divide Start
A0	SDIVI	Signed Divide Iterate
B0	UDIVIS	Unsigned Divide Start
C0	UDIVI	Unsigned Divide Iterate
D0	UMULI	Unsigned Multiply Iterate
E0	SDIVIT	Signed Divide Terminate
F0	UDIVIT	Unsigned Divide Terminate

select S/R instruction (SEL): I7-I0 = 1016

This instruction is used to pass either the S bus or the R bus to the output depending on the state of the SSF input pin. Normally, the preceding instruction would test the two operands and the resulting status information would be used to force the SSF input pin. SSF = 0 will output the R bus and SSF = 1 will output the S bus. The status set by the select S/R instruction is as follows:

- N → Result MSB equal one
- OVR → None (force to zero)
- C_n+8 → None (force to zero)
- Z → Result equal zero

single-length normalize instruction (SNORM): I7-I0 = 2016

This instruction will cause the contents of the MQ register to shift toward the most significant bit. Zeros are shifted in via the Q100 input. The number of shifts performed can be counted and stored in one of the register files by forcing a high at the C_n input. When the two most significant bits are of opposite value, normalization is complete. This condition is indicated on the microcycle that completes the normalization at the OVR output.

The chip contains conditional logic that inhibits the shift function (and also inhibits the register file increment) if the number within the MQ register is already normalized at the beginning of the instruction (Figure 7). The status set by the single-length normalize instruction is as follows:

- N → MSB of result
- OVR → MSB XOR 2nd MSB
- C_n+8 → Carry out equal one
- Z → Result equal zero

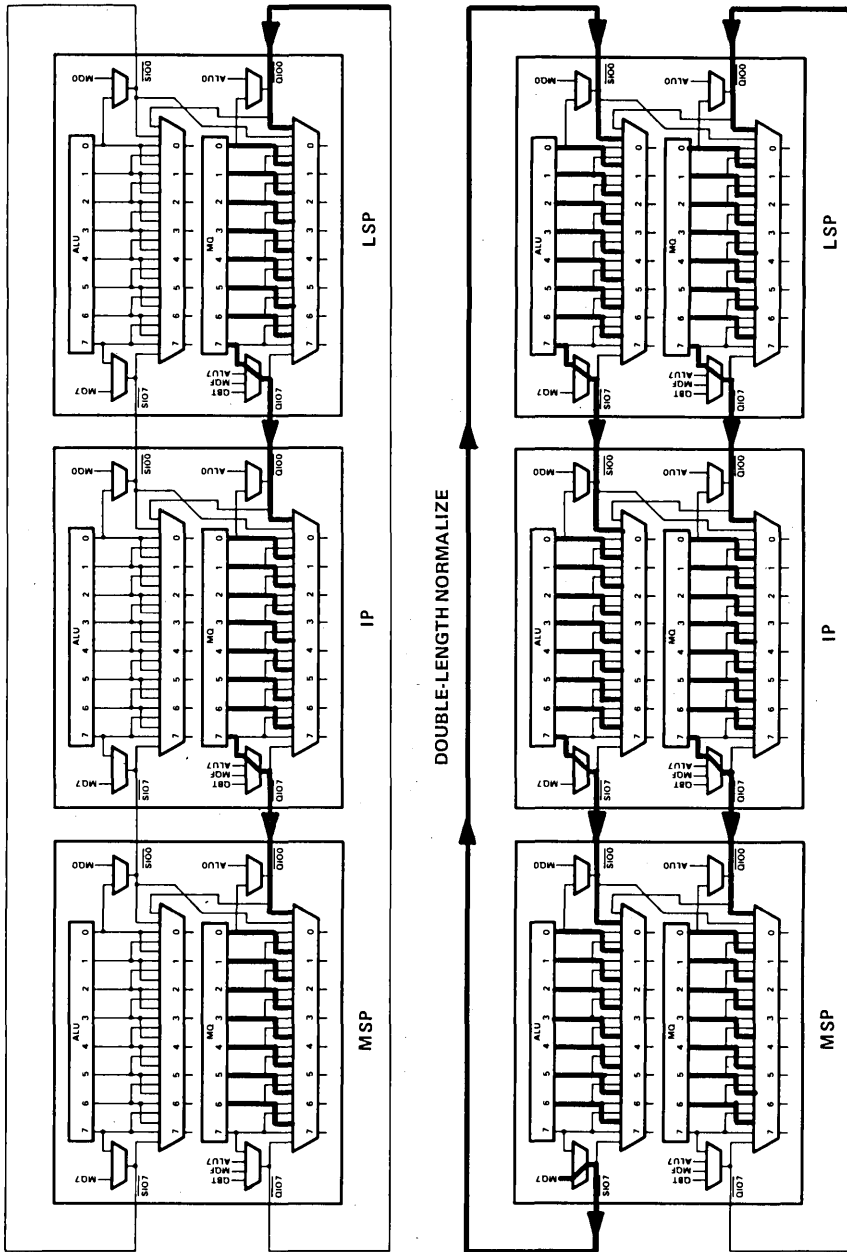


FIGURE 7. SINGLE-AND DOUBLE-LENGTH NORMALIZE

SN54AS895, SN74AS895 8-BIT MEMORY ADDRESS GENERATORS

double-length normalize instruction (DNORM): I7-I0 = 30₁₆

This instruction will cause the contents of a double-length word (register file contains the most significant half and the MQ register contains the least significant half) to shift toward the most significant bit. Zeros are shifted in via the \overline{QIOO} input. When the two most significant bits are of opposite value, normalization is complete. This condition is indicated on the microcycle that completes the normalization at the OVR output.

The chip contains conditional logic which inhibits the shift function if the number is already normalized at the beginning of the instruction (Figure 7). The most significant half of the operand must be placed on the S bus. The status set by the double-length normalize instruction is as follows:

N	→	MSB of result
OVR	→	MSB XOR 2nd MSB
C _{n+8}	→	None (force to zero)
Z	→	Result equal zero

multiply operations

The ALU performs three unique types of N by N multiplies each of which produces a 2N-bit result (Figure 8). All three types of multiplication proceed via the following recursion:

$$P(J+1) = 2[P(J) + \text{Multiplicand} \times M(8N-J)]$$

where

$$P(J) = \text{partial product at iteration number } J$$

$$N = \text{number of 'AS888 packages that are cascaded}$$

$$P(J+1) = \text{partial product at iteration number } J+1$$

$$J \text{ varies from } 0 \text{ to } 8N [N = 2 \text{ for } 16 \times 16 \text{ multiply}]$$

$$M(8N-J) = \text{mode bit (unique to multiply type)}$$

$$2 \text{ denotes some type of shift (unique to multiply)}$$

Notice that by proper choice of mode terms and shifting operations, signed, unsigned, and mixed multiplies (signed times unsigned) may be performed.

All multiplies assume that the multiplier is stored in MQ before the operation begins (in the case of mixed multiply, the unsigned number must be the multiplier).

The processor has the following multiply instructions:

1. SIGNED MULTIPLY ITERATE (SMULI): I7-I0 = 60₁₆
2. SIGNED MULTIPLY TERMINATE (SMULT): I7-I0 = 70₁₆
3. UNSIGNED MULTIPLY ITERATE (UMULI): I7-I0 = D0₁₆

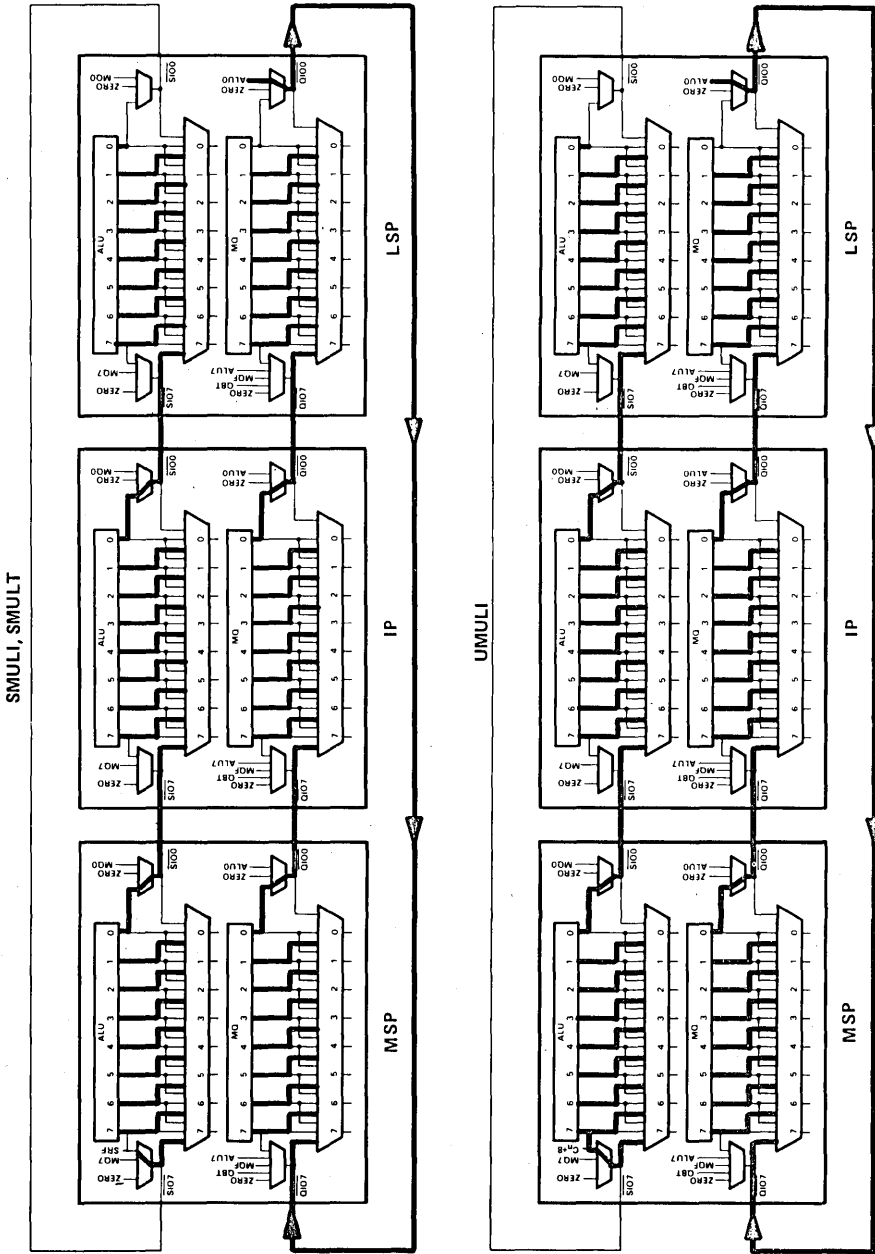


FIGURE 8. MULTIPLICATION OPERATIONS

2

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SN54AS895, SN74AS895

8-BIT MEMORY ADDRESS GENERATORS

The signed multiply iterate (SMULI) instruction performs a signed times signed iteration. This instruction interprets M(8N-J) as the 8N-J bit of the multiplier. The shift is a double-precision right shift one bit. This instruction is repeated 15 times for a 16×16 signed multiply. This instruction will be used 16 consecutive times for a mixed multiplication.

The signed multiply terminate (SMULT) instruction provides correct (negative) weighting of the sign bit of a negative multiplier in signed multiplication. The instruction is identical to signed multiply iterate (SMULI) except that M(8N-J) is interpreted as -1 if the sign bit of the multiplier is 1, and 0 if the sign bit of the multiplier is 0.

The unsigned multiply iterate (UMULI) performs an unsigned multiplication iteration. This instruction interprets M(8N-J) as the 8N-J bit of the multiplier. The shift is a double-precision right shift with the carry out from the $P(J) + \text{Multiplicand} \times M(8N-J)$ operation forced into bit 8N of $P(J + 1)$. This instruction is used in unsigned and mixed multiplication.

signed multiplication

Signed multiplication performs an $8N + 2$ clock two's complement multiply. The instructions necessary to produce an algebraically correct result proceed in the following manner:

Zero register to be used for accumulator

Load MQ with multiplier

SMULI (repeat 8N-1 times)	S port = Accumulator
	R port = Multiplicand
	F port = Iteration result

SMULT	S port = Accumulator
	R port = Multiplicand
	F port = Product (MSH)

At completion, the accumulator will contain the 8N most significant bits and the MQ contains the 8N least significant bits of the product.

The status for the signed multiply iterate should not be used for any testing (overflow is not set by SMULI). The following status is set for the signed multiply terminate instruction:

N	→	Result MSB equal one
OVR	→	Forced to zero
$C_n + 8$	→	Carry out equal to one
Z	→	Double precision result is zero

unsigned multiplication

Unsigned multiplication produces an unsigned times unsigned product in $8N + 2$ clocks. The instructions necessary to produce an algebraically correct result proceed in the following manner:

Zero register to be used for accumulator

Load MQ with multiplier

UMULI (8N times)	S port = Accumulator
	R port = Multiplicand
	F port = Iteration result (product MSH on final result)

Upon completion, the accumulator will contain the 8N most significant bits and the MQ contains the 8N least significant bits of the product.

The status set by the unsigned multiply iteration is meaningless except on the final execution of the instruction. The status set by the unsigned multiply iteration instruction is as follows:

- N → Result MSB equal one
- OVR → Forced to zero
- C_{n+8} → Carry out equal to one
- Z → Double-precision result is zero

mixed multiplication

Mixed multiplication multiplies a signed multiplicand times an unsigned multiplier to produce a signed result in 8N+2 clocks. The steps are as follows:

Zero register used for accumulator

Load MQ with unsigned multiplier

SMULI (8N times)

- S port = Accumulator
- R port = Multiplicand
- F port = Iteration result

Upon completion, the accumulator will contain the 8N most significant bits and the MQ will contain the 8N least significant bits of the product.

The following status is set by the last SMULI instruction:

- N → Result MSB equal one
- OVR → Forced to zero
- C_{n+8} → Carry out equal to one
- Z → Double-precision result is zero

divide operations

The divide uses a nonrestoring technique to perform both signed and unsigned division of a 16N bit integer dividend and an 8N bit integer divisor (Figure 9). It produces an 8N integer quotient and remainder.

The remainder and quotient will be such that the following equation is satisfied:

$$(\text{Quotient}) \times (\text{Divisor}) + \text{Remainder} = \text{Dividend}$$

The processor has the following divide instructions:

1. UNSIGNED DIVIDE START (UDIVIS): I7-I0 = B0₁₆
2. UNSIGNED DIVIDE ITERATE (UDIVI): I7-I0 = C0₁₆
3. UNSIGNED DIVIDE TERMINATE (UDIVIT): I7-I0 = F0₁₆
4. SIGNED DIVIDE INITIALIZE (SDIVIN): I7-I0 = 80₁₆
5. SIGNED DIVIDE OVERFLOW TEST (SDIVO): I7-I0 = AF₁₆
6. SIGNED DIVIDE START (SDIVIS): I7-I0 = 90₁₆
7. SIGNED DIVIDE ITERATE (SDIVI): I7-I0 = A0₁₆
8. SIGNED DIVIDE TERMINATE (SDIVIT): I7-I0 = E0₁₆
9. DIVIDE REMAINDER FIX (DIVRF): I7-I0 = 40₁₆
10. SIGNED DIVIDE QUOTIENT FIX (SDIVQF): I7-I0 = 50₁₆

2
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SN54AS895, SN74AS895
8-BIT MEMORY ADDRESS GENERATORS

2

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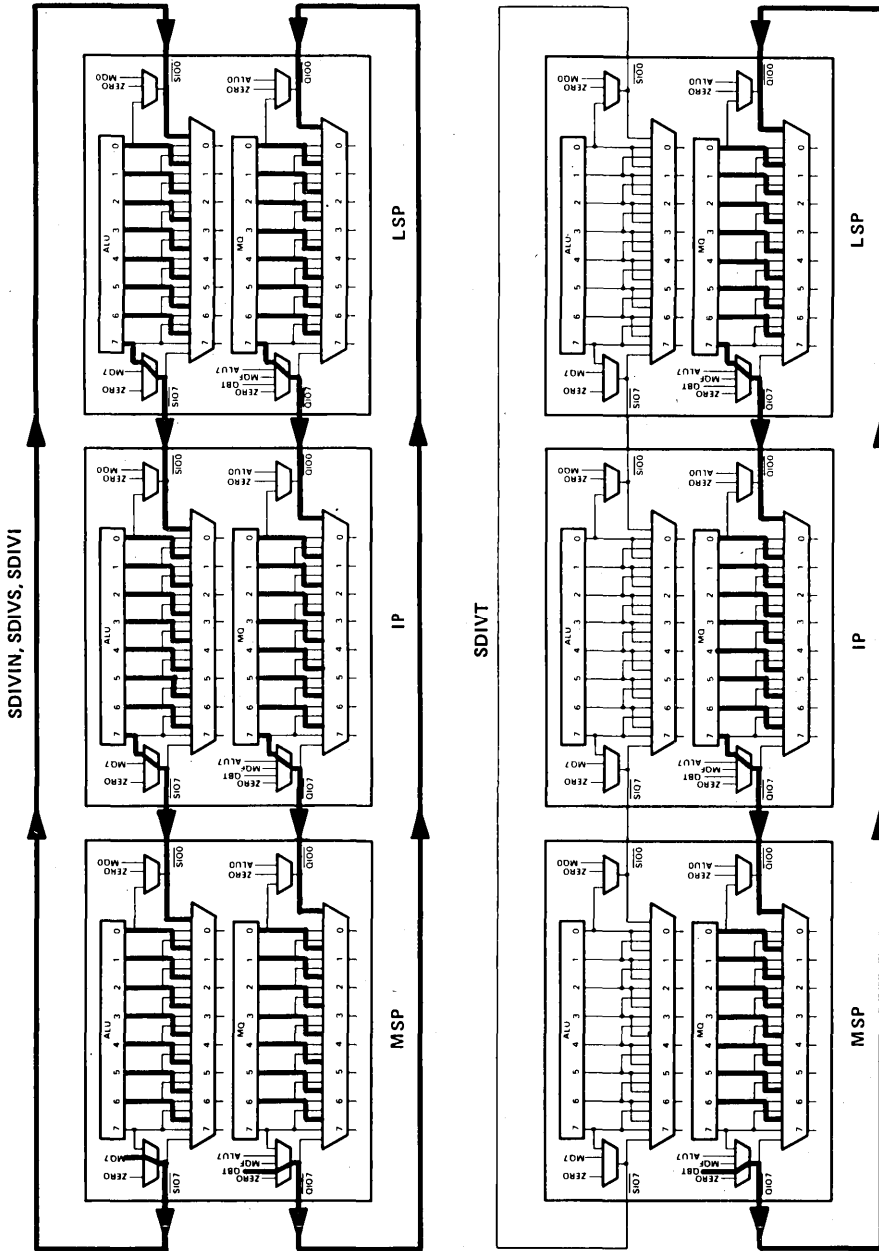


FIGURE 9. DIVIDE OPERATIONS

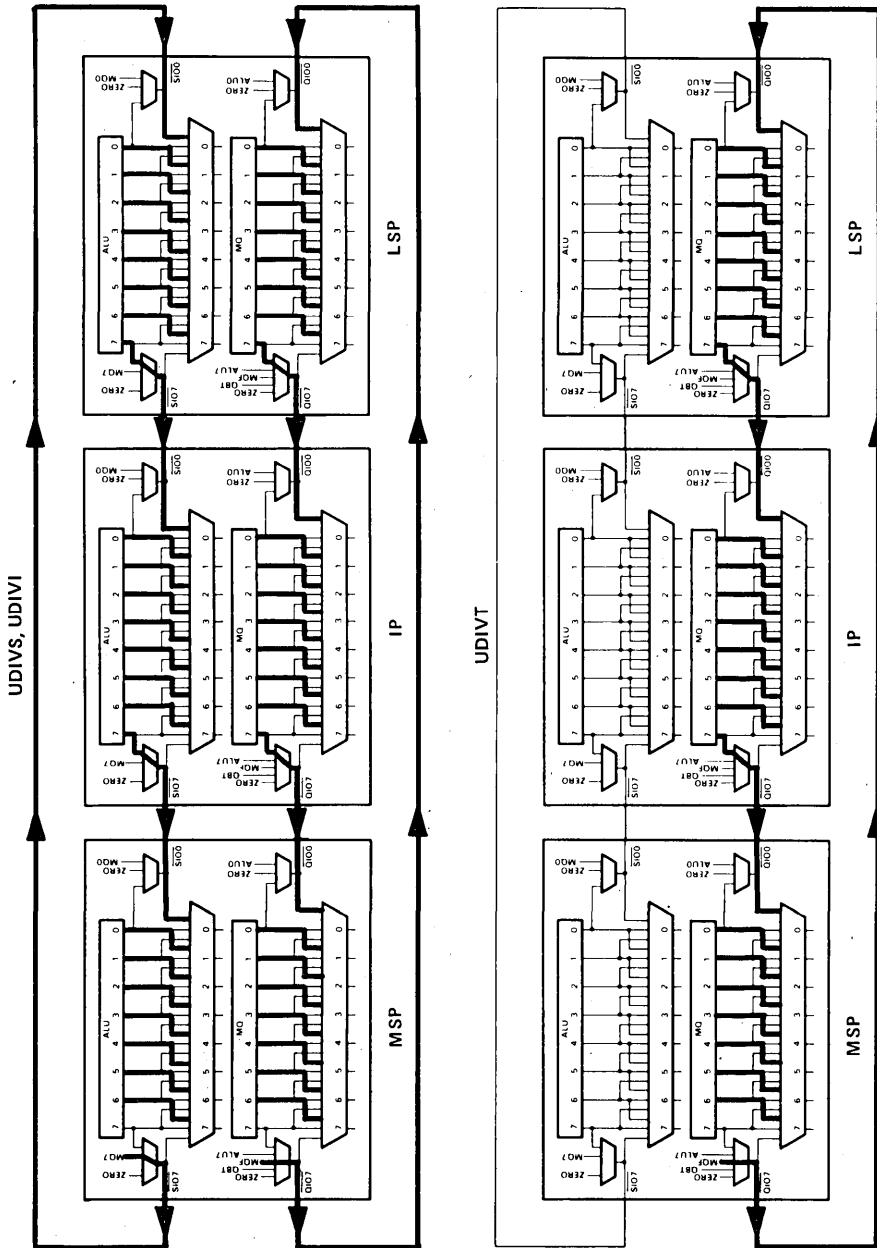


FIGURE 9. DIVIDE OPERATIONS (Continued)

SN54AS895, SN74AS895 8-BIT MEMORY ADDRESS GENERATORS

The unsigned divide iterate start (UDIVIS) instruction begins the iterate procedure while testing for overflow. Overflow is reported when the first subtraction of the divisor from the MSH of the dividend produces carry out. The test detects quotient overflow and divide by zero.

The unsigned divide iterate terminate (UDIVIT) instruction completes the iterate procedure generating the last quotient bit.

The signed divide initialize (SDIVIN) instruction prepares for iteration by shifting the dividend and storing the sign of the dividend for use in the following instructions and overflow tests.

The signed divide overflow test (SDIVO) checks for overflow possibilities. This instruction may be deleted from the divide operation if the OVR pin is ignored. If it is removed some overflow conditions will go undetected. \overline{WE} must be high (writing inhibited) when this instruction is used.

The signed divide iterate start (SDIVIS) instruction calculates the difference between the divisor and MSH of the dividend. Partial detection of overflow is also done during this instruction. Operations with like signs (positive quotient) and division by zero will overflow during this instruction (including zero divisor). Operations with unlike signs are tested for overflow during the signed divide quotient fix instruction (SDIVQF). Partial overflow results are saved and will be used during SDIVQF when overflow is reported.

The signed divide iterate (SDIVI) instruction forms the quotient and remainder through iterative subtract/add-shift operations of the divisor and dividend. One quotient bit is generated on each clock.

The signed divide iterate terminate (SDIVIT) instruction completes the iterate procedure, generating the last quotient bit. It also tests for a remainder equal to zero, which determines the action to be taken in the following correction (fix) instructions.

The divide remainder fix (DIVRF) instruction corrects the remainder. If a zero remainder was detected by the previous instructions, the remainder is forced to zero. For nonzero remainder cases where the remainder and dividend have the same sign, the remainder is correct. When the remainder and dividend have unlike signs, a correction add/subtract of the divisor to the remainder is performed.

The signed divide quotient fix (SDIVQF) instruction corrects the quotient if necessary. This correction requires adding one to the incorrect quotient. An incorrect quotient results if the signs of the divisor and dividend differ and the remainder is nonzero. An incorrect quotient also results if the sign of the divisor is negative and the remainder is zero.

Overflow detection is completed during this instruction. Overflow may be generated for differing signs of the dividend and divisor. The partial overflow test result performed during SDIVIS is ORed with this test result to produce a true overflow indication.

signed divide usage

The instructions necessary to perform an algebraically correct division of signed numbers are as follows:

Load MQ with the least significant half of the dividend

SDIVIN	S port = MSH of dividend R port = Divisor F port = Intermediate result
SDIVO	S port = Result of SDIVIN R port = Divisor F port = Test result (\overline{WE} must be high)
SDIVIS	S port = Result of SDIVIN R port = Divisor F port = Intermediate result

SDIVI (8N-2 times)	S port = Result of SDIVIS (or SDIVI) R port = Divisor F port = Intermediate result
SDIVIT	S port = Result of last SDIVI R port = Divisor F port = Intermediate result
DIVRF	S port = Result of SDIVIT R port = Divisor F port = Remainder
SDIVQF	S port = MQ register R port = Divisor F port = Quotient

The status of all signed divide instructions except SDIVIN, DIVRF, and SDIVQF is as follows:

N	→	Forced to zero
OVR	→	Forced to zero
C _{n+8}	→	Carry out equal to one
Z	→	Intermediate result is zero

The status of the SDIVIN instruction is as follows:

N	→	Forced to zero
OVR	→	Forced to zero
C _{n+8}	→	Forced to zero
Z	→	Divisor is zero

The status of the DIVRF instruction is as follows:

N	→	Forced to zero
OVR	→	Forced to zero
C _{n+8}	→	Carry out equal to one
Z	→	Remainder is zero

The status of the SDIVQF instruction is as follows:

N	→	Sign of quotient
OVR	→	Divide overflow
C _{n+8}	→	Carry out equal to one
Z	→	Quotient is zero

The quotient is stored in the MQ register and the remainder is stored in the register file location that originally held the most significant word of the dividend. If fractions are divided, the quotient must be shifted right one bit and the remainder right three bits to obtain the correct fractional representations.

The signed division algorithm is summarized in Table 7.

SN54AS895, SN74AS895
8-BIT MEMORY ADDRESS GENERATORS

TABLE 7. SIGNED DIVISION ALGORITHM

OP CODE	MNEMONIC	CLOCK CYCLES	INPUT S PORT	INPUT R PORT	OUTPUT F PORT
E4	LOADMQ	1	Dividend (LSH)	—	Dividend (LSH)
80	SDIVIN	1	Dividend (MSH)	Divisor	Remainder (N)
AF	SDIVO	1	Remainder (N)	Divisor	Test Result
90	SDIVIS	1	Remainder (N)	Divisor	Remainder (N)
A0	SDIVI	$8N - 2^\dagger$	Remainder (N)	Divisor	Remainder (N)
E0	SDIVIT	1	Remainder (N)	Divisor	Remainder (Unfixed)
40	DIVRF	1	Remainder (Unfixed)	Divisor	Remainder
50	SDIVQF	1	MQ Register	Divisor	Quotient

$^\dagger N$ = Number of cascaded packages.

unsigned divide usage

The instructions necessary to perform an algebraically correct division of unsigned numbers are as follows:

Load MQ with the least significant half of the dividend

UDIVIS	S port = MSH of dividend R port = Divisor F port = Intermediate result
UDIVI (8N-1 times)	S port = Result of UDIVIS (OR UDIVI) R port = Divisor F port = Intermediate result
UDIVIT	S port = Result of last UDIVI R port = Divisor F port = Remainder (unfixed)
DIVRF	S port = Result of UDIVIT R port = Divisor F port = Remainder

The status of all unsigned divide instructions except UDIVIS is as follows:

N	→ Forced to zero
OVR	→ Forced to zero
C_n+8	→ Carry out equal to one
Z	→ Intermediate result is zero

The status of the UDIVIS instruction is as follows:

N	→ Forced to zero
OVR	→ Divide overflow
C_n+8	→ Carry out equal to one
Z	→ Intermediate result is zero

If fractions are divided, the remainder must be shifted right two bits to obtain the correct fractional representation. The quotient is correct as is. The quotient is stored in the MQ register at the completion of the divide.

The unsigned division algorithm is summarized in Table 8.

TABLE 8. UNSIGNED DIVISION ALGORITHM

OP CODE	MNEMONIC	CLOCK CYCLES	INPUT S PORT	INPUT R PORT	OUTPUT F PORT
E4	LOADMQ	1	Dividend (LSH)	—	Dividend (LSH)
B0	UDIVIS	1	Dividend (MSH)	Divisor	Remainder (N)
C0	UDIVI	8N - 1†	Remainder (N)	Divisor	Remainder (N)
F0	UDIVIT	1	Remainder (N)	Divisor	Remainder (Unfixed)
40	DIVRF	1	Remainder (Unfixed)	Divisor	Remainder

† N = Number of cascaded packages.

group 5 instructions

Hex code F of Group 1 instructions is used to access Group 5 instructions. Group 5 instructions are summarized in Table 9.

TABLE 9. GROUP 5 INSTRUCTIONS

INSTRUCTION BITS (I7-I0) OP CODE (HEX)	MNEMONIC	FUNCTION
0F	CLR	Clear
1F	CLR	Clear
2F	CLR	Clear
3F	CLR	Clear
4F	CLR	Clear
5F	CLR	Clear
6F	CLR	Clear
7F	BCDBIN	BCD to Binary
8F	EX3BC	Excess-3 Byte Correction
9F	EX3C	Excess-3 Word Correction
AF	SDIVO	Signed Divide Overflow Check
BF	CLR	Clear
CF	CLR	Clear
DF	BINEX3	Binary to Excess-3
EF	CLR	Clear
FF	NOP	No Operation

clear instructions (CLR)

There are 11 clear instructions listed in Table 9. The instructions force the ALU output to be zero and the BCD flip-flops to be cleared. The status set by the clear instruction is as follows:

- N → None (force to zero)
- OVR → None (force to zero)
- C_n+8 → None (force to zero)
- Z → Active (one)

no operation instruction (NOP): I7-I0 = FF₁₆

This instruction is identical to the clear instructions except that the BCD flip-flops retain their old value.

2

LSI Devices

SN54AS895, SN74AS895 8-BIT MEMORY ADDRESS GENERATORS

excess-3 correction instructions (EX3BC, EX3C)

Two excess-3 correction instructions are available:

1. Excess-3 byte correction (EX3BC): $17-10 = 8F_{16}$
2. Excess-3 word correction (EX3C): $17-10 = 9F_{16}$

One instruction supports the byte mode and the other supports the word mode. These instructions correct the excess-3 additions (subtractions) in either the byte or word mode. For correct excess-3 arithmetic, this instruction must follow each add/subtract. The operand must be on the S port.

NOTE: The previous arithmetic overflow should be ignored.

The status of the EX3C instruction is as follows:

N	→	MSB of result
OVR	→	Signed overflow
C_{n+8}	→	Carry out equal one
Z	→	None (force to one)

The status of the EX3BC instruction is as follows:

N	→	None (force to zero)
OVR	→	Byte signed overflow
C_{n+8}	→	Carry out equal one
Z	→	None (force to one)

radix conversions

Conversions between decimal and binary number representations are performed with the aid of two special instructions: BINEX3 and BCDBIN. (Figure 10)

BCD to binary instructions (BCDBIN): $17-10 = 7F_{16}$

This instruction (Figure 11) allows the user to convert an N-digit BCD number to a 4N-bit binary number in $4(N-1)$ plus 8 clocks. This function sums the R bus, the S bus, and the C_n bit, performs an arithmetic left shift on the ALU result, and simultaneously circular shifts the MQ left. The status set by the BCD to binary instruction is as follows:

N	→	MSB of result
OVR	→	Signed arithmetic overflow†
C_{n+8}	→	Carry out equal one
Z	→	Result equal zero

† Overflow may be the result of an ALU operation or the arithmetic left shift operation.

The following code illustrates the BCD to binary conversion technique.

Let ACC be an accumulator register
 Let NUM be the register which contains the BCD number
 Let MSK be a mask register

M1:	LOADMQ NUM	; LOAD MQ WITH BCD NUMBER
M2:	SUB ACC, ACC, SLCMQ	; CLEAR ACC AND ALIGN MQ
M3:	SUB, MSK, MSK, SLCMQ	; CLEAR MSK AND ALIGN MQ
M4:	SLCMQ	; ALIGN
M5:	SLCMQ	; ALIGN
M6:	ADDI ACC, MSK, 15 ₁₀	; MSK = 15 ₁₀
		; REPEAT L1 THRU L4
		; N - 1 TIMES (N = number of
		; BCD digits)
L1:	AND MQ, MSK, R1, SLCMQ	; EXTRACT ONE DIGIT
		; ALIGN MQ
L2:	ADD, ACC, R1, R1, SLCMQ	; ACC + DIGIT
		; IS STORED IN R1
		; ALIGN MQ
L3:	BCDBIN, R1, R1, ACC	; 4 × (ACC + DIGIT)
		; IS STORED IN ACC
		; ALIGN MQ
L4:	BCDBIN, ACC, R1, ACC	; 10 × (ACC + DIGIT)
		; IS STORED IN ACC
		; ALIGN MQ
M7:	AND MQ, MSK, R1	; FETCH LAST DIGIT
M8:	ACC+R1 → ACC	; ADD IN LAST DIGIT

The previous code generates a binary number by executing the standard conversion formula for a BCD number (shown for 32 bits).

$$ABCD = [(A \times 10 + B) \times 10 + C] \times 10 + D$$

Notice that the conversion begins with the most significant BCD digit and that the addition is performed in radix 2.

binary to excess-3 instructions (BINEX3): I7-I0 = DF16

This instruction (Figure 12) allows the user to convert an N-bit binary number to an N/4-bit excess-3 number representation in 2N + 3 clocks. The data on the R and S ports are summed with the MSB of the MQ register. The MQ register is simultaneously shifted left circularly. The status set by the binary to excess-3 instruction is as follows:

N	→	MSB of result
OVR	→	Signed arithmetic overflow
C _{n+8}	→	Carry out equal one
Z	→	Result equal zero

SN54AS895, SN74AS895
8-BIT MEMORY ADDRESS GENERATORS

2

LSI Devices

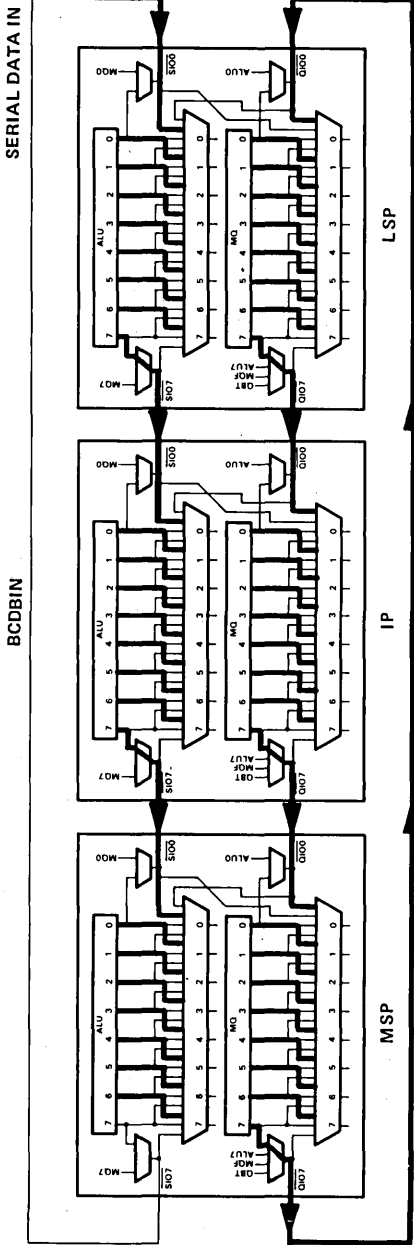


FIGURE 10. BCD TO BINARY

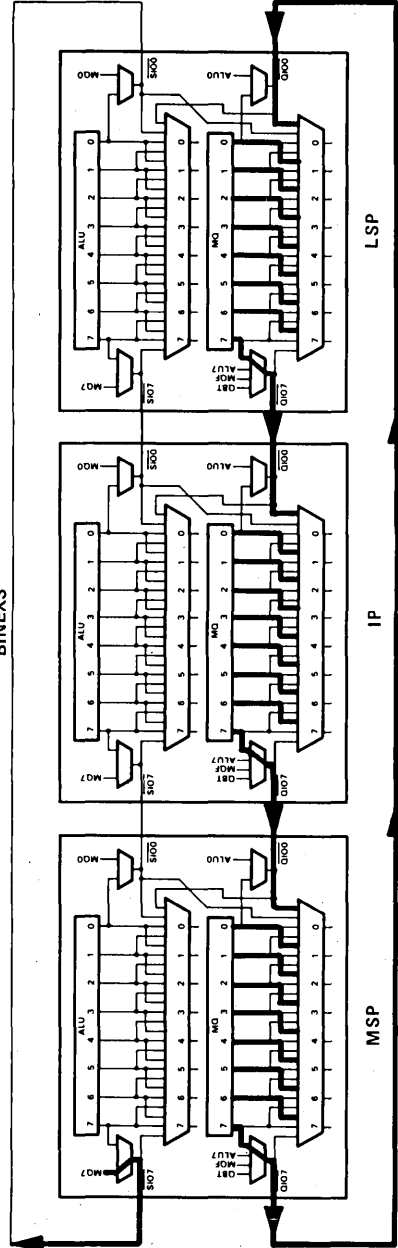


FIGURE 11. BINARY TO EXCESS-3

The following illustrates the binary to excess-3 conversion technique.

Let NUM be a register containing an unsigned binary number
Let ACC be an accumulator

```

M1:      LOADMQ NUM                ; LOAD MQ WITH BINARY
                                           ; NUMBER
M2:      CLEAR ACC                 ; CLEAR ACC
M3:      SET1 ACC H/33/            ; ACC → HEX/3333 . . .
L1:      BINEX3 ACC, ACC, ACC      ; DOUBLE ACC AND ADD IN
                                           ; MSB OF MQ
                                           ; ALIGN MQ
L2:      EX3C ACC, ACC             ; EXCESS 3 CORRECT
                                           ; REPEAT L1 AND L2
                                           ; N-1 TIMES
    
```

The previous code generates an excess-3 number by executing the standard conversion formula for a binary number.

$$a_n 2^n + a_{n-1} 2^{n-1} + a_{n-2} 2^{n-2} + \dots + a_0 2^0 = [(2a_n + a_{n-1})2 + a_{n-2}]2 + \dots + a_0$$

Notice that the conversion begins with the most significant binary bit and that the addition is performed in radix-10 (excess-3).

decimal arithmetic

Decimal numbers are represented in excess-3 code. Excess-3 code numbers may be generated by adding three to each digit of a Binary Coded Decimal (BCD) number. The hardware necessary to implement excess-3 arithmetic is only slightly different from binary arithmetic. Carries from one digit to another during addition in BCD occur when the sum of the two digits plus the carry-in is greater than or equal to ten. If both numbers are excess-3, the sum will be excess-6, which will produce the proper carries. Therefore, every addition or subtraction operation may use the binary adder. To convert the result from excess-6 to excess-3, one must consider two cases resulting from a BCD digit add: (1) where a carry-out is produced, and (2) where a carry-out is not produced. If a carry-out is not produced, three must be subtracted from the resulting digit. If a carry is produced, the digit is correct as a BCD number. For example, if BCD 5 is added to BCD 6, the excess-3 result would be $8 + 9 = 1$ (with a carry). A carry rolls the number through the illegal BCD representations into a correct BCD representation. Binary 3 must be added to digit positions that produce a carry-out to correct the result to an excess-3 representation. Every addition and subtraction instruction stores the carry generated from each 4-bit digit location for use by the excess-3 correction functions. These correction instructions (word or byte) must be executed in the clock cycle immediately after the addition or subtraction operation.

Signed numbers may be represented in ten's complement form by complementing the excess-3 number. As an example, add the decimal number -423 to the decimal number 24, which will be represented by 8AA and 357 in excess-3, respectively.

8AA	
357	
C01	Sum
011	Carry
934	Excess-3 correct
-6CC	Complement
-399	Excess-3 to decimal

Complements of excess-3 numbers may be generated by subtracting the excess-3 number from an excess-3 zero followed by an excess-3 correct.

SN54AS895, SN74AS895 8-BIT MEMORY ADDRESS GENERATORS

excess-3 to USASCII conversion

Input/output devices or files represent numbers differently than high-speed central processing units. I/O devices handle all alphanumeric data similarly. CPUs handle more numeric data than alphabetic data and store numeric data in packed form to minimize calculation throughout and reduce memory requirements. To represent the cost of a shirt that was \$10.96, the I/O device would handle the six USASCII characters "\$", "1", "0", ".", "9", "6", which would require 6 bytes of storage. In packed BCD, this number could be stored as 1096 in two bytes of data. The 'AS895 may be programmed to perform data format conversions such as converting excess-3 BCD to USASCII.

The code below converts a packed word of excess-3 BCD to two unpacked words of USASCII code. Instruction "MAIN1" reads the input word from memory into Register 0 (R0). For illustrative purposes, suppose this data was 43C9, which represents the \$10.96 shirt in excess-3 code. "MAIN2" and "MAIN3" generate a constant of 2D2D16, which is an offset constant to convert excess-3 numbers to USASCII. "MAIN4" copies R0 into R2 to set up the subroutine parameters and calls the subroutine "UNPACK", "UNPACK2" strips off the upper byte leaving 00C9 in R2. "UNPACK2" and "UNPACK3" together shift the contents of R2 one character position and places the result 0C90 into R3. "UNPACK4" performs a logical OR operation to produce OCD9 in register 2. "UNPACK5" clears the most significant nibble in each byte to produce 0C09 in R2. "UNPACK6" adds the constant 2D2D16 to R2 to produce 3936 the USASCII representation of the numerals 96 and returns program control to "MAIN5". "MAIN5" through "MAIN9" align the two remaining characters and call UNPACK and the process repeats. Finally the USASCII representation of 1096 is stored into memory. (Note that no attempt was made to pack the "\$" or "." characters.)

Unpacking Excess-3 to USASCII:

```

MAIN1:   READ, RFA(0)           ; READ IN PACKED EXCESS-3
MAIN2:   XOR, RFA(4), RFB(4), RFC(4) ; CLEAR R4
MAIN3:   SET1, RFB(40), RDC(2), RFA(D), ; GENERATE HEXADECIMAL
        MSH, LSH                ; 2D2D16
MAIN4:   MOVE, RFA(0), RFC(2), JSR(UNPACK) ; COPY RFA(0) INTO RFA(2),
        ; PROCEDURE CALL
MAIN5:   MOVE, RFA(2), RFC(1)     ; TWO CHARACTERS IN R1
MAIN6:   ADDR, RFB(0), RFA(0), RFC(0), SLC ; R0 SHIFTED 2
MAIN7:   ADDR, RFB(0), RFA(0), RFC(0), SLC ; R0 SHIFTED 4
MAIN8:   ADDR, RFB(0), RFA(0), RFC(0), SLC ; R0 SHIFTED 6
MAIN9:   ADDR, RFB(0), RFA(0), RFC(0), SLC ; R0 SHIFTED 8
        JSR (UNPACK)
MAIN10:  STORE, RFA(1)           ; STORE USASCII, TWO
        ; CHARACTERS IN R2
MAIN11:  STORE, RFA(2)           ; STORE USASCII
UNPACK1: SET0, RFB(2), RFC(F), MSH   ; CLEAR MSH
UNPACK2: ADDR, RFB(2), RFA(2), RFC(3), SLC ; SHIFT R2 TWO PLACES
UNPACK3: ADDR, RFB(3), RFA(3), RFC(3), SLC ; SHIFT R3 TWO PLACES
UNPACK4: OR, RFB(2), RFA(3), RFC(2) ; OR R3 TO R2
UNPACK5: SET0, RFB(2), RFC(F), RFA(0), LSH, MSH ; CLEAR MOST SIGNIFICANT 4
        ; BITS IN EACH BYTE
UNPACK6: ADDR, RFB(2), RFB(4), RFC(2), RTS ; ADD HEX 2D, RETURN
    
```

2

LSI Devices

SN54AS895, SN74AS895 8-BIT MEMORY ADDRESS GENERATORS

absolute maximum rating over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1}	7 V
Supply voltage, V_{CC2}	3 V
Input voltage	7 V
High-level voltage applied to 3-state outputs	5.5 V
Operating case temperature range: SN54AS895	-55°C to 125°C
Operating free-air temperature range: SN74AS895, SN74AS895-1	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54AS895			SN74AS895 SN74AS895-1			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC1}	I/O supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{CC2}	STL internal logic supply voltage	1.9	2	2.1	1.9	2	2.1	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage				0.8			V
I_{OH}	High-level output current				-1			-2.6 mA
I_{OL}	Low-level output current	All output except \bar{G} and ZERO			8			8 mA
		\bar{G}			16			16
		ZERO			48			48
T_C	Operating case temperature	-55			125			°C
T_A	Operating free-air temperature				0			70

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54AS895			SN74AS895 SN74AS895-1			UNIT
			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
V_{IK}		$V_{CC1} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$	-1.2			-1.2			V
V_{OH}	All outputs except ZERO	$V_{CC1} = 4.5 \text{ V to } 5.5 \text{ V}$, $I_{OH} = -0.4 \text{ mA}$	$V_{CC}-2$			$V_{CC}-2$			V
		$V_{CC1} = 4.5 \text{ V}$, $I_{OH} = -1 \text{ mA}$	2.4			2.4			
		$V_{CC1} = 4.5 \text{ V}$, $I_{OH} = -2.6 \text{ mA}$							
I_{OH}	ZERO	$V_{CC1} = 4.5 \text{ V}$, $V_{OH} = 5.5 \text{ V}$	0.1			0.1			mA
V_{OL}	All outputs except \bar{G} and ZERO	$V_{CC1} = 4.5 \text{ V}$, $I_{OL} = 8 \text{ mA}$	0.5			0.5			V
		$V_{CC1} = 4.5 \text{ V}$, $I_{OL} = 16 \text{ mA}$	0.5			0.5			
		$V_{CC1} = 4.5 \text{ V}$, $I_{OL} = 48 \text{ mA}$	0.5			0.5			
I_I	I/O	$V_{CC1} = 5.5 \text{ V}$, $V_I = 5.5 \text{ V}$	0.1			0.1			mA
	All others	$V_{CC1} = 5.5 \text{ V}$, $V_I = 7 \text{ V}$	0.1			0.1			
I_{IH}^{\ddagger}		$V_{CC1} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$	20			20			μA
I_{IL}^{\ddagger}		$V_{CC1} = 5.5 \text{ V}$, $V_I = 0.5 \text{ V}$	-0.4			-0.4			mA
I_O^{\S}		$V_{CC1} = 5.5 \text{ V}$, $V_O = 2.25 \text{ V}$	-30	-112	-30	-112	-112	mA	
I_{CC1}		$V_{CC1} = 5.5 \text{ V}$	150			130			mA
I_{CC2}		$V_{CC2} = 2.1 \text{ V}$	410			390			mA

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

[‡]For I/O ports, the parameters I_{IH} and I_{IL} include the off-state current.

[§]The output conditions have been chosen to produce a current that closely approximates one-half the true short-circuit current, I_{OS} .

2
LSI Devices

SN54AS895, SN74AS895 8-BIT MEMORY ADDRESS GENERATORS

SN54AS895 maximum switching characteristics, $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $T_C = -55^\circ\text{C to }125^\circ\text{C}$
(see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)										UNIT
		Y	C_{n+8}	\bar{G}, \bar{P}	Z^\dagger	N	OVR	DA	DB	$\bar{Q}\bar{I}\bar{O}$	$\bar{S}\bar{I}\bar{O}$	
t_{pd}	A3-A0 B3-B0	62	42	48	69	62	60	18	—	65	66	ns
	DA7-DA0, DB7-DB0	47	28	28	58	50	42	—	—	50	50	
	C_n	25	14	—	32	24	18	—	—	32	32	
	$\bar{E}\bar{A}$	54	32	35	62	52	52	—	—	58	58	
	$\bar{E}\bar{B}$	54	32	35	62	52	52	—	—	58	58	
	I7-I0	58	32	32	62	52	41	—	—	58	58	
	$\bar{O}\bar{E}\bar{B}$	—	—	—	—	—	—	—	14	—	—	
	$\bar{O}\bar{E}\bar{Y}$	14	—	—	—	—	—	—	—	—	—	
	$\bar{Q}\bar{I}\bar{O}$ (n) Shift	15	—	—	24	—	—	—	—	—	—	
	$\bar{S}\bar{I}\bar{O}$ (n) Shift	15	—	—	24	22	—	—	—	—	—	
	CK	68	60	56	62	50	68	38	30	70	70	
	$\bar{O}\bar{E}\bar{A}$	—	—	—	—	—	—	—	14	—	—	
	SSF ‡	—	—	—	—	—	—	14	—	—	—	

† Load resistor $R_1 = 100\ \Omega$.

‡ For byte instructions only.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN74AS895 maximum switching characteristics, $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $T_A = 0^\circ\text{C to }70^\circ\text{C}$ (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)										UNIT
		Y	C_{n+8}	\bar{G}, \bar{P}	Z^\dagger	N	OVR	DA	DB	$\bar{Q}\bar{I}\bar{O}$	$\bar{S}\bar{I}\bar{O}$	
t_{pd}	A3-A0 B3-B0	54	36	42	60	52	50	—	—	58	58	ns
	DA7-DA0, DB7-DB0	44	26	26	52	46	38	—	—	44	44	
	C_n	25	9	—	32	24	18	—	—	31	31	
	$\bar{E}\bar{A}$	49	29	29	58	49	47	—	—	54	54	
	$\bar{E}\bar{B}$	49	29	29	58	49	47	—	—	54	54	
	I7-I0	55	30	30	60	49	39	—	—	54	54	
	$\bar{O}\bar{E}\bar{B}$	—	—	—	—	—	—	—	12	—	—	
	$\bar{O}\bar{E}\bar{Y}$	12	—	—	—	—	—	—	—	—	—	
	$\bar{Q}\bar{I}\bar{O}$ (n) Shift	15	—	—	24	—	—	—	—	—	—	
	$\bar{S}\bar{I}\bar{O}$ (n) Shift	15	—	—	24	19	—	—	—	—	—	
	CK	58	55	52	61	52	62	35	25	60	60	
	$\bar{O}\bar{E}\bar{A}$	—	—	—	—	—	—	—	12	—	—	
	SSF ‡	—	—	—	—	—	—	12	—	—	—	

† Load resistor $R_1 = 100\ \Omega$.

‡ For byte instructions only.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54AS895, SN74AS895

8-BIT MEMORY ADDRESS GENERATORS

SN74AS895-1 maximum switching characteristics, $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $T_A = 0^\circ\text{C to }70^\circ\text{C}$ (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)										UNIT
		Y	C _{n+8}	\bar{G}, \bar{P}	Z [†]	N	OVR	DA	DB	$\bar{Q}10$	$\bar{S}10$	
t _{pd}	A3-A0 B3-B0	44	30	36	50	44	44	17	—	48	48	ns
	DA7-DA0, DB7-DB0	36	24	24	46	41	32	—	—	40	40	
	C _n	22	8	—	27	21	16	—	—	25	25	
	$\bar{E}A$	40	25	25	49	41	41	—	—	44	44	
	$\bar{E}B$	40	25	25	49	41	41	—	—	44	44	
	I7-I0	46	27	27	50	42	35	—	—	45	45	
	$\bar{O}E\bar{B}$	—	—	—	—	—	—	—	12	—	—	
	$\bar{O}E\bar{Y}$	12	—	—	—	—	—	—	—	—	—	
	$\bar{Q}10$ (n) Shift	14	—	—	20	—	—	—	—	—	—	
	$\bar{S}10$ (n) Shift	14	—	—	20	18	—	—	—	—	—	
	CK	50	46	46	50	50	50	30	22	50	50	
	$\bar{O}E\bar{A}$	—	—	—	—	—	—	—	12	—	—	
	SSF [‡]	—	—	—	—	—	—	12	—	—	—	

[†] Load resistor R1 = 100 Ω .

[‡] For byte instructions only.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

register file write setup and hold times

PARAMETER		SN54AS895		SN74AS895		SN74AS895-1		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{su}	C3-C0	8		7		6		ns
	DB [§]	14		12		11		
	I7-I4	16		14		13		
	I3-I0	24		22		21		
	$\bar{O}E\bar{Y}$	4		3		3		
	Y7-Y0	2		2		2		
	$\bar{W}E$	8		6		6		
	$\bar{Q}10$ (n), $\bar{S}10$ (n)	6		5		5		
t _h	SELY	8		6		6		ns
	C3-C0	0		0		0		
	DB [§]	0		0		0		
	I7-I4	0		0		0		
	I3-I0	0		0		0		
	$\bar{O}E\bar{Y}$	6		5		5		
	Y7-Y0	10		10		10		
	$\bar{W}E$	3		2		2		
$\bar{Q}10$ (n), $\bar{S}10$ (n)	0		0		0			
SELY	8		6		6			

[§]DB (during select instruction) through Y port.

2
LSI Devices

SN54AS895, SN74AS895 8-BIT MEMORY ADDRESS GENERATORS

special instruction switching characteristics

During various special instructions, the SSF pin is used to pass required information between the 'AS888 packages which make up a total system.

For instance, during the multiplication process, the LSB of the multiplier determines whether an ADD/SHIFT or SHIFT operation is performed. During multiplication, the SSF pin of the least significant package (LSP) becomes an output pin while all other packages become input pins.

Similarly, during normalization, the required operation depends on whether the two data MSBs are the same or different. Therefore, during normalization the SSF pin of the most significant package (MSP) becomes an output pin while all other packages become input pins.

Tables 10, 11, and 12 list the instructions which force the SSF pin during their execution. The propagation delay from various inputs is also shown. The parameter which limits normal system performance is indicated by a dagger.

TABLE 10. SN54AS895 SSF PIN DELAYS AND SETUP TIMES

MNEMONIC	HEX CODE	SSF SOURCE		INPUT → SSF (ns)				SSF SETUP TIME (ns)
		LSP	MSP	C _n	I _(n)	CK	B _(n)	
SNORM	20		X	—	29 [†]	46	—	20
DNORM	30		X	—	29	55	40 [†]	20
DIVRF	40		X	—	29 [†]	46	—	20
SDIVQF	50		X	—	26 [†]	—	—	18
SMULI	60	X		—	26 [†]	43	—	0
SDIVN	80		X	—	48	64	44 [†]	0
SDIVIS	90		X	26 [†]	51	64	55	0
SDIVI	A0		X	26 [†]	51	64	55	0
UDIVIS	B0		X	18 [†]	45	64	46	0
UDIVI	C0		X	18 [†]	50	54	40	0
UMULI	D0	X		—	25 [†]	48	—	0
SDIVIT	E0		X	26 [†]	50	56	54	0
ABS	48		X	—	34	62	39 [†]	20
SMTC	58		X	—	29	58	39 [†]	20
BINEX3	DF		X	—	29 [†]	58	—	18
LOADMQ (Arith)		X		23 [†]	34	62	40	0
LOADMQ (Log)		X		—	33	62	40 [†]	0
BADD	88			18 [†]	58	62	49	—
BSUBS	98			18 [†]	58	62	49	—
BSUBR	A8			18 [†]	58	71	49	—
BINCS	B8			18 [†]	58	60	49	—
BINCNS	C8			18 [†]	58	71	49	—
BXOR	D8			—	58	—	—	—
BAND	E8			—	58	—	—	—
BOR	F8			—	58	—	—	—
EX3BC	8F			—	58	46	49 [†]	—

[†]This parameter limits normal system performance.

SN54AS895, SN74AS895
8-BIT MEMORY ADDRESS GENERATORS

TABLE 11. SN74AS895 SSF PIN DELAYS AND SETUP TIMES

MNEMONIC	HEX CODE	SSF SOURCE		INPUT → SSF (ns)				SSF SETUP TIME (ns)
		LSP	MSP	C _n	I _(n)	CK	B _(n)	
SNORM	20		X	—	26 [†]	40	—	17
DNORM	30		X	—	26	52	37 [†]	17
DIVRF	40		X	—	26 [†]	40	—	17
SDIVQF	50		X	—	25 [†]	—	—	17
SMULI	60	X		—	25 [†]	40	—	0
SDIVIN	80		X	—	38	60	40 [†]	0
SDIVIS	90		X	24 [†]	48	60	52	0
SDIVI	A0		X	24 [†]	48	60	52	0
UDIVIS	B0		X	17 [†]	43	60	45	0
UDIVI	C0		X	17 [†]	44	52	37	0
UMULI	D0	X		—	26 [†]	40	—	0
SDIVIT	E0		X	25 [†]	46	52	49	0
ABS	48		X	—	32	60	38	17
SMTC	58		X	—	26	52	38 [†]	17
BINEX3	DF		X	—	26 [†]	40	—	17
LOADMQ (Arith)		X		22 [†]	32	50	38	0
LOADMQ (Log)		X		—	32	50	38 [†]	0
BADD	88			17 [†]	52	55	46	—
BSUBS	98			17 [†]	52	55	46	—
BSUBR	A8			17 [†]	52	62	46	—
BINCS	B8			17 [†]	52	55	46	—
BINCNS	C8			17 [†]	52	62	46	—
BXOR	D8			—	52	—	—	—
BAND	E8			—	52	—	—	—
BOR	F8			—	52	—	—	—
EX3BC	8F			—	45	45	46 [†]	—

[†]This parameter limits normal system performance.

2
LSI Devices

SN54AS895, SN74AS895
8-BIT MEMORY ADDRESS GENERATORS

TABLE 12. SN74AS895-1 SSF PIN DELAYS AND SETUP TIMES

MNEMONIC	HEX CODE	SSF SOURCE		INPUT → SSF (ns)				SSF SETUP TIME (ns)
		LSP	MSP	C _n	I _(n)	CK	B _(n)	
SNORM	20		X	—	23 [†]	28	—	14
DNORM	30		X	—	23	40	34 [†]	14
DIVRF	40		X	—	23 [†]	27	—	14
SDIVQF	50		X	—	23 [†]	—	—	14
SMULI	60	X		—	22 [†]	27	—	0
SDIVIN	80		X	—	35	46	35 [†]	0
SDIVIS	90		X	22 [†]	42	48	42	0
SDIVI	A0		X	22 [†]	42	46	42	0
UDIVIS	B0		X	16 [†]	42	46	38	0
UDIVI	C0		X	16 [†]	36	46	34	0
UMULI	D0	X		—	22 [†]	27	—	0
SDIVIT	E0		X	21 [†]	40	44	42	0
ABS	48		X	—	28	46	30 [†]	14
SMTC	58		X	—	24	44	30 [†]	14
BINEX3	DF		X	—	23 [†]	27	—	14
LOADMQ (Arith)		X		19 [†]	28	40	30	0
LOADMQ (Log)		X		—	28	35	30 [†]	0
BADD	88		↑	16 [†]	42	42	40	—
BSUBS	98			16 [†]	42	40	40	—
BSUBR	A8			16 [†]	42	50	40	—
BINCS	B8			16 [†]	42	46	40	—
BINCNS	C8			16 [†]	42	54	42	—
BXOR	D8		SIGNIFICANT	—	42	—	—	—
BAND	E8		BYTE	—	42	—	—	—
BOR	F8		SELECTED	—	42	—	—	—
EX3BC	8F		↓	—	42	42	42 [†]	—

[†]This parameter limits normal system performance.

SN54AS897A, SN74AS897A 16-BIT PARALLEL/SERIAL BARREL SHIFTERS

D2885, OCTOBER 1985—REVISED MARCH 1986

- High-Speed "Flash" Shift Operations
- Expandable to 32 Bits
- Hexadecimal and Binary Normalization with Leading Zero Detection
- Bit Reversal
- Merge Capabilities
- Texas Instruments Quality and Reliability

description

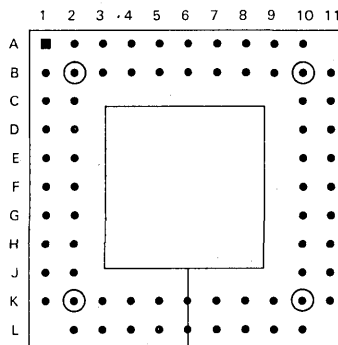
The SN54AS897A and SN74AS897A are multipurpose 16-bit barrel shifters in a 68-pin ceramic pin-grid-array package. The devices are capable of several different types of shift operations, as well as other more specialized functions such as hexadecimal and binary normalization, bit replacement, and leading-zero detection.

The unique feature of all barrel shifters is how the shift function is implemented. In conventional shift registers, shift operations are controlled by the number of input clock pulses applied. With barrel shifters, the desired number of positions to be shifted is determined by an input decoder. This form of implementation does not require an input clock and results in a shift operation that is restricted only by internal propagation delays. This delay is the same regardless of the number of positions to be shifted. The result is a high-speed "flash" type of shift.

The 'AS897A offers the system designer a much broader range of capabilities than previous conventional shift registers. Normalization of data in floating-point computations, bit-reversal when generating Fast Fourier Transform (FFT) addresses, and insertion of stop/start bits in asynchronous data communications are just a few of the applications that are possible with this device.

The 'AS897A can be operated as an 'AS897 by connecting the HEX/ $\overline{\text{BIN}}$ pin (J1) to ground.

SN54AS897A, SN74AS897A
GB PIN-GRID ARRAY PACKAGE
(TOP VIEW)



PIN ASSIGNMENT TABLE

PIN NO.	PIN NAME	PIN NO.	PIN NAME
A2	ZN1	F10	GND
A3	ZN2	F11	Y9
A4	ZN3	G1	D4
A5	GND	G2	GND
A6	$\overline{\text{NORM}}$	G10	Y11
A7	ZL	G11	Y8
A8	GND	H1	NC
A9	16B/ $\overline{32B}$	H2	D5
A10	OP	H10	GND
B1	D14	H11	Y7
B2	D13	J1	HEX/ $\overline{\text{BIN}}$
B3	D15	J2	D3
B4	ZN0	J10	GND
B5	VCC2	J11	GND
B6	ZN4	K1	D2
B7	IP	K2	D1
B8	VCC1	K3	VCC1
B9	GND	K4	M1
B10	S	K5	GND
B11	Y15	K6	CLK
C1	D12	K7	GND
C2	D9	K8	VCC2
C10	Y13	K9	Y6
C11	Y12	K10	Y4
D1	D11	K11	Y5
D2	D8	L2	D0
D10	NC	L3	M2
D11	GND	L4	M0
E1	D10	L5	TP
E2	D7	L6	$\overline{\text{OEY}}$
E10	Y14	L7	Y0
E11	Y10	L8	Y1
F1	GND	L9	Y2
F2	D6	L10	Y3

NC—No internal connection

Chip Carrier information available from factory upon request.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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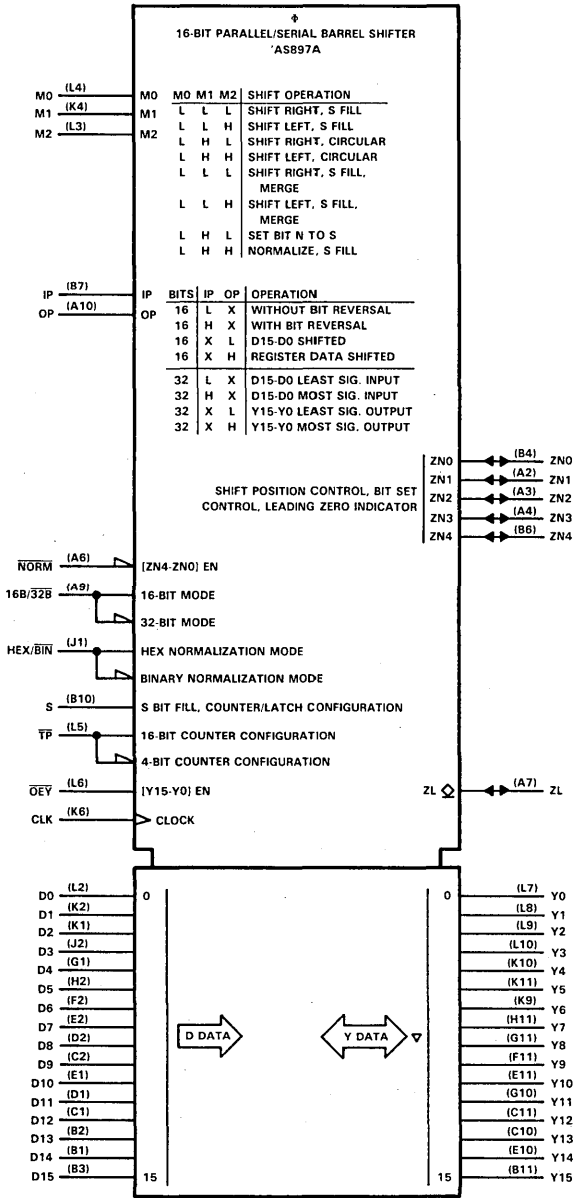
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2
LSI Devices

SN54AS897A, SN74AS897A
16-BIT PARALLEL/SERIAL BARREL SHIFTERS

logic symbol†



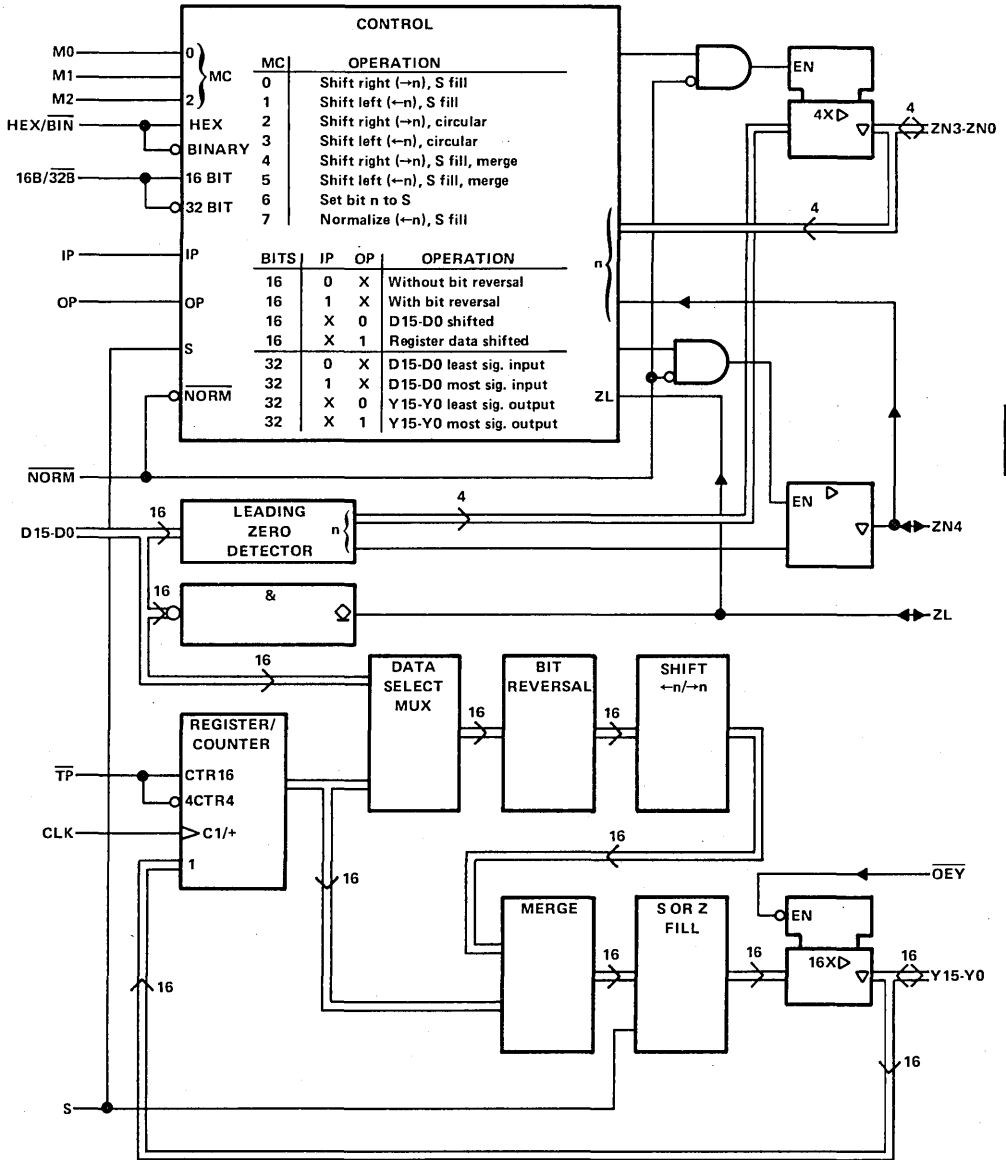
† This symbol is in accordance with ANSI/IEEE Std 91-1984.

2

LSI Devices

SN54AS897A, SN74AS897A
16-BIT PARALLEL/SERIAL BARREL SHIFTERS

functional block diagram (positive logic)



2

LSI Devices

SN54AS897A, SN74AS897A
16-BIT PARALLEL/SERIAL BARREL SHIFTERS

2 LSI Devices

PIN		I/O	DESCRIPTION
NAME	NO.		
16B/32B	A9	I	When high, 16-bit operation is selected. When low, 32-bit operation is selected.
CLK	K6	I	Clock input. Loads the internal register on the low-to-high transition. In 16-bit circular mode, acts as clock for the 16-bit/14-bit counter.
D0	L2	I	Input data bits 0 through 15
D1	K2	I	
D2	K1	I	
D3	J2	I	
D4	G1	I	
D5	H2	I	
D6	F2	I	
D7	E2	I	
D8	D2	I	
D9	C2	I	
D10	E1	I	
D11	D1	I	
D12	C1	I	
D13	B2	I	
D14	B1	I	
D15	B3	I	
GND	A5		Ground (All ground pins should be used)
GND	A8		
GND	B9		
GND	D11		
GND	F1		
GND	F10		
GND	G2		
GND	H10		
GND	J10		
GND	J11		
GND	K5		
GND	K7		
HEX/BIN	J1	I	Controls mode of operation for leading zero detector. When low, causes the number of leading binary zeros to be counted. When high, causes the number of binary zeros in leading hexadecimal groups (binary 0000s) to be counted. When tied to ground, causes the 'AS897A to operate as an 'AS897.
IP	B7	I	In the 16-bit mode, controls the bit-reversal option. A high logic level causes data selected by OP to be bit-reversed before it is passed to the shifter. When IP is low, data is passed unaltered. In the 32-bit mode, defines the data input position. When IP is high, D15-D0 are in the most significant input position. When IP is low, D15-D0 are in the least significant position.
M0	L4	I	Shift instruction control. Determine the type of shift operation to be performed. See Table 1 for further information.
M1	K4	I	
M2	L3	I	
NC	D10		No internal connection
NC	H1		
NORM	A6	I	A three-state control input for ZN4-ZN0 I/O ports used only in normalize instructions. When <u>NORM</u> is low, the number of leading zeros detected in the data present on D15-D0 is output on ZN4-ZN0. When <u>NORM</u> is high, ZN4-ZN0 act only as inputs.

SN54AS897A, SN74AS897A
16-BIT PARALLEL/SERIAL BARREL SHIFTERS

PIN		I/O	DESCRIPTION
NAME	NO.		
\overline{OEY}	L6	I	Control input for the Y15-Y0 I/O ports. When \overline{OEY} is low, the Y outputs are enabled.
OP	A10	I	In the 16-bit mode, controls the source of input data. A logic high on this input selects data from the register/counter. A low selects data on the D15-D0 inputs. In the 32-bit mode, defines the package output positions. When OP is high, Y15-Y0 are in the most significant output position. When OP is low, Y15-Y0 are in the least significant output position.
S	B10	I	Specifies the logic level that will fill the bit position or positions vacated during all shift operations except 16-bit circular. In the 16-bit circular mode, when S is high, the data latch operates as a 16-bit binary counter. When S is low, the register functions as a data latch.
\overline{TP}	L5	I	Functional testing input. When low, transforms the 16-bit counter into four 4-bit counters. During normal operation, \overline{TP} must be maintained at a high logic level.
VCC1	B8		5-volt supply for TTL-compatible I/O
VCC1	K3		
VCC2	B5		2-volt supply for internal Schottky Transistor Logic (STL)
VCC2	K8		
Y0	L7	I/O	Input/output bits 0-15. As an input, they load the data register. As an output, they present the shifted data.
Y1	L8	I/O	
Y2	L9	I/O	
Y3	L10	I/O	
Y4	K10	I/O	
Y5	K11	I/O	
Y6	K9	I/O	
Y7	H11	I/O	
Y8	G11	I/O	
Y9	F11	I/O	
Y10	E11	I/O	
Y11	G10	I/O	
Y12	C11	I/O	
Y13	C10	I/O	
Y14	E10	I/O	
Y15	B11	I/O	
ZL	A7	I/O	An input/open-collector output used primarily in 32-bit applications. When the input at D15-D0 is zero, the ZL output is high. The ZL outputs of cascaded packages are connected in a wired-AND configuration to detect if all inputs are zero. A recommended pull-up resistor of 200 to 680 Ω must be provided externally for proper operation in the 32-bit mode.
ZN0	B4	I/O	A four-bit code that performs the following functions in the 16-bit mode: 1. As an input in shift instructions, specifies how many bit positions are to be shifted. 2. As an input in replace instructions, specifies position of the bit to be replaced. 3. As an input to the normalize instruction, specifies the number of left shifts to be performed. 4. As an output from the normalize instruction, when $NORM = L$, specifies the number of leading zeros in the data on D15-D0.
ZN1	A2	I/O	
ZN2	A3	I/O	
ZN3	A4	I/O	
ZN4	B6	I/O	ZN4 is concatenated with ZN3-ZN0 for use in 32-bit shift operations as described above. In 16-bit normalization operations, ZN4 indicates when the input to the shifter is zero. In 16-bit left and right shifts and in shift and merge operations, a high on ZN4 causes all 16-bits to be filled with the logic level on the S input.

2

LSI Devices

SN54AS897A, SN74AS897A
16-BIT PARALLEL/SERIAL BARREL SHIFTERS

description (continued)

control block

The control block decodes the M2-M0 instruction inputs, 16B/32B configuration select, IP and OP data select/bit reversal options, and other control inputs and transmits the resulting control signals to the rest of the internal logic.

instruction set

The 'AS897A can operate in any of the eight user-programmable shift modes shown in Table 1. Selection of these instructions is controlled by pins M2-M0.

TABLE 1. INSTRUCTION SET

M2	M1	M0	DESCRIPTION
L	L	L	Shift right the number of bit positions defined by ZN3-ZN0 (16-bit mode) or ZN4-ZN0 (32-bit mode). Fill vacated bit positions with logic level on S input. A high on ZN4 causes all bits in the 16-bit mode to be filled with the logic level on S.
L	L	H	Shift left the number of bit positions defined by ZN3-ZN0 (16-bit mode) or ZN4-ZN0 (32-bit mode). Fill vacated bit positions with logic level on S input. A high on ZN4 causes all bits in the 16-bit mode to be filled with the logic level on S.
L	H	L	Circular right shift the number or bit positions defined by ZN3-ZN0 (16-bit mode) or ZN4-ZN0 (32-bit mode).
L	H	H	Circular left shift the number of bit positions defined by ZN3-ZN0 (16-bit mode) or ZN4-ZN0 (32-bit mode).
H	L	L	Shift right the number of bit positions defined by ZN3-ZN0 (16-bit mode) or ZN4-ZN0 (32-bit mode). Fill vacated bit positions with logic level on S input. Merge result with data from the register/counter. A high on ZN4 causes all bits in the 16-bit mode to be filled with the logic level on S.
H	L	H	Shift left the number of bit positions defined by ZN3-ZN0 (16-bit mode) or ZN4-ZN0 (32-bit mode). Fill vacated bit positions with logic level on S input. Merge result with data from the register/counter. A high on ZN4 causes all bits in the 16-bit mode to be filled with the logic level on S.
H	H	L	Set the bit position defined by ZN3-ZN0 (16-bit mode) or ZN4-ZN0 (32-bit mode) to the logic level on the S input.
H	H	H	If NORM is low, shift data left the number of bit positions defined by the leading-zero detector. Fill vacated bit positions with logic level on S input. Output number of leading zeros in D15-D0 on ZN3-ZN0 (16-bit mode) or ZN4-ZN0 (32-bit mode). Note: If NORM is high, this instruction performs like the left shift described above for M2 = L, M1 = L, M0 = H.

mode configuration

The 'AS897A can be configured to operate on 16-bit or 32-bit words. Configuration is controlled by 16B/32B. When 16B/32B is high, the 'AS897A operates in 16-bit mode.

Figure 1 illustrates the connection of four 'AS897As to provide a 32-bit barrel shifter that can perform all Table 1 shift instructions. For 32-bit mode operation, the 16B/32B inputs of all 'AS897A devices must be low and should be configured as shown in Figure 1.

2
LSI Devices

SN54AS897A, SN74AS897A
16-BIT PARALLEL/SERIAL BARREL SHIFTERS

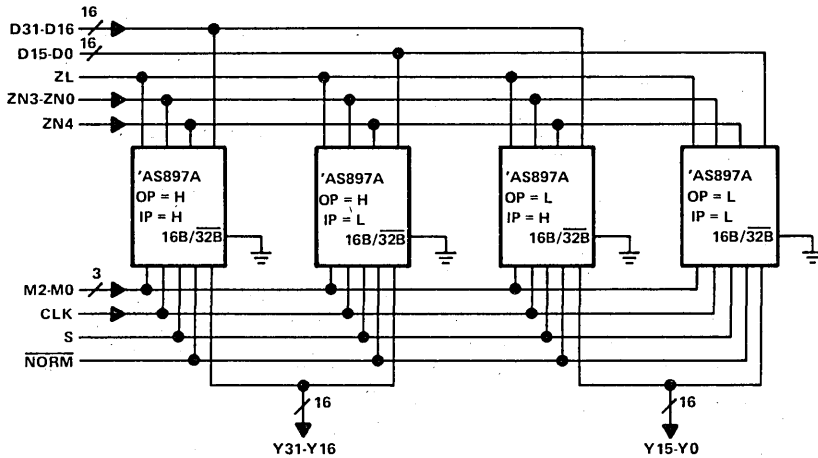


FIGURE 1. 32-BIT BARREL SHIFTER

2
LSI Devices

data input/output

Data can be input to the chip from two ports: D15-D0, which passes data to the zero detector and to the shifter via the data select and bit-reversal multiplexers, and Y15-Y0, which passes data to the register/counter. Y15-Y0 is also used to output the shift result from the chip.

Data input and output positions in the 32-bit mode are defined by IP and OP (see Table 2). When IP is high, the D15-D0 port is the most significant input position; when IP is low, the D15-D0 input port is the least significant. If OP is high, the Y15-Y0 port is the most significant output position; if OP is low, the Y15-Y0 port is the least significant position.

TABLE 2. IP AND OP CONTROLS

SIGNAL	16-BIT OPERATION (16B/32B = H)	32-BIT OPERATION (16B/32B = L)
IP = L	Bit-reversal option off	D15-D0 is least significant input position
IP = H	Bit-reversal option on	D15-D0 is most significant input position
OP = L	D15-D0 is shifted	Y15-Y0 is least significant output position
OP = H	Register/counter data is shifted	Y15-Y0 is most significant output position

zero detector

The zero detector detects the number of leading zeros at the D15-D0 input port. If $\overline{\text{HEX}/\text{BIN}}$ is high, the zero detector counts only those binary zeros that are part of a leading hexadecimal zero group. For example, given the binary number 0000 0000 0001 0001, the leading-zero count will be decimal 11 if $\overline{\text{HEX}/\text{BIN}}$ is low and decimal 8 if $\overline{\text{HEX}/\text{BIN}}$ is high.

If all zeros are detected at the D port, the ZL output transistor will be turned off. If the ZL output pin is pulled up through the recommended pull-up resistor (see pin description table), the resulting signal will be high. If anything other than a zero is detected on the D15-D0 inputs, the output transistor will be turned on; this will pull the ZL signal low.

SN54AS897A, SN74AS897A 16-BIT PARALLEL/SERIAL BARREL SHIFTERS

During data normalization ($M2 = H$, $M1 = H$, $M0 = H$), the zero-detector outputs the leading zero count to the ZN4-ZN0 I/O ports, provided \overline{NORM} is low. When \overline{NORM} is high, ZN4-ZN0 act only as inputs in this mode. For operations other than normalization, the state of \overline{NORM} is irrelevant.

In the data-normalization mode, a high logic level will be output on the ZN4 pin when the D15-D0 bus contains all lows and \overline{NORM} is low (see Table 3).

TABLE 3. ZN4 I/O PORT

SIGNAL	I/O	16-BIT CONFIGURATION (16B/32B = H)	32-BIT CONFIGURATION (16B/32B = L)
ZN4	I	In shift-left, shift-right, and shift-and-merge modes, a high fills all bits with the logic level on the S input. Inactive in other modes.	With ZN3-ZN0 indicates number of bits to be shifted in shift operations and position of bit to be replaced in replace-bit mode.
	O	In the normalization mode, when $\overline{NORM} = L$, indicates when the input to the shifter is zero	In the normalization mode, when $\overline{NORM} = L$, ZN4-ZN0 indicates number of leading zeros detected in D15-D0 and number of places to be shifted for normalization.

2

LSI Devices

data selector multiplexer

The data selector multiplexer is used only in 16-bit operation ($16B/\overline{32B} = H$). OP controls the mux and selects the data to be presented to the bit-reversal block. OP high selects the register/counter; OP low selects D15-D0 (see Table 2).

bit reversal

Bit reversal is also available only in the 16-bit mode ($16B/\overline{32B} = H$) and is controlled by IP (see Table 2). When the bit-reversal option is selected ($IP = H$), data selected by OP is bit-reversed before it is passed to the shifter: the most significant bit becomes the least significant bit, the second most significant bit becomes the second least significant bit, and so forth. When the bit-reversal option is off ($IP = L$), the data presented to the shifter is not altered.

register/counter

During most instructions, the register/counter operates as a data latch. Data on the Y15-Y0 bus is latched into the register/counter on the rising edge of the clock. Data can be input to the register/counter from the shifter ($\overline{OEY} = L$) or from the bidirectional Y port ($\overline{OEY} = H$).

In the 16-bit circular-shift mode ($16B/\overline{32B} = H$, $M2 = L$, $M1 = H$, $M0 = X$), the register counter will function as a 16-bit counter on the rising edge of the clock when S is high. Under these same conditions, the register/counter will function as four 4-bit counters when \overline{TP} is low. In the 16-bit circular-shift mode, the register/counter functions as a register when S is low. The counter option is not available for other instructions in the 16-bit mode or for any instructions in the 32-bit mode.

shifter

The shifter performs the operations specified by the M2-M0 inputs (see Table 1). The number of bits to be shifted or the position of the bit to be replaced is specified by ZN3-ZN0 (16-bit operation) or ZN4-ZN0 (32-bit operation).

SN54AS897A, SN74AS897A 16-BIT PARALLEL/SERIAL BARREL SHIFTERS

merge

During the shift and merge instruction ($M2 = H$, $M1 = L$, $M0 = X$), the merge block ORs the shift result with data from the register/counter.

S or Z fill

During bit replacement ($M2 = H$, $M1 = H$, $M0 = L$) in the 16-bit mode, this block sets the bit specified on the ZN3-ZN0 inputs with the logic level on the S input. This option works identically in the 32-bit mode, except that the bit to be replaced is specified on the Z4-Z0 inputs. During all other instructions except circular shifts, the S input specifies the logic level that will fill the bit position or positions vacated during the shift.

Z fill is used in the 32-bit mode to selectively put the device outputs in a high-impedance state. This feature is necessary to properly select the correct bit locations that will combine to form the shifted output. An example of a 32-bit circular shift four positions to the right, which illustrates the Z-fill technique, is shown in Figure 2.

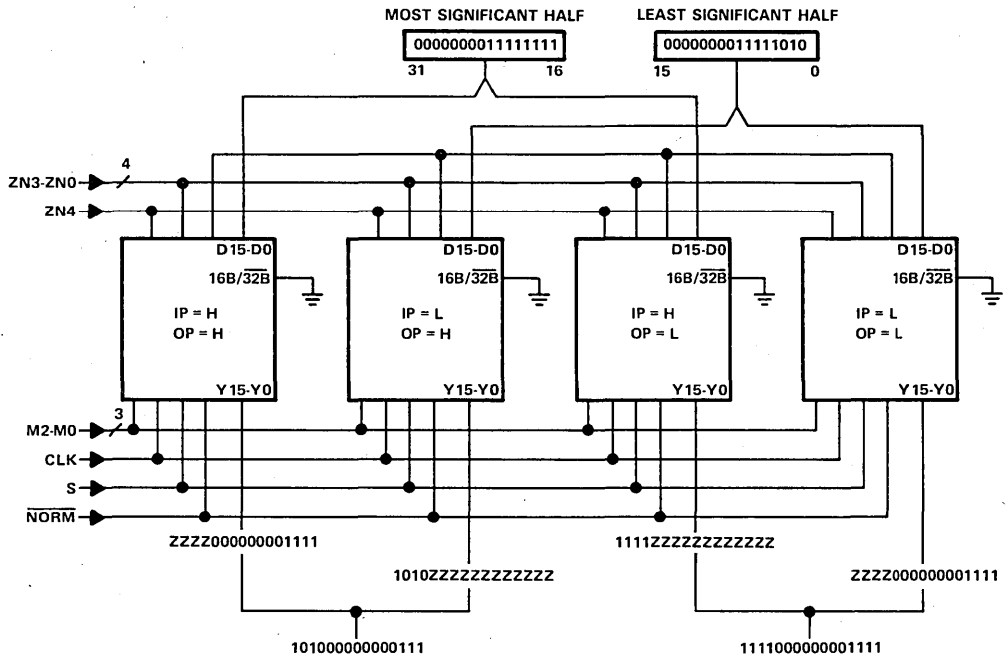


FIGURE 2. 32-BIT Z-FILL TECHNIQUE

SN54AS897A, SN74AS897A 16-BIT PARALLEL/SERIAL BARREL SHIFTERS

SHIFT OPERATION EXAMPLES

Examples of 'AS897A shift instructions are provided in the following paragraphs. Unless otherwise specified, the examples assume a 16-bit configuration.

shift left or right (M2 = L, M1 = L, M0 = X)

When in the shift-right (M0 = L) or shift-left (M0 = H) modes, ZN3-ZN0 define the number of bit positions to be shifted. If, for example, ZN3-ZN0 is equal to a decimal 10, the data selected by OP will be shifted 10 bit positions. The positions vacated during the shift operation are filled with the logic level being applied to the S input. NORM is inactive in all shift modes except normalization and is therefore shown as a don't care. If IP is high, the data selected by OP will be bit-reversed before it is passed to the shifter.

Example

Shift a 16-bit word on the data bus ten positions to the left and fill the least significant bits with highs.

CONTROL SIGNALS

SHIFT INSTRUCTION	NORMALIZE	NUMBER OF BITS TO SHIFT	BIT REVERSAL	DATA SOURCE	BIT FILL	CONFIGURATION
M2-M0	<u>NORM</u>	ZN4-ZN0	IP	OP	S	16B/32B
001	X	01010	0	0	1	1

Assume D15-D0 contains hex AF50:

D15-D0

Input Data 1010 1111 0101 0000

Y15-Y0

Result 0100 0011 1111 1111

Example

Shift a 32-bit word on the data bus 20 positions to the right. Fill vacated bit positions with highs.

CONTROL SIGNALS

SHIFT INSTRUCTION	NORMALIZE	NUMBER OF BITS TO SHIFT	BIT REVERSAL	DATA SOURCE	BIT FILL	CONFIGURATION
M2-M0	<u>NORM</u>	ZN4-ZN0	IP	OP	S	16B/32B
000	X	10100	See Figure 1		1	1

Assume D15-D0 contains hex 75BB FCAE:

D31-D16 D15-D0

Input Data 0111 0101 1011 1011 1111 1100 1010 1110

Y31-Y16 Y15-Y0

Result 1111 1111 1111 1111 1111 0111 0101 1011

2

LSI Devices

SN54AS897A, SN74AS897A 16-BIT PARALLEL/SERIAL BARREL SHIFTERS

2
LSI Devices

circular shift left or right (M2 = L, M1 = H, M0 = X)

In this mode, data selected by OP is circularly shifted left (M0 = H) or right (M0 = L) the number of bit positions specified by ZN3-ZN0. If, for example, the device is in the circular-shift-right mode (M0 = L) and ZN3-ZN0 contains a decimal five, the data selected by OP will be shifted right five positions.

In all shift modes except 16-bit circular, the S input contains the bit used for end fill or bit replacement. In the 16-bit circular-shift mode, the S input controls whether the register/counter will operate as a 16-bit counter or as a data register. When S is high, the register/counter operates as a 16-bit binary counter; when S is low, the register/counter operates as a 16-bit data latch. Both functions are controlled on the positive edge of the CLK input. Data on Y15-Y0 will be latched into the register/counter on the rising edge of the clock when S is low.

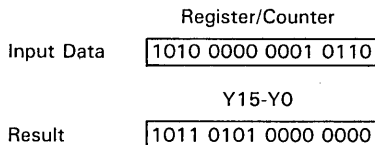
Example

Circular shift a 16-bit word in the register/counter five positions to the right.

CONTROL SIGNALS

SHIFT INSTRUCTION	NORMALIZE	NUMBER OF BITS TO SHIFT	BIT REVERSAL	DATA SOURCE	LATCH OR COUNTER	CONFIGURATION
M2-M0	NORM	ZN4-ZN0	IP	OP	S	16B/32B
010	X	X0101	0	1	0	1

Assume the register/counter contains hex A016:



shift and merge (M2 = H, M1 = L, M0 = X)

In the shift-and-merge mode, data selected by OP is shifted by OP is shifted left (M0 = H) or right (M0 = L) the number of positions specified by ZN3-ZN0, bit positions vacated by the shift are filled by the logic level on S, and the result is ORed with data in the register/counter.

Example

Shift data on the data bus six positions to the left, and fill vacated positions with zeros. Merge the shifted data with data from the data register.

CONTROL SIGNALS

SHIFT INSTRUCTION	NORMALIZE	NUMBER OF BITS TO SHIFT	BIT REVERSAL	DATA SOURCE	END FILL	CONFIGURATION
M2-M0	NORM	ZN4-ZN0	IP	OP	S	16B/32B
100	X	00110	0	0	0	1

**SN54AS897A, SN74AS897A
16-BIT PARALLEL/SERIAL BARREL SHIFTERS**

Assume D15-D0 contains hex 6174 and register/counter contains hex 320B:

D15-D0

Input Data 0110 0001 0111 0100

Shift Result

Intermediate Result 0101 1101 0000 0000

Register/Counter

Input Data 0011 0010 0000 1011

Y15-Y0

Result 0111 1111 0000 1011

bit replacement (M2 = H, M1 = H, M0 = L)

In the bit-replacement mode, data in the bit position specified by ZN3-ZN0 is replaced by the logic level on the S input. If, for example, ZN3-ZN0 contains a decimal seven and S contains a logic high, bit 7 of the data selected by OP will be set high regardless of its original state. In the following example, OP has been set high to select data from the register/counter. Because IP has been set high, the data will be bit-reversed before it enters the shifter..

Example

Bit-reverse the data in the register/counter and set bit 7 of the result to zero.

CONTROL SIGNALS

SHIFT INSTRUCTION	NORMALIZE	POSITION OF BIT TO BE INSERTED	BIT REVERSAL	DATA SOURCE	INSERT BIT	CONFIGURATION
M2-M0	NORM	ZN4-ZN0	IP	OP	S	16B/32B
110	X	X0111	1	1	0	1

Register/Counter

Input Data 0110 0001 0011 0100

Result after Bit-Reversal

Intermediate Result 0010 1100 1000 0110

Y15-Y0

Result 0010 1100 0000 0110

SN54AS897A, SN74AS897A 16-BIT PARALLEL/SERIAL BARREL SHIFTERS

2
LSI Devices

data normalization (M2 = H, M1 = H, M0 = L)

The data-normalization mode shifts data on D15-D0 to the left until a high logic level appears in the most-significant-bit position of output Y15-Y0 if $\overline{\text{HEX/BIN}}$ is low. If $\overline{\text{HEX/BIN}}$ is high, only 4-digit groups containing leading zeros are shifted left. The number of positions shifted to accomplish this is determined by the leading-zero detector. This count will be output on ZN3-ZN0 when the $\overline{\text{NORM}}$ input is low.

Since the leading-zero detector counts leading zeros in the D15-D0 input, the normalization is designed to operate on data from the data bus rather than the register/counter. Therefore OP is set low in the following example. The S input is programmed low so that all bit positions vacated during the shift will be filled with zeros.

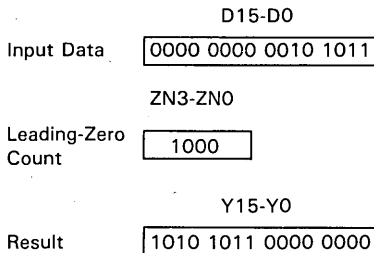
Example

Perform a hex normalization on a 16-bit data word from the data bus.

CONTROL SIGNALS

SHIFT INSTRUCTION	NORMALIZE	NUMBER OF BITS TO BE SHIFTED	LEADING-ZERO MODE	BIT REVERSAL	DATA SOURCE	INSERT BIT	CONFIGURATION
M2-M0	$\overline{\text{NORM}}$	ZN4-ZN0	HEX/ $\overline{\text{BIN}}$	IP	OP	S	16B/32B
111	0	Outputs leading zero count	1	0	0	0	1

Assume D15-D0 contains hex 002B:



Example

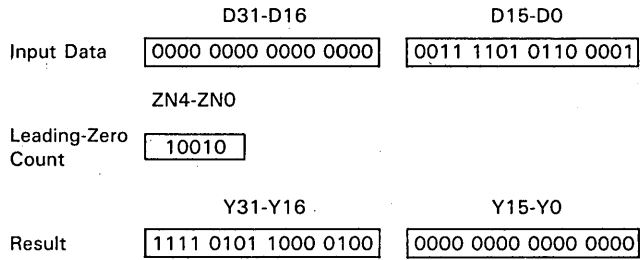
Perform a binary normalization on a 32-bit word from the data bus.

CONTROL SIGNALS

SHIFT INSTRUCTION	NORMALIZE	NUMBER OF BITS TO SHIFT	LEADING-ZERO MODE	BIT REVERSAL	DATA SOURCE	BIT FILL	CONFIGURATION
M2-M0	$\overline{\text{NORM}}$	ZN4-ZN0	HEX/ $\overline{\text{BIN}}$	IP	OP	S	16B/32B
111	0	Outputs leading zero count	0	See Figure 1		0	0

SN54AS897A, SN74AS897A 16-BIT PARALLEL/SERIAL BARREL SHIFTERS

Assume D31-D0 contains hex 0000 3D61:



IEEE floating-point normalization

Floating-point normalization is used to preserve number resolution after subtraction or some other floating-point algorithm that results in orders of magnitude reduction. Three 'AS897A devices can be configured to convert a 32-bit data word into the IEEE floating-point format shown in Figure 3.

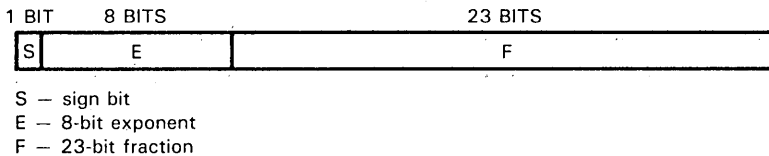


FIGURE 3. IEEE FLOATING-POINT FORMAT

2

LSI Devices

SN54AS897A, SN74AS897A 16-BIT PARALLEL/SERIAL BARREL SHIFTERS

Figure 4 shows the three-device configuration. The limitation of this application is that only 23 bits of the 32 bits are used in the significand, and the sign bit must be set from hardware. As an alternate to the IEEE floating-point format, the same hardware configuration can be used to normalize a 32-bit data word resulting in a 32-bit significand and a five-bit exponent.

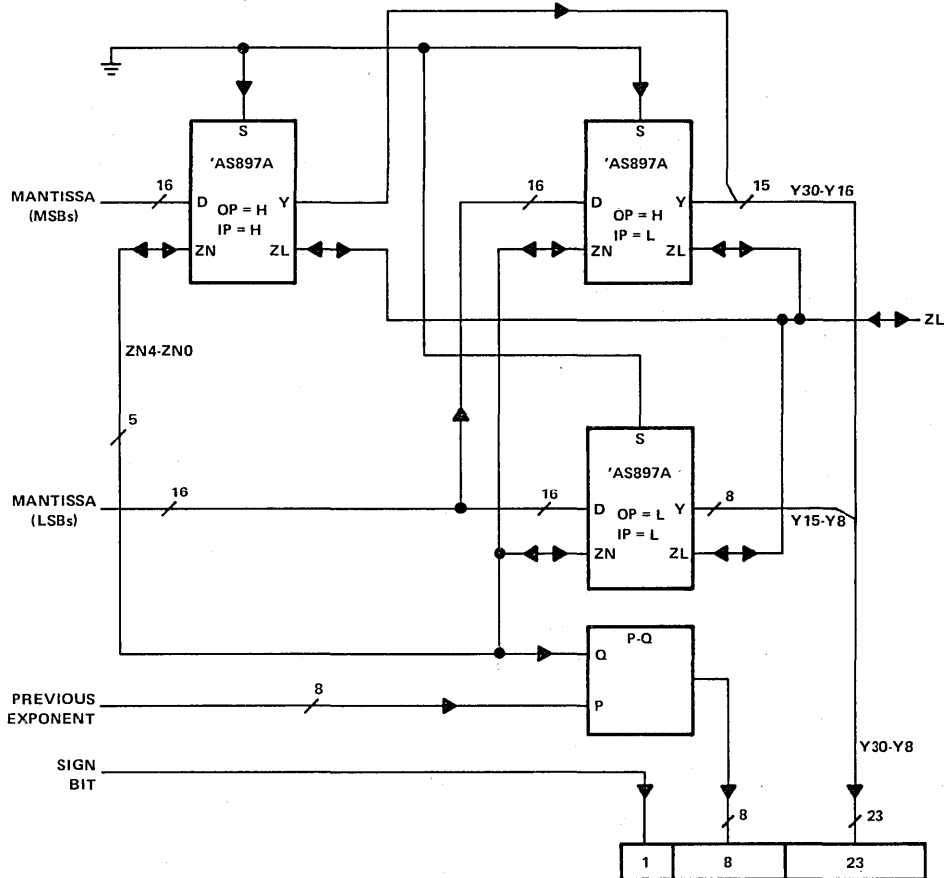


FIGURE 4. THREE-DEVICE CONFIGURATION FOR IEEE FLOATING-POINT FORMAT

2
LSI Devices

SN54AS897A, SN74AS897A
16-BIT PARALLEL/SERIAL BARREL SHIFTERS

Example

Input data in IEEE floating point format

Sign Bit	Previous Exponent	Mantissa
1	0010 1001	000 1001 0001 0001 0001 0001

Input mantissa concatenated with: 0 0000 0000 to D31-D0 of the 'AS897As

D31-D16	D15-D0
0001 0010 0010 0010	0010 0010 0000 0000

Normalize mantissa and output the leading zero count on ZN4-ZN0.

D31-D16	D15-D0	ZN4-ZN0
1001 0001 0001 0001	0001 0000 0000 0000	00011

Pack result in IEEE floating point format

Note: Exponent = old exponent - ZN4-ZN0

Sign Bit	Exponent	Mantissa
1	0010 0110	001 0001 0001 0001 0001 0000

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC1	7 V
Supply voltage, VCC2	3 V
Input voltage: I/O ports	5.5 V
All other inputs	7 V
Operating case temperature range: SN54AS897A	-55°C to 125°C
Operating free-air temperature range: SN74AS897A	0°C to 70°C
Storage temperature range	-65°C to 150°C

SN54AS897A, SN74AS897A 16-BIT PARALLEL/SERIAL BARREL SHIFTERS

recommended operating conditions

		SN54AS897A			SN74AS897A			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX		
V _{CC1}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
V _{CC2}	Supply voltage	1.9	2	2.1	1.9	2	2.1	V	
V _{IH}	High-level input voltage	2			2			V	
V _{IL}	Low-level input voltage	0.8			0.8			V	
V _{OH}	High-level output voltage	ZL	5.5			5.5			V
I _{OH}	High-level output current	ZN4-ZN0	-0.4			-0.4			mA
		Y15-Y0	-1			-2.6			
I _{OL}	Low-level output current	ZN4-ZN0	4			8			mA
		ZL, Y15-Y0	12			24			
t _w	Pulse duration	CLK low	10			10			ns
		CLK high	10			10			
t _{su}	Setup time before CLK†	Y15-Y0	10			10			ns
		S†	15			14			
		M0, M1, M2†	15			14			
		16B/32B‡	20			18			
t _h	Hold time after CLK†	Y15-Y0‡	2			2			ns
		S†	0			0			
		M0, M1, M2†	0			0			
		16B/32B‡	8			8			
T _A	Operating free-air temperature	-55			0			70	°C
T _C	Operating case temperature	125							°C

† These parameters only apply in the circular mode and with 16B/32B high.

‡ These parameters only apply in the circular mode.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS897A		SN74AS897A		UNIT
				MIN	TYP†	MAX	MIN	
V _{IK}		V _{CC} = 4.5 V,	I _I = 18 mA	-1.5		-1.5		V
I _{OH}	ZL	V _{CC} = 4.5 V,	V _{OH} = 5.5 V	0.1		0.1		mA
V _{OH}	All outputs	V _{CC} = 4.5 V to 5.5 V,	I _{OH} = -0.4 mA	V _{CC} - 2		V _{CC} - 2		V
	Y15-Y0	V _{CC} = 4.5 V,	I _{OH} = -1 mA	2.4	3.2			V
V _{OL}	ZN4-ZN0	V _{CC} = 4.5 V,	I _{OL} = 4 mA	0.25	0.4	0.25	0.4	V
		V _{CC} = 4.5 V,	I _{OL} = 8 mA			0.35	0.5	
	ZL, Y15-Y0	V _{CC} = 4.5 V,	I _{OL} = 12 mA	0.25	0.4	0.25	0.4	
		V _{CC} = 4.5 V,	I _{OL} = 24 mA			0.35	0.5	
I _I	I/O ports‡	V _{CC} = 5.5 V,	V _I = 5.5 V	0.1		0.1		mA
	All others	V _{CC} = 5.5 V,	V _I = 7 V	0.1		0.1		
I _{IH}	I/O ports‡	V _{CC} = 5.5 V,	V _I = 2.7 V	40		40		µmA
	All others			20		20		
I _{IL}	All inputs	V _{CC} = 5.5 V,	V _I = 0.4 V	-0.4		-0.4		mA
I _O §		V _{CC} = 5.5 V,	V _O = 2.25 V	-30	-112	-30	-112	mA
I _{CC1}		V _{CC} = 5.5 V,	See Note 1	100		90		mA
I _{CC2}		V _{CC} = 2.1 V,	See Note 1	180		170		mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the offstate output current.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

NOTE 1: Supply currents I_{CC1} and I_{CC2} are measured with M0, M1, M2, IP, OP, S, ZN3-ZN0, D15-D0, and OEY low; 16B/32B, NORM, and CLK high; and Y15-Y0, ZL, and ZN4 open.

2

LSI Devices

SN54AS897A, SN74AS897A
16-BIT PARALLEL/SERIAL BARREL SHIFTERS

switching characteristics over recommended operating temperature range

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω				UNIT
			SN54AS897A		SN74AS897A		
			MIN	MAX	MIN	MAX	
t _{pd}	D15-D0	Y15-Y0		37		33	ns
	S	Y15-Y0		20		17	
	ZN3-ZN0	Y15-Y0		24		22	
	IP	Y15-Y0		33		29	
	OP	Y15-Y0		33		29	
	M0, M1, M2	Y15-Y0		24		21	
	CLK [†]	Y15-Y0		47		42	
	D15-D0	ZL		28		27	
	D15-D0 [‡]	ZN4-ZN0		28		26	
t _{en}	M0, M1, M2 [§]	ZN4-ZN0		25		20	ns
	16B/32B	Y15-Y0		29		26	
	NORM [‡]	ZN3-ZN0		26		21	
	OEY	Y15-Y0		22		19	
	ZN4, ZL	Y15-Y0		32		29	
t _{dis}	M0, M1, M2 [§]	ZN4-ZN0		22		20	ns
	16B/32B	Y15-Y0		31		27	
	NORM [‡]	ZN3-ZN0		14		12	
	OEY	Y15-Y0		10		9	
	ZN4, ZL	Y15-Y0		30		26	

[†] This parameter applies only to the circular mode with S high and OP high.

[‡] These parameters apply only to the normalization mode.

[§] These parameters apply only to the 32-bit mode (16B/32B = L).

2

LSI Devices

- Serial-to-Parallel and Parallel-to-Serial Conversions
- Parallel I/O Registers
- Data Exchangeable Between I/O Register and Shift Register
- Choice of Synchronous and/or Asynchronous Clear
- Independent or Dual Register Clocking
- Functionally Similar to National Semiconductor DM74LS962
- Dependable Texas Instruments Quality and Reliability

description

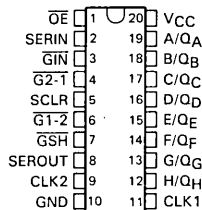
The 'ALS963 and 'ALS964 each contain an 8-bit shift register in parallel with an 8-bit I/O register. In addition to serial-to-parallel and parallel-to-serial conversions, these devices are capable of exchanging data between the shift and I/O registers. Control lines determine the mode of operation as shown in the function table.

The 'ALS963 features individual shift and I/O register clock inputs whereas the 'ALS964 features simultaneous register clocking through a single clock input. Clocking in both cases is achieved by positive transitions at the clock inputs.

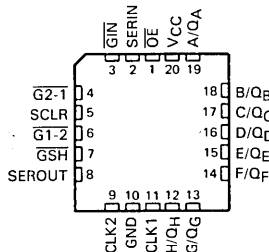
The clear function for the 'ALS963 is synchronous (active high). The 'ALS964 features active-high synchronous and asynchronous clearing.

The SN54ALS963 and SN54ALS964 are characterized for operation over the full military of -55°C to 125°C. The SN74ALS963 and SN74ALS964 are characterized for operation from 0°C to 70°C.

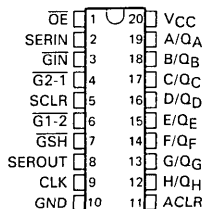
SN54ALS963 . . . JT PACKAGE
SN74ALS963 . . . DW OR NT PACKAGE
(TOP VIEW)



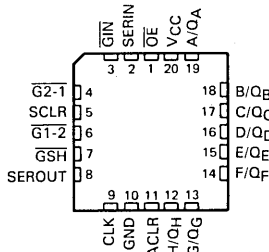
SN54ALS963 . . . FK PACKAGE
SN74ALS963 . . . FN PACKAGE
(TOP VIEW)



SN54ALS964 . . . JT PACKAGE
SN74ALS964 . . . DW OR NT PACKAGE
(TOP VIEW)



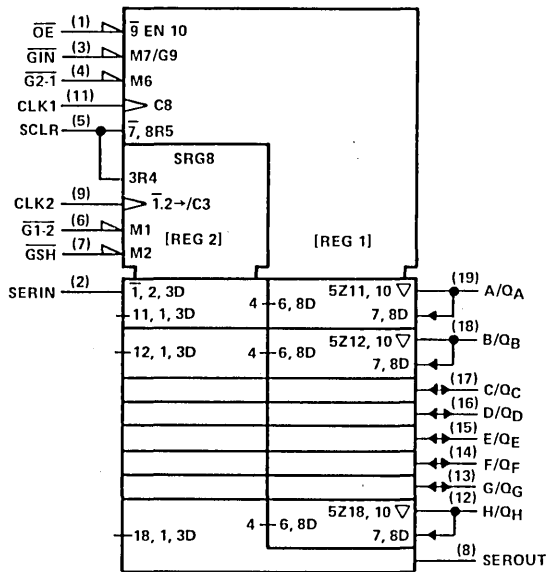
SN54ALS964 . . . FK PACKAGE
SN74ALS964 . . . FN PACKAGE
(TOP VIEW)



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LSI Devices

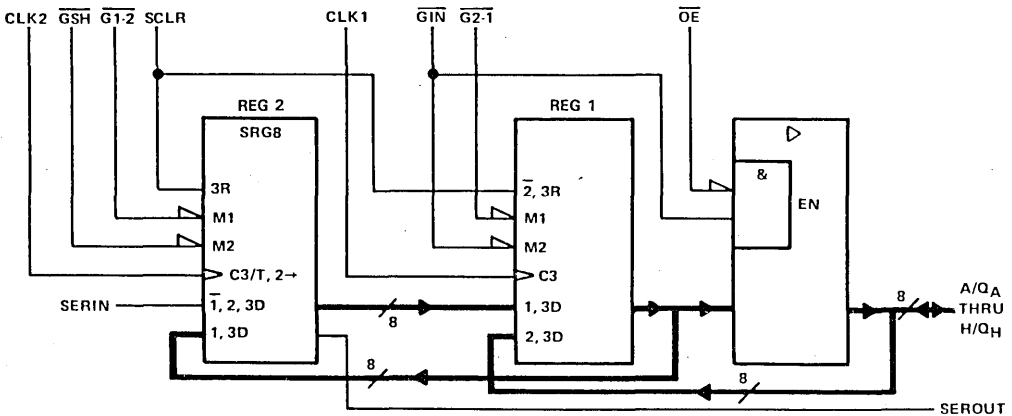
SN54ALS963, SN74ALS963
DUAL-RANK 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUTS

'ALS963 logic symbol†



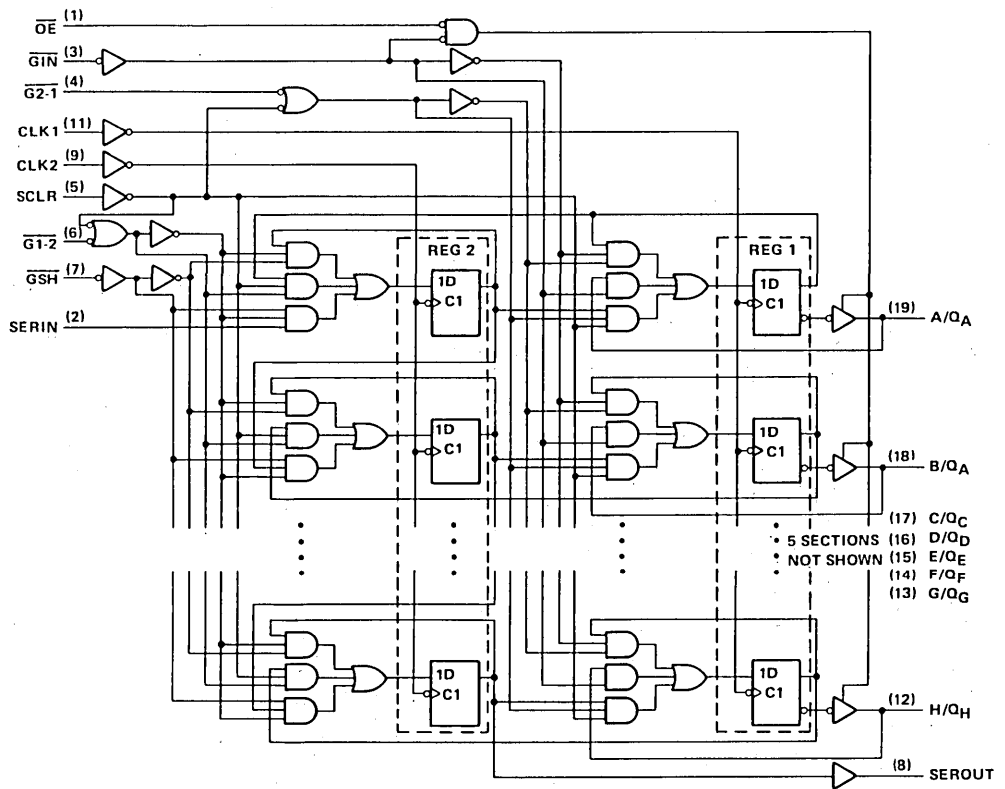
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'ALS963 register-level logic diagram



SN54ALS963, SN74ALS963
 DUAL-RANK 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUTS

'ALS963 gate-level logic diagram (positive logic)



2
 LSI Devices

SN54ALS963, SN74ALS963
DUAL-RANK 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUTS

ALS963
 FUNCTION TABLE

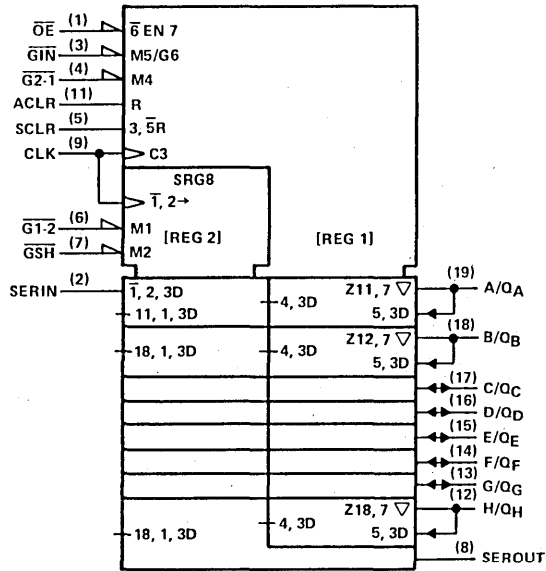
INPUTS								A/QA THROUGH H/QH	OPERATION OR FUNCTION
OE	GIN	GE-1	G1-2	GSH	CLK1	CLK2	SCLR		
H	H	H	H	H	X	X	L	HI-Z	All data stable
L	H	H	H	H	X	X	L	OUTPUT	All data stable
X	L	H	H	H	↑	X	L	INPUT	Enter data from I/O into Reg 1
H	H	L	H	H	↑	X	L	HI-Z	Copy data from Reg 2 to Reg 1
L	H	L	H	H	↑	X	L	OUTPUT	Copy data from Reg 2 to Reg 1
X	L	L	H	H	↑	↑	L	INPUT	Reg 1 ORs data from Reg 2 and I/O
H	H	H	L	X	X	↑	L	HI-Z	Copy data from Reg 1 to Reg 2
L	H	H	L	X	X	↑	L	OUTPUT	Copy data from Reg 1 to Reg 2
X	L	H	L	X	↑	↑	L	INPUT	Copy data from Reg 1 to Reg 2, enter new data from I/O into Reg 1
H	H	L	L	X	↑	↑	L	HI-Z	Exchange data between registers
L	H	L	L	X	↑	↑	L	OUTPUT	Exchange data between registers
X	L	L	L	X	↑	↑	L	INPUT	Copy data from Reg 1 to Reg 2, Reg 1 ORs data from Reg 2 and I/O
H	H	H	H	L	X	↑	L	HI-Z	Shift data in Reg 2
L	H	H	H	L	X	↑	L	OUTPUT	Shift data in Reg 2
X	L	H	H	L	↑	↑	L	INPUT	Shift data in Reg 2, enter new data from I/O into Reg 1
H	H	L	H	L	↑	↑	L	HI-Z	Copy data from Reg 2 to Reg 1, shift data in Reg 2
L	H	L	H	L	↑	↑	L	OUTPUT	Copy data from Reg 2 to Reg 1, shift data in Reg 2
X	L	L	H	L	↑	↑	L	INPUT	Reg 1 ORs data from Reg 2 and I/O, shift data in Reg 2
X	H	X	X	X	↑	X	H		Synchronously clear Reg 1
X	X	X	X	X	X	↑	H		Synchronously clear Reg 2
X	H	X	X	X	↑	↑	H		Synchronously clear both registers
X	L	X	X	X	↑	↑	H	INPUT	Enter data from I/O into Reg 1 and synchronously clear Reg 2
X	L	X	X	X	↑	X	H	INPUT	Enter data from I/O into Reg 1

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LSI Devices

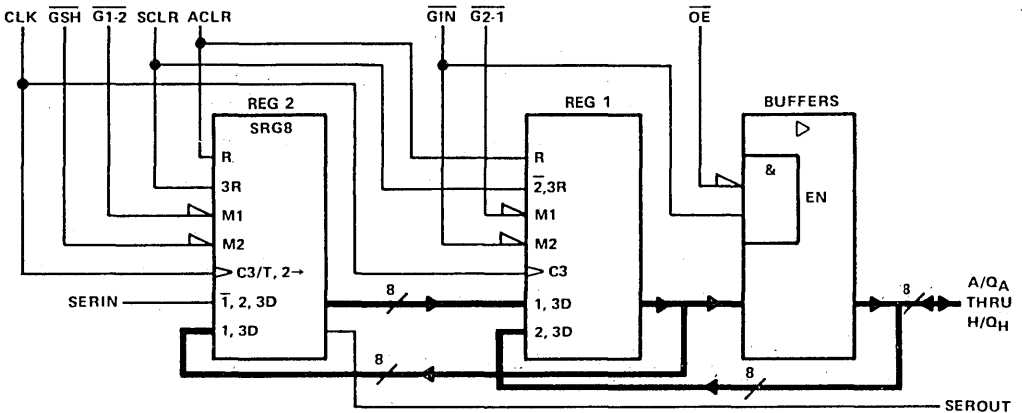
SN54ALS964, SN74ALS964
DUAL-RANK 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUTS

†ALS964 logic symbol†



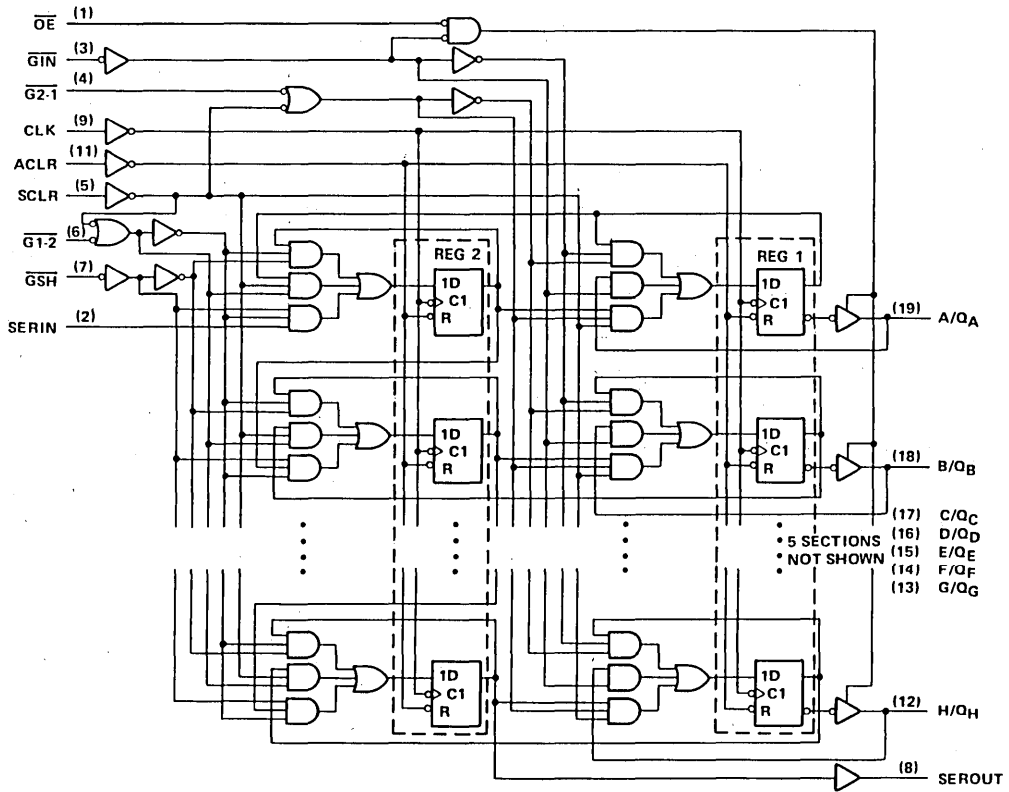
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

†ALS964 register-level logic diagram



SN54ALS964, SN74ALS964
DUAL-RANK 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUTS

'ALS964 gate-level logic diagram (positive logic)



2

LSI Devices

SN54ALS964, SN74ALS964
DUAL-RANK 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUTS

ALS964
 FUNCTION TABLE

INPUTS								A/QA THROUGH H/QH	OPERATION OR FUNCTION
OE	G1N	G2-T	G1-2	GSH	CLK	ACLR	SCLR		
H	H	H	H	H	X	L	L	HI-Z	All data stable
L	H	H	H	H	X	L	L	OUTPUT	All data stable
X	L	H	H	H	↑	L	L	INPUT	Enter data from I/O into Reg 1
H	H	L	H	H	↑	L	L	HI-Z	Copy data from Reg 2 to Reg 1
L	H	L	H	H	↑	L	L	OUTPUT	Copy data from Reg 2 to Reg 1
X	L	L	H	H	↑	L	L	INPUT	Reg 1 ORs data from Reg 2 and I/O
H	H	H	L	X	↑	L	L	HI-Z	Copy data from Reg 1 to Reg 2
L	H	H	L	X	↑	L	L	OUTPUT	Copy data from Reg 1 to Reg 2
X	L	H	L	X	↑	L	L	INPUT	Copy data from Reg 1 to Reg 2, enter new data from I/O into Reg 1
H	H	L	L	X	↑	L	L	HI-Z	Exchange data between registers
L	H	L	L	X	↑	L	L	OUTPUT	Exchange data between registers
X	L	L	L	X	↑	L	L	INPUT	Copy data from Reg 1 to Reg 2, Reg 1 ORs data from Reg 2 and I/O
H	H	H	H	L	↑	L	L	HI-Z	Shift data in Reg 2
L	H	H	H	L	↑	L	L	OUTPUT	Shift data in Reg 2
X	L	H	H	L	↑	L	L	INPUT	Shift data in Reg 2, enter new data from I/O into Reg 1
H	H	L	H	L	↑	L	L	HI-Z	Copy data from Reg 2 to Reg 1, shift data in Reg 2
L	H	L	H	L	↑	L	L	OUTPUT	Copy data from Reg 2 to Reg 1, shift data in Reg 2
X	L	L	H	L	↑	L	L	INPUT	Reg 1 ORs data from Reg 2 and I/O, shift data in Reg 2
X	H	X	X	X	↑	L	H	INPUT	Synchronously clear Reg 1 and Reg 2
X	X	X	X	X	X	H	X		Asynchronously clear Reg 1 and Reg 2
X	L	X	X	X	↑	L	H		Enter data from I/O into Reg 1 and synchronously clear Reg 2

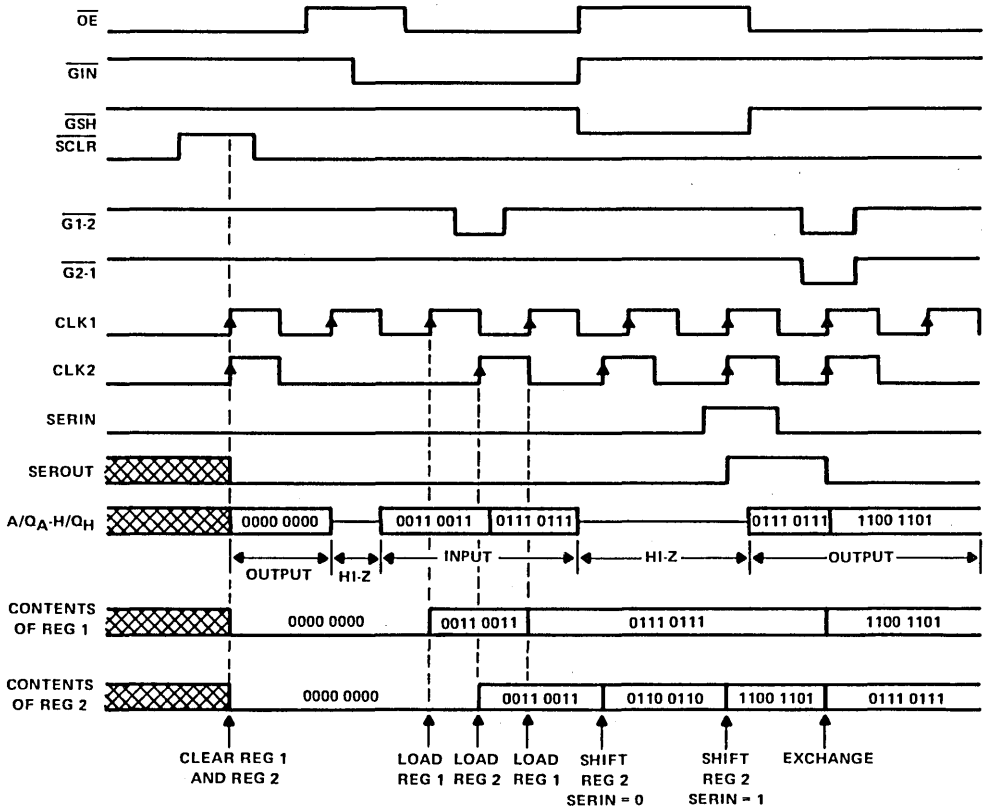
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LSI Devices

SN54ALS963, SN74ALS963 DUAL-RANK 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUTS

'ALS963 typical sequence

Illustrated below is the following sequence:

1. Clear both registers to zero.
2. Input 0011 0011 in Reg 1.
3. Transfer 0011 0011 from Reg 1 to Reg 2.
4. Input 0111 0111 into Reg 1.
5. Shift contents of Reg 2, SERIN = 0
6. Shift contents of Reg 2, SERIN = 1
7. Exchange contents of Reg 1 with Reg 2.

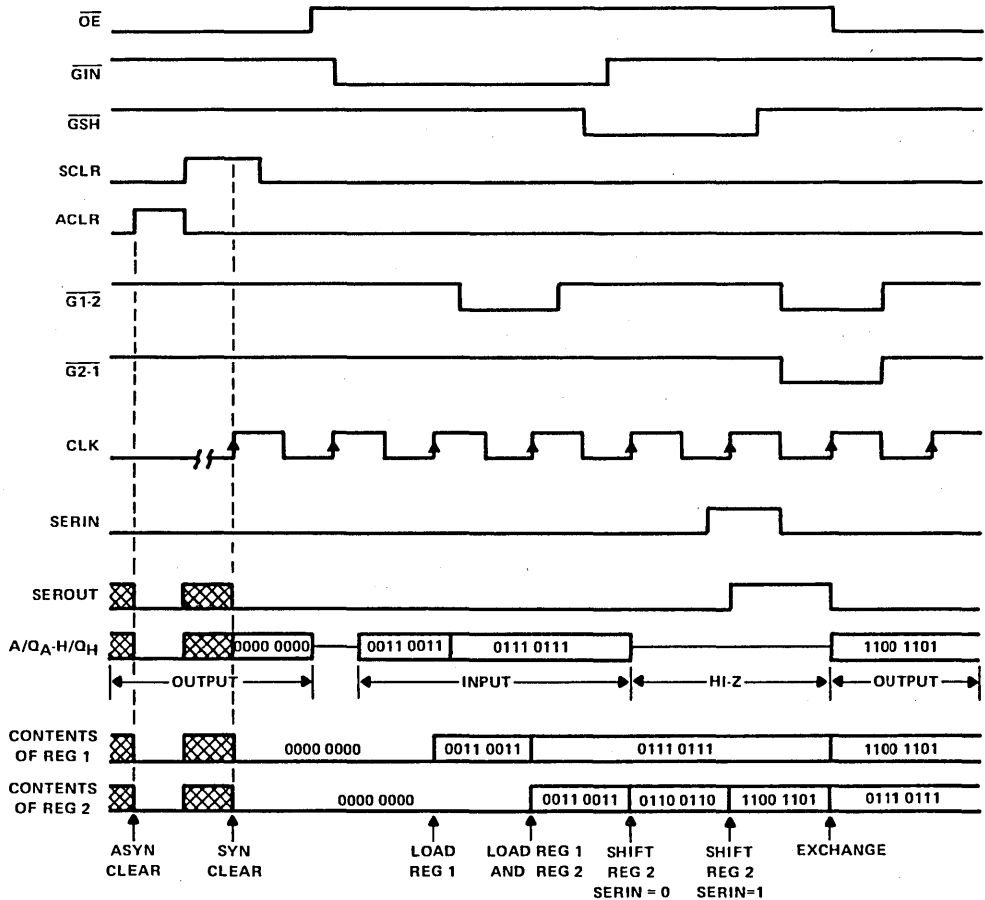


SN54ALS964, SN74ALS964 DUAL-RANK 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUTS

ALS964 typical sequence

Illustrated below is the following sequence:

1. Asynchronously clear Reg 1 and Reg 2 to zero, operate, then synchronously clear.
2. Input 0011 0011 into Reg 1.
3. Transfer 0011 0011 from Reg 1 to Reg 2 and input 0111 0111 into Reg 1.
4. Shift contents of Reg 2, SERIN = 0
5. Shift contents of Reg 2, SERIN = 1
6. Exchange contents of Reg 1 with Reg 2.



2
LSI Devices

SN54ALS963, SN54ALS964, SN74ALS963, SN74ALS964 DUAL-RANK 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS963 SN54ALS964			SN74ALS963 SN74ALS964			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $I_{OH} = -0.4 \text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -1 \text{ mA}$	2.4	3.3					
	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -2.6 \text{ mA}$				2.4	3.2		
V_{OL}	SEROUT	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 8 \text{ mA}$	0.25	0.4	0.25	0.4	V	
		$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 16 \text{ mA}$			0.35	0.5		
	Q_A thru Q_H	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 12 \text{ mA}$	0.25	0.4	0.25	0.4		
		$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 24 \text{ mA}$			0.35	0.5		
I_I	A thru H	$V_{CC} = 5.5 \text{ V}$, $V_I = 5.5 \text{ V}$		0.1		0.1	mA	
	Any other	$V_{CC} = 5.5 \text{ V}$, $V_I = 7 \text{ V}$		0.1		0.1		
I_{IH}^\dagger	$V_{CC} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$			20		20	μA	
I_{IL}^\ddagger	$V_{CC} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$			-0.1		-0.1	mA	
I_O^\S	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.25 \text{ V}$	-30		-112	-30	-112	mA	
I_{CC}	'ALS963	$V_{CC} = 5.5 \text{ V}$	Outputs high				mA	
			Outputs low					
			Outputs disabled					
	'ALS964	$V_{CC} = 5.5 \text{ V}$	Outputs high				mA	
			Outputs low					
			Outputs disabled					

†All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡For I/O ports (Q_A through Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

2
LSI Devices

SN54ALS963, SN54ALS964, SN74ALS963, SN74ALS964
DUAL-RANK 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUTS

'ALS963 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX						UNIT
			SN54ALS963			SN74ALS963			
			MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}	CLK1 or CLK2	Any Q	25	30		25	30	MHz	
t _{PLH}	CLK1	Any Q				10			ns
t _{PHL}						14			
t _{PLH}	CLK2	SEROUT				10			ns
t _{PHL}						14			
t _{PHZ}	OE	Any Q				15			ns
t _{PLZ}						18			
t _{PZH}	OE	Any Q				12			ns
t _{PZL}						12			

2

LSI Devices

'ALS964 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX						UNIT
			SN54ALS964			SN74ALS964			
			MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}	CLK	Any Q	25	30		25	30	MHz	
t _{PLH}	CLK	Any Q				10			ns
t _{PHL}						14			
t _{PLH}	CLK	SEROUT				10			ns
t _{PHL}						14			
t _{PHZ}	ACLR	Any Q or SEROUT				14			ns
t _{PHZ}	OE	Any Q				15			ns
t _{PLZ}						18			
t _{PZH}	OE	Any Q				12			ns
t _{PZL}						12			

NOTE: Load circuit and voltage waveforms are shown in Section 1.

SN74ALS990, SN74ALS991 8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

D2835, APRIL 1984—REVISED JANUARY 1986

- 3-State I/O-Type Read-Back Inputs
- Bus-Structured Pinout
- Choice of True or Inverting Logic
'ALS990 . . . True Outputs
'ALS991 . . . Inverting Outputs
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

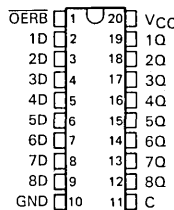
These 8-bit latches are designed specifically for storing the contents of the input data bus plus providing the capability of reading-back the stored data onto the input data bus.

The eight latches of the 'ALS990 and 'ALS991 are transparent D-type. While the enable (C) is high, the Q outputs of the 'ALS990 will follow the data (D) inputs. For the 'ALS991, the Q outputs will provide the complement of what is applied to its data (D) inputs.

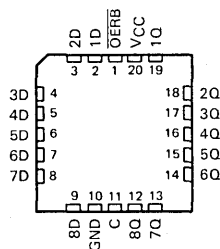
Read-back is provided through the read-back control input ($\overline{\text{OERB}}$). When the control is taken low, the data present at the output of the data latches will be allowed to pass back onto the input data bus. When it is taken high, the output of the data latches will be isolated from the data (D) inputs. The read-back control does not affect the internal operation of the latches; however, precautions should be taken not to create a bus-conflict situation.

The SN74ALS990 and SN74ALS991 are characterized for operation from 0°C to 70°C.

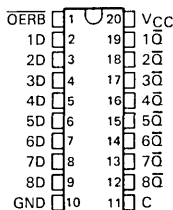
SN74ALS990 . . . DW OR N PACKAGE
(TOP VIEW)



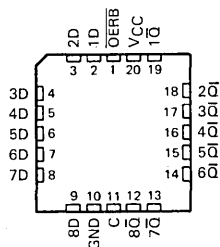
SN74ALS990 . . . FN PACKAGE
(TOP VIEW)



SN74ALS991 . . . DW OR N PACKAGE
(TOP VIEW)



SN74ALS991 . . . FN PACKAGE
(TOP VIEW)



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TEXAS
INSTRUMENTS

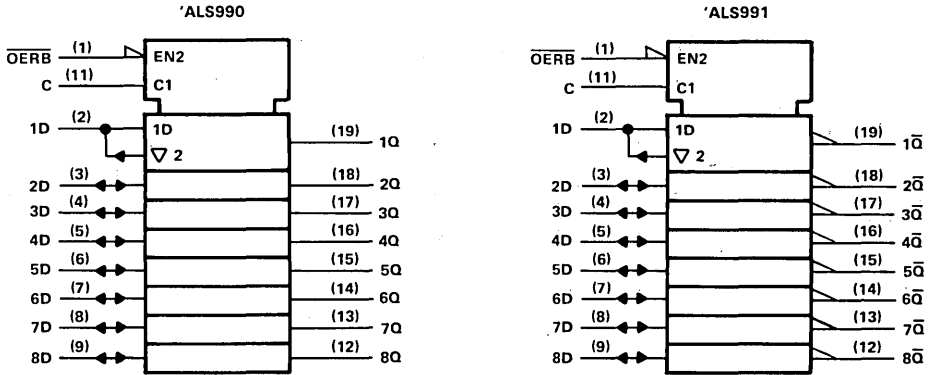
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2-441

SN74ALS990, SN74ALS991
8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

logic symbols†



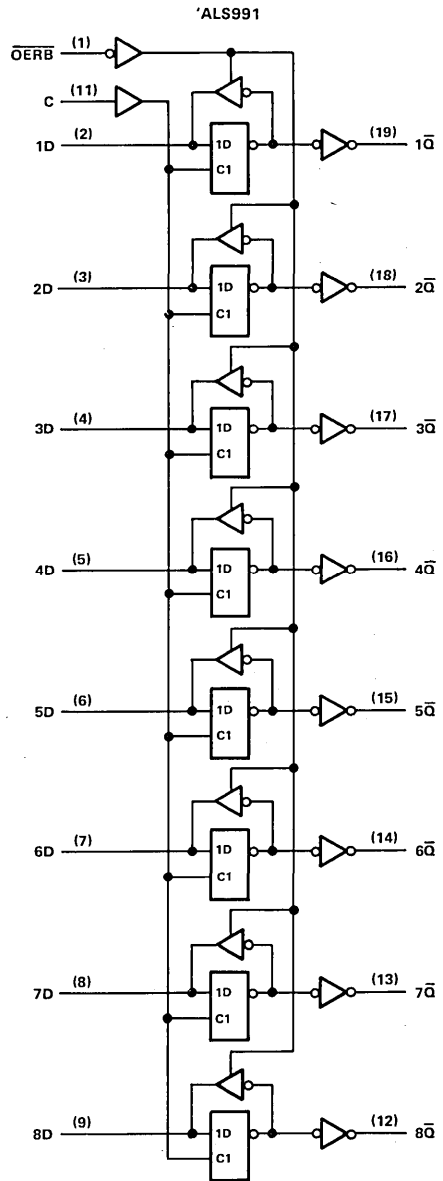
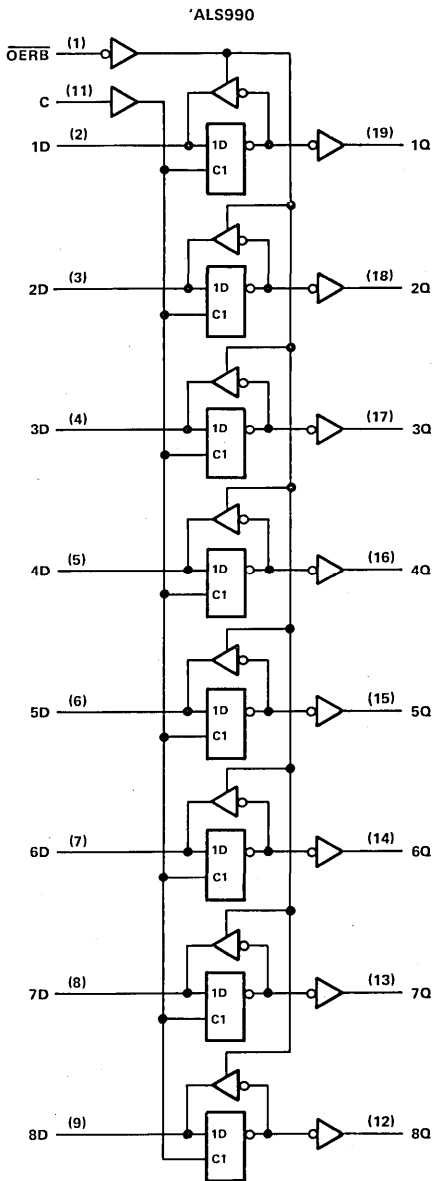
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

2

LSI Devices

SN74ALS990, SN74ALS991 8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

logic diagrams (positive logic)



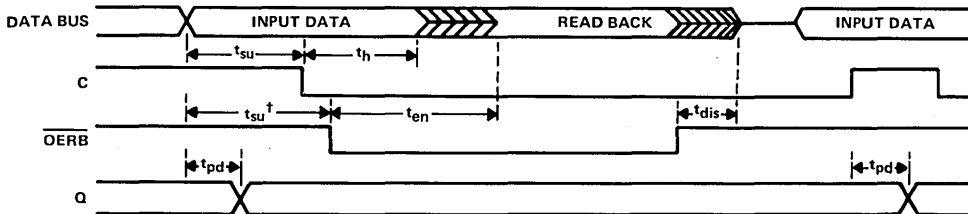
2

LSI Devices

SN74ALS990, SN74ALS991

8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

timing diagram



† This setup time ensures the readback circuit will not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage, (\overline{OERB} and C inputs)	7 V
Voltage applied to D inputs	5.5 V
Operating free-air temperature range SN74ALS990, SN74ALS991	0°C to 70°C
Storage temperature range	-65°C to 150°C

2

LSI Devices

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	Q		-2.6	mA
		D		-0.4	
I_{OL}	Low-level output current	Q		24	mA
		D		8	
t_w	Pulse duration, enable C high	10			ns
t_{su}	Setup time	Data before C \uparrow	10		ns
		Data before $\overline{OERB}\downarrow$	10		
t_h	Hold time	5			ns
T_A	Operating free-air temperature	0		70	°C

SN74ALS990, SN74ALS991, 8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
V _{IK}		V _{CC} = 4.5 V,	I _I = -18 mA			-1.2	V
V _{OH}	All outputs	V _{CC} = 4.5 V to 5.5 V,	I _{OH} = -0.4 mA	V _{CC} - 2			V
	Q or \bar{Q}	V _{CC} = 4.5 V,	I _{OH} = -2.6 mA	2.4	3.2		
V _{OL}	D	V _{CC} = 4.5 V,	I _{OL} = 4 mA		0.25	0.4	V
		V _{CC} = 4.5 V,	I _{OL} = 8 mA		0.35	0.5	
	Q or \bar{Q}	V _{CC} = 4.5 V,	I _{OL} = 12 mA		0.25	0.4	
		V _{CC} = 4.5 V,	I _{OL} = 24 mA		0.35	0.5	
I _I	\overline{OERB} , C	V _{CC} = 5.5 V,	V _I = 7 V			0.1	mA
	D inputs	V _{CC} = 5.5 V,	V _I = 5.5 V			0.1	
I _{IH}	\overline{OERB} , C	V _{CC} = 5.5 V,	V _I = 2.7 V			20	μ A
	D inputs [‡]					20	
I _{IL}	\overline{OERB} , C	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.1	mA
	D inputs [‡]					-0.1	
I _O [§]		V _{CC} = 5.5 V,	V _O = 2.25 V	-30		-112	mA
I _{CC}	'ALS990	V _{CC} = 5.5 V, \overline{OERB} high	Q outputs high		27	50	mA
			Q outputs low		40	70	
	\bar{Q} outputs high			25	45		
	\bar{Q} outputs low			45	75		
	'ALS991						

[†]All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡]For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§]The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit output current, I_{OS}.

SN74ALS990, SN74ALS991

8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

'ALS990 switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, T _A = 25°C, See Figures 1 and 2			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, T _A = 0°C to 70°C, See Figures 1 and 2		UNIT
			MIN	TYP	MAX	MIN	MAX	
t _{PLH}	D	Q		8	14	4	17	ns
t _{PHL}			11	22	5	24		
t _{PLH}	C	Q		13	22	6	26	ns
t _{PHL}			16	23	8	26		
t _{en}	OERB	D		12	18	4	21	ns
t _{dis}			10	18	4	19		

t_{en} = t_{PZL} or t_{PZH}

t_{dis} = t_{PLZ} or t_{PHZ}

'ALS991 switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, T _A = 25°C, See Figures 1 and 2			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, T _A = 0°C to 70°C, See Figures 1 and 2		UNIT
			MIN	TYP	MAX	MIN	MAX	
t _{PLH}	D	Q		12	15	4	20	ns
t _{PHL}			9	12	4	15		
t _{PLH}	C	Q		17	21	9	28	ns
t _{PHL}			14	18	7	23		
t _{en}	OERB	D		12	17	4	22	ns
t _{dis}			8	12	4	17		

t_{en} = t_{PZL} or t_{PZH}

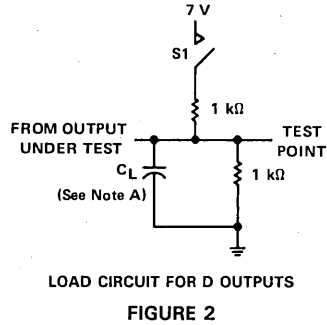
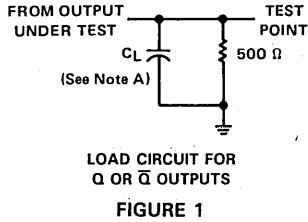
t_{dis} = t_{PLZ} or t_{PHZ}

2

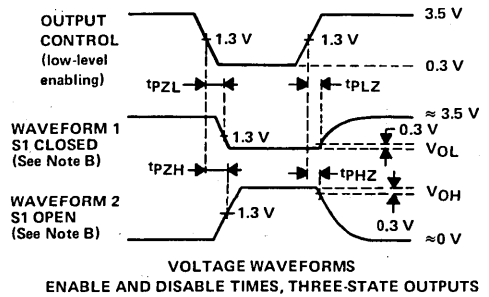
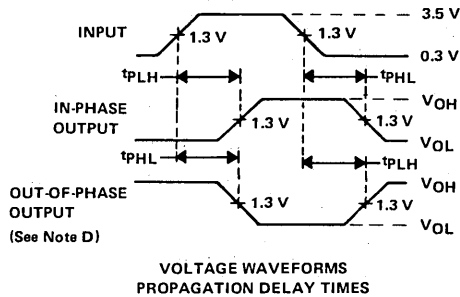
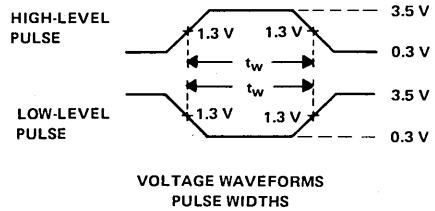
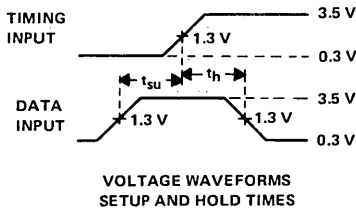
LSI Devices

SN74ALS990, SN74ALS991 8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.



- NOTES: B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
- D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

2

LSI Devices

SN74ALS992, SN74ALS993 9-BIT D-TYPE TRANSPARENT READ-BACK LATCHES WITH 3-STATE OUTPUTS

D2836, APRIL 1984—REVISED JANUARY 1986

- 3-State I/O-Type Read-Back Inputs
- Bus-Structured Pinout
- Choice of True or Inverting Logic
'ALS992 . . . True Outputs
'ALS993 . . . Inverting Outputs
- Designed with 9 Bits for Parity Applications
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

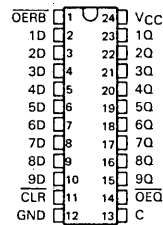
These 9-bit latches are designed specifically for storing the contents of the input data bus plus providing the capability of reading-back the stored data onto the input data bus. In addition, they provide a 3-state buffer-type output and are easily implemented in parity applications.

The nine latches of the 'ALS992 and 'ALS993 are transparent D-type. While the enable (C) is high, the Q outputs of the 'ALS992 will follow the data (D) inputs. For the 'ALS993, the \bar{Q} outputs will provide the complement of what is applied to its data (D) inputs. On both devices, the Q or \bar{Q} outputs will be in the 3-state condition when output enable \overline{OEQ} is high.

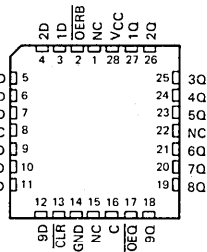
Read-back is provided through the read-back control input (\overline{OERB}). When the control is taken low, the data present at the output of the data latches will be allowed to pass back onto the input data bus. When it is taken high, the output of the data latches will be isolated from the data (D) inputs. The read-back control does not affect the internal operation of the latches; however, precautions should be taken not to create a bus-conflict situation.

The SN74ALS992 and SN74ALS993 are characterized for operation from 0°C to 70°C.

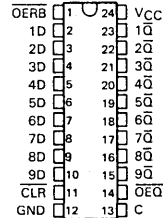
SN74ALS992 . . . DW OR NT PACKAGE
(TOP VIEW)



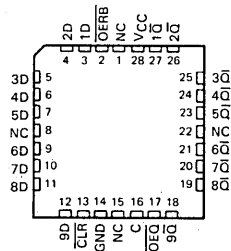
SN74ALS992 . . . FN PACKAGE
(TOP VIEW)



SN74ALS993 . . . DW OR NT PACKAGE
(TOP VIEW)



SN74ALS993 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

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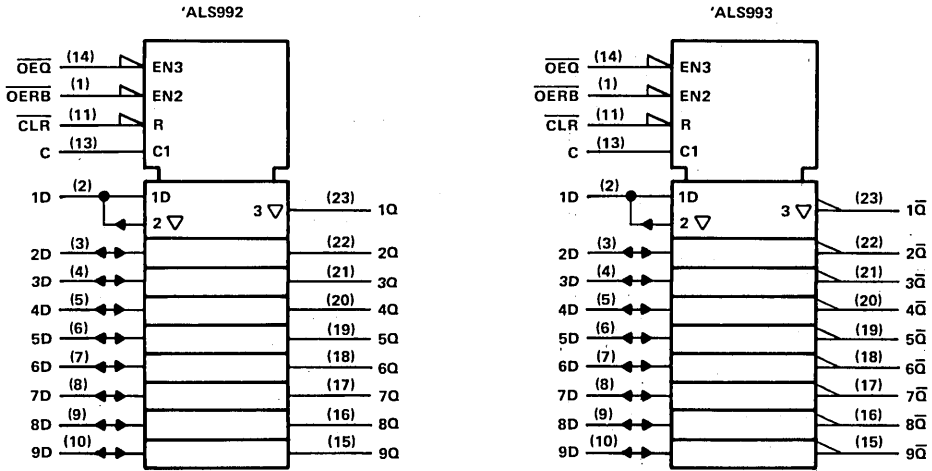
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SN74ALS992, SN74ALS993

9-BIT D-TYPE TRANSPARENT READ-BACK LATCHES WITH 3-STATE OUTPUTS

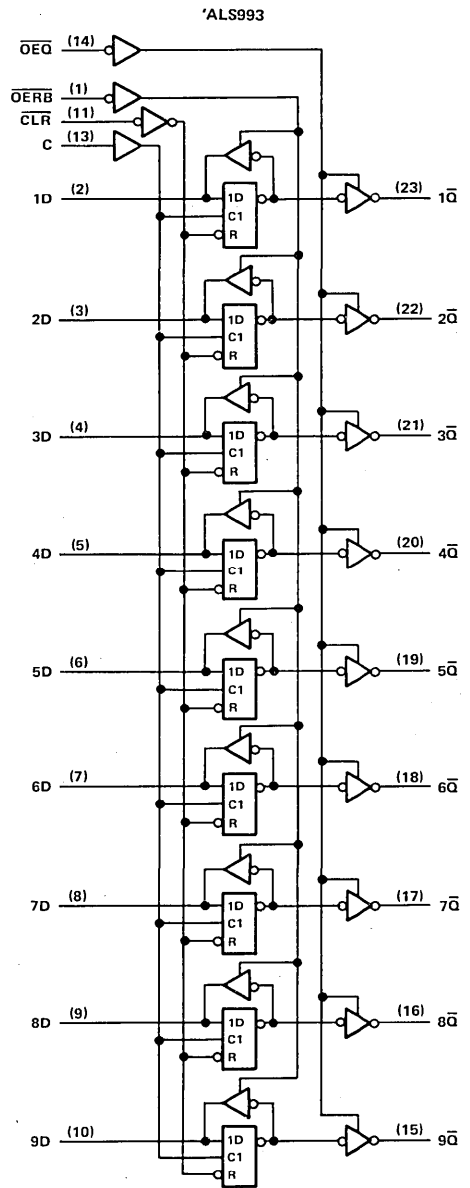
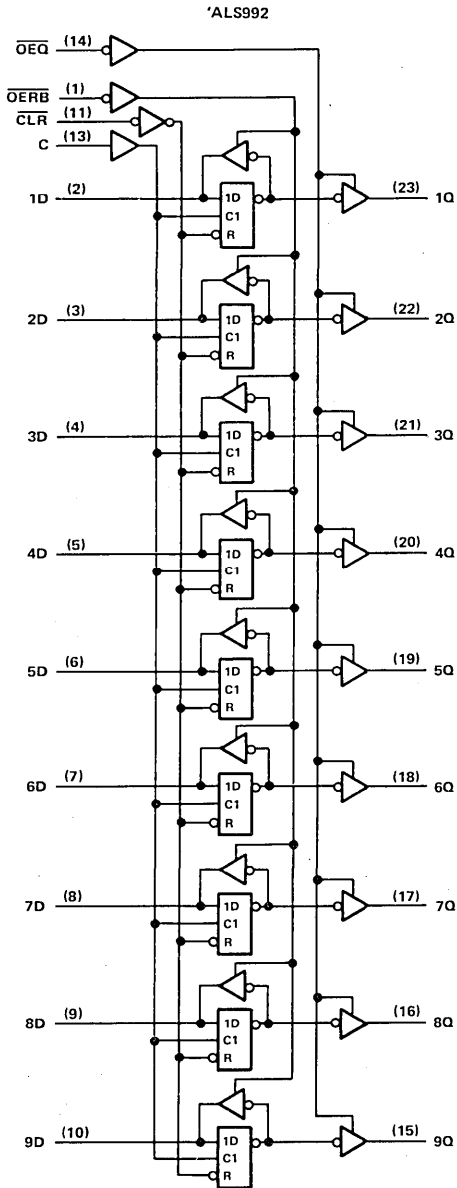
logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers are for DW and NT packages.

SN74ALS992, SN74ALS993
9-BIT D-TYPE TRANSPARENT READ-BACK LATCHES
WITH 3-STATE OUTPUTS

logic diagrams (positive logic)



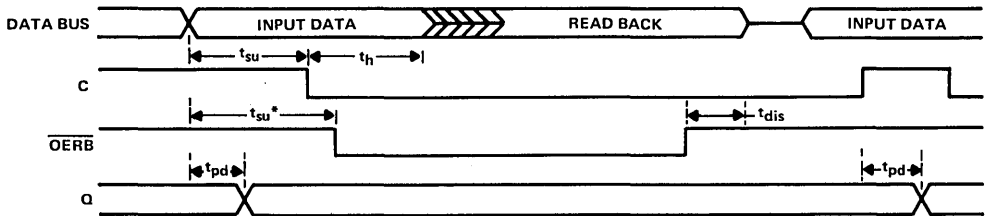
Pin numbers are for DW and NT packages.

2
LSI Devices

SN74ALS992, SN74ALS993

9-BIT D-TYPE TRANSPARENT READ-BACK LATCHES WITH 3-STATE OUTPUTS

timing diagram



$\overline{\text{CLR}} = \text{H}, \overline{\text{OE}} = \text{L}$

*This setup time ensures the readback circuit will not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage, ($\overline{\text{OERB}}$, $\overline{\text{OE}}$, $\overline{\text{CLR}}$, and C inputs)	7 V
Voltage applied to D inputs and to disabled 3-state outputs	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

2

LSI Devices

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	Q or \overline{Q}		-2.6	mA
		D		-0.4	
I_{OL}	Low-level output current	Q or \overline{Q}		24	mA
		D		8	
t_w	Pulse duration	Enable C high	10		ns
		$\overline{\text{CLR}}$ low	10		
t_{su}	Setup time	Data before C↓	10		ns
		Data before $\overline{\text{OERB}}\downarrow$	10		
t_h	Hold time		5		ns
T_A	Operating free-air temperature	0		70	°C

SN74ALS992, SN74ALS993
9-BIT D-TYPE TRANSPARENT READ-BACK LATCHES
WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
V_{IK}		$V_{CC} = 4.5 \text{ V}$,	$I_I = -18 \text{ mA}$			-1.2	V	
V_{OH}	All outputs Q or \bar{Q}	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$,	$I_{OH} = -0.4 \text{ mA}$	$V_{CC} - 2$			V	
		$V_{CC} = 4.5 \text{ V}$,	$I_{OH} = -2.6 \text{ mA}$	2.4	3.2			
V_{OL}	D	$V_{CC} = 4.5 \text{ V}$,	$I_{OL} = 4 \text{ mA}$		0.25	0.4	V	
		$V_{CC} = 4.5 \text{ V}$,	$I_{OL} = 8 \text{ mA}$		0.35	0.5		
	Q or \bar{Q}	$V_{CC} = 4.5 \text{ V}$,	$I_{OL} = 12 \text{ mA}$		0.25	0.4		
		$V_{CC} = 4.5 \text{ V}$,	$I_{OL} = 24 \text{ mA}$		0.35	0.5		
I_{OZH}	Q or \bar{Q}	$V_{CC} = 5.5 \text{ V}$,	$V_O = 2.7 \text{ V}$			20	μA	
I_{OZL}		$V_{CC} = 5.5 \text{ V}$,	$V_O = 0.4 \text{ V}$			-20		
I_I	D inputs	$V_{CC} = 5.5 \text{ V}$,	$V_I = 5.5 \text{ V}$			0.1	mA	
	All other	$V_{CC} = 5.5 \text{ V}$,	$V_I = 7 \text{ V}$			0.1		
I_{IH}	D inputs‡	$V_{CC} = 5.5 \text{ V}$,	$V_I = 2.7 \text{ V}$			20	μA	
	All other					20		
I_{IL}	D inputs‡	$V_{CC} = 5.5 \text{ V}$,	$V_I = 0.4 \text{ V}$			-0.1	mA	
	All other					-0.1		
I_O^{\S}		$V_{CC} = 5.5 \text{ V}$,	$V_O = 2.25 \text{ V}$	-30		-1.12	mA	
I_{CC}	'ALS992	$V_{CC} = 5.5 \text{ V}$, $\overline{\text{OERB}}$ high	Q outputs high			30	50	mA
			Q outputs low			50	80	
			Q outputs disabled			35	55	
	'ALS993		\bar{Q} outputs high			30	50	
			\bar{Q} outputs low			52	82	
			\bar{Q} outputs disabled			40	60	

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit output current, I_{OS} .

2

LSI Devices

SN74ALS992, SN74ALS993
9-BIT D-TYPE TRANSPARENT READ-BACK LATCHES
WITH 3-STATE OUTPUTS

'ALS992 switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, T _A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t _{PLH}	D	Q	7	10	3	14	ns	
t _{PHL}			9	13	4	16		
t _{PLH}	C	Q	12	15	6	20	ns	
t _{PHL}			15	19	8	25		
t _{PHL}	CLR	Q	12	16	6	20	ns	
t _{PHL}		D	15	22	8	26		
t _{en}	O _{ERB}	D	11	17	4	21	ns	
t _{dis}			6	11	2	14		
t _{en}	O _{EQ}	Q	11	16	4	18	ns	
t _{dis}			6	10	1	14		

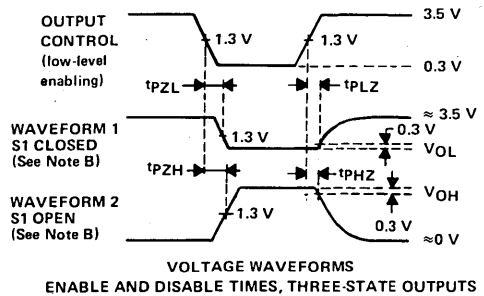
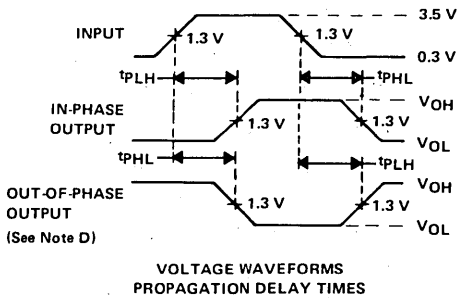
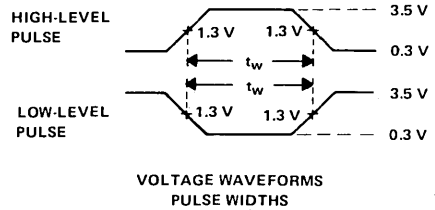
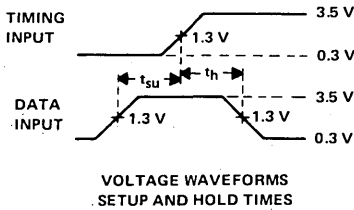
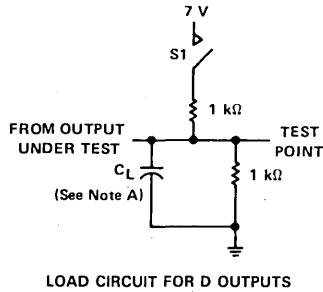
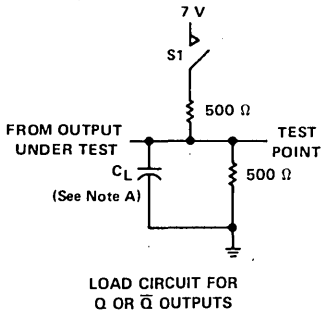
'ALS993 switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, T _A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t _{PLH}	D	Q̄	11	14	6	20	ns	
t _{PHL}			8	11	4	15		
t _{PLH}	C	Q̄	16	20	9	28	ns	
t _{PHL}			13	16	7	22		
t _{PLH}	CLR	Q	10	13	5	17	ns	
t _{PLH}		D	15	22	8	26		
t _{en}	O _{ERB}	D	11	17	4	21	ns	
t _{dis}			6	11	2	14		
t _{en}	O _{EQ}	Q̄	11	16	4	20	ns	
t _{dis}			6	10	1	12		

t_{en} = t_{PZH} or t_{PZL}
t_{dis} = t_{PHZ} or t_{PLZ}

SN74ALS992, SN74ALS993
9-BIT D-TYPE TRANSPARENT READ-BACK LATCHES
WITH 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

FIGURE 1

2
LSI Devices

SN74ALS994, SN74ALS995 10-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

D2856, OCTOBER 1984—REVISED JANUARY 1986

- 3-State I/O-Type Read-Back Inputs
- Bus-Structured Pinout
- Choice of True or Inverting Logic
'ALS994 . . . True Outputs
'ALS995 . . . Inverting Outputs
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

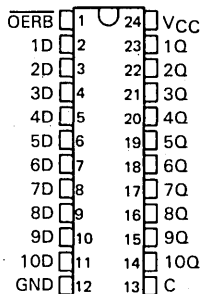
These 10-bit latches are designed specifically for storing the contents of the input data bus plus providing the capability of reading-back the stored data onto the input data bus.

The ten latches of the 'ALS994 and 'ALS995 are transparent D-type. While the enable (C) is high, the Q outputs of the 'ALS994 will follow the data (D) inputs. For the 'ALS995, the Q outputs will provide the inverse of what is applied to its data (D) inputs.

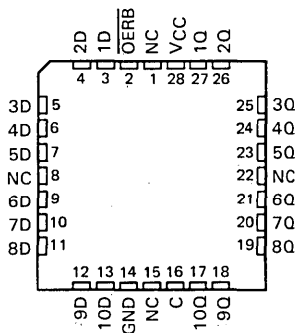
Read-back is provided through the read-back control input ($\overline{\text{OERB}}$). When the control is taken low, the data present at the output of the data latches will be allowed to pass back onto the input data bus. When it is taken high, the output of the data latches will be isolated from the data (D) inputs. The read-back control does not affect the internal operation of the latches; however, precautions should be taken not to create a bus-conflict situation.

The SN74ALS994 and SN74ALS995 are characterized for operation from 0°C to 70°C.

SN74ALS994 . . . DW OR NT PACKAGE
(TOP VIEW)



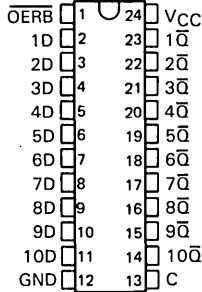
SN74ALS994 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection.

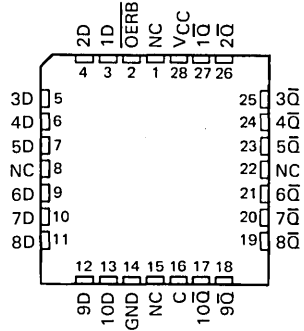
SN74ALS994, SN74ALS995 10-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

SN74ALS995 . . . DW OR NT PACKAGE
(TOP VIEW)

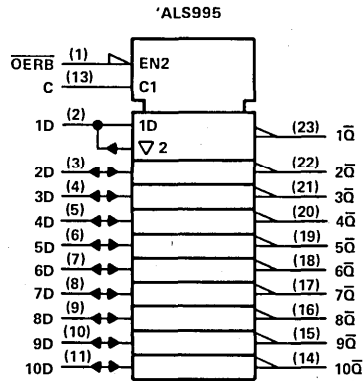
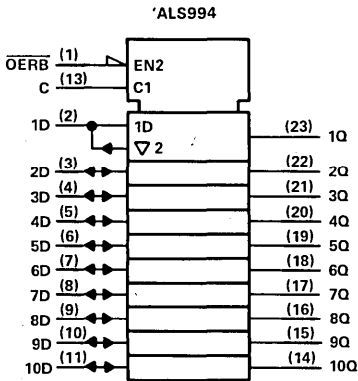


NC—No internal connection

SN74ALS995 . . . FN PACKAGE
(TOP VIEW)



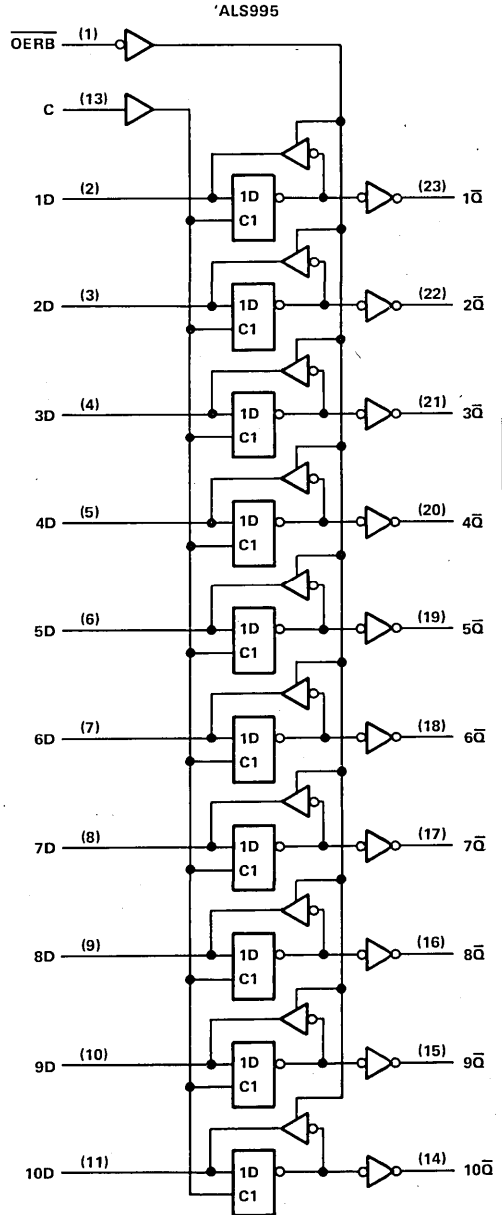
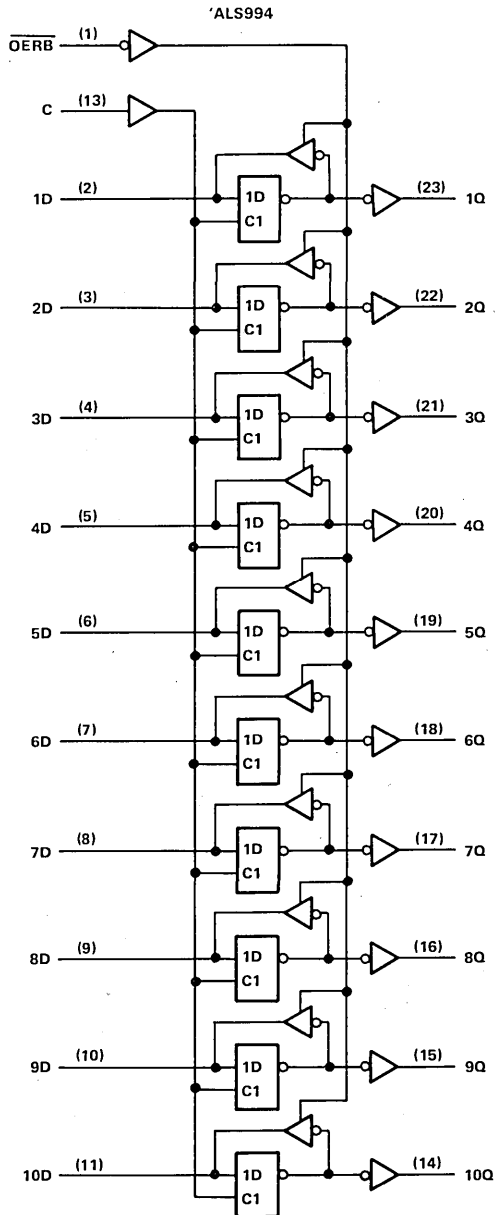
logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW and NT packages.

SN74ALS994, SN74ALS995 10-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

logic diagrams (positive logic)



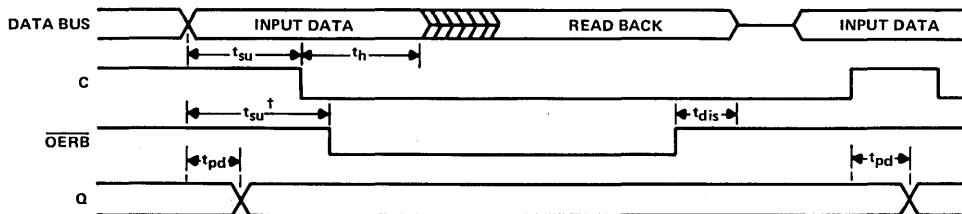
Pin numbers shown are for DW and NT packages.

2

LSI Devices

SN74ALS994, SN74ALS995 10-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

timing diagram



† This setup time ensures the readback circuit will not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage (OERB and C)	7 V
Voltage applied to D inputs	5.5 V
Operating free-air temperature	0°C to 70°C
Storage temperature range	-65°C to 150°C

2

LSI Devices

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	Q or \bar{Q}		-2.6	mA
		D		-0.4	
I_{OL}	Low-level output current	Q or \bar{Q}		24	mA
		D		8	
t_w	Pulse duration, enable C high	10			ns
t_{su}	Setup time	Data before C↓	10		ns
		Data before OERB!†	10		
t_h	Hold time	5			ns
T_A	Operating free-air temperature	0		70	°C

† This setup time ensures the readback circuit will not create a conflict on the input data bus.

SN74ALS994, SN74ALS995
10-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT	
V_{IK}		$V_{CC} = 4.5 \text{ V}$,	$I_I = -18 \text{ mA}$			-1.2	V	
V_{OH}	All outputs	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $I_{OH} = -0.4 \text{ mA}$		$V_{CC}-2$			V	
	Q or \bar{Q}	$V_{CC} = 4.5 \text{ V}$,	$I_{OH} = -2.6 \text{ mA}$	2.4	3.2			
V_{OL}	D	$V_{CC} = 4.5 \text{ V}$,	$I_{OL} = 4 \text{ mA}$		0.25	0.4	V	
		$V_{CC} = 4.5 \text{ V}$,	$I_{OL} = 8 \text{ mA}$		0.35	0.5		
	Q or \bar{Q}	$V_{CC} = 4.5 \text{ V}$,	$I_{OL} = 12 \text{ mA}$		0.25	0.4		
		$V_{CC} = 4.5 \text{ V}$,	$I_{OL} = 24 \text{ mA}$		0.35	0.5		
I_I	\overline{OERB} , C	$V_{CC} = 5.5 \text{ V}$,	$V_I = 7 \text{ V}$			0.1	mA	
	D inputs	$V_{CC} = 5.5 \text{ V}$,	$V_I = 5.5 \text{ V}$			0.1		
I_{IH}	\overline{OERB} , C	$V_{CC} = 5.5 \text{ V}$,	$V_I = 2.7 \text{ V}$			20	μA	
	D inputs [‡]					20		
I_{IL}	\overline{OERB} , C	$V_{CC} = 5.5 \text{ V}$,	$V_I = 0.4 \text{ V}$			-0.1	mA	
	D inputs [‡]					-0.1		
I_O [§]		$V_{CC} = 5.5 \text{ V}$,	$V_O = 2.25 \text{ V}$	-30		-112	mA	
I_{CC}	'ALS994	$V_{CC} = 5.5 \text{ V}$,	\overline{OERB} high	Q outputs high		30	50	mA
				Q outputs low		52	82	
	\bar{Q} outputs high				30	50		
	\bar{Q} outputs low				55	85		
	'ALS995							

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] The output conditions have been chosen to produce a current that closely approximates one-half the true short-circuit output current, I_{OS} .

SN74ALS994, SN74ALS995
10-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

'ALS994 switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, T _A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t _{PLH}	D	Q	7	10	3	14	ns	
t _{PHL}			11	15	4	18		
t _{PLH}	C	Q	12	16	6	21	ns	
t _{PHL}			16	21	8	27		
t _{en}	$\overline{\text{OERB}}$	D	11	17	4	21	ns	
t _{dis}			9	13	2	16		

'ALS995 switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, T _A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t _{PLH}	D	$\overline{\text{Q}}$	12	16	6	20	ns	
t _{PHL}			9	12	4	15		
t _{PLH}	C	$\overline{\text{Q}}$	17	23	9	28	ns	
t _{PHL}			14	19	7	22		
t _{en}	$\overline{\text{OERB}}$	D	12	18	4	21	ns	
t _{dis}			8	12	2	15		

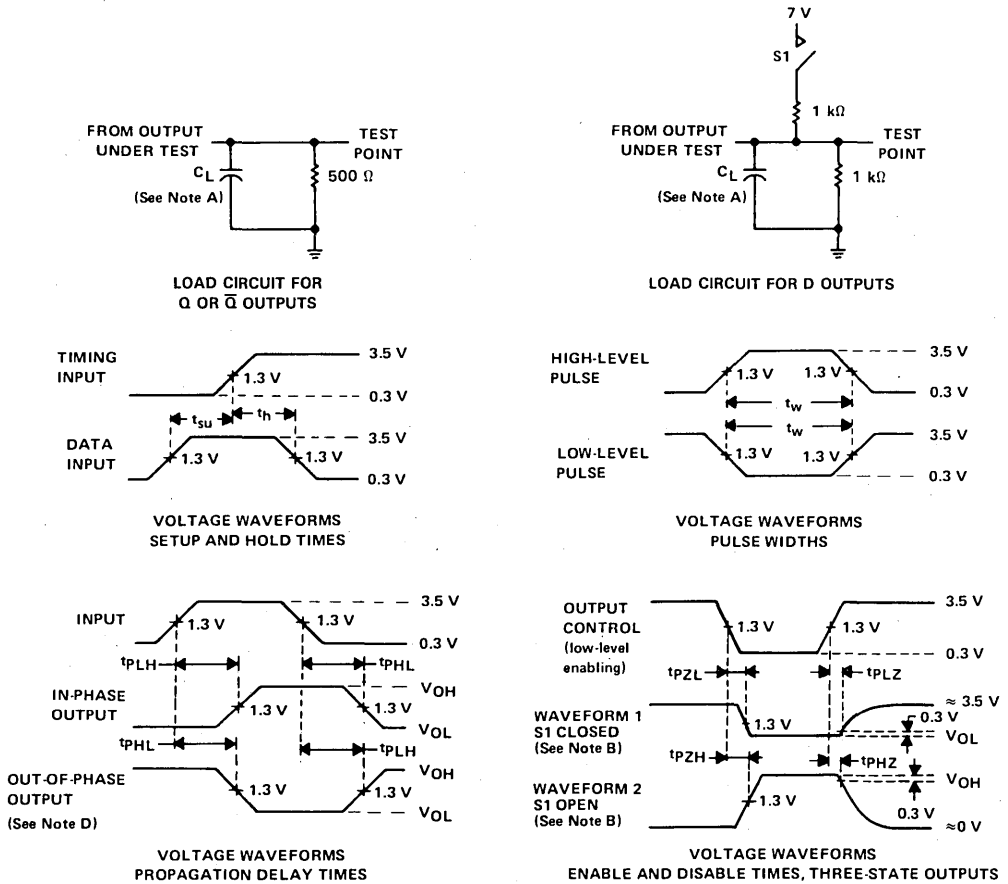
t_{en} = t_{PZH} or t_{PZL}
t_{dis} = t_{PHZ} or t_{PLZ}

2

LSI Devices

SN74ALS994, SN74ALS995 10-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

FIGURE 1

2
LSI Devices

2

LSI Devices

- 3-State I/O-Type Read-Back Inputs
- Bus-Structured Pinout
- T/\overline{C} Determines True or Complementary Data at Q Outputs
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit registers are designed specifically for storing the contents of the input data bus plus providing the capability of reading-back the stored data onto that bus. The Q outputs are designed with bus-driving capability.

The edge-triggered flip-flops enter the data on the low-to-high transition of the clock (CLK) when enable (\overline{EN}) is low. Data can be read-back onto the data inputs by taking the read input (RD) low, in addition to having \overline{EN} low. Whenever \overline{EN} is high, both the read-back and write modes are disabled. Transitions on \overline{EN} should only be made with CLK high in order to prevent false clocking.

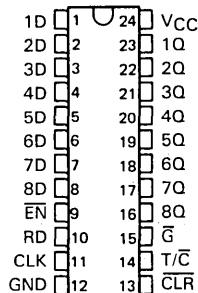
The polarity of the Q outputs can be controlled by the polarity input T/\overline{C} . When T/\overline{C} is high, Q will be the same as is stored in the flip-flops. When T/\overline{C} is low, the output data will be inverted. The Q outputs can be placed in a high-impedance state by taking the output control (\overline{G}) high. The output control \overline{G} does not affect the internal operations of the register. Old data can be retained or new data can be entered while the outputs are off.

A low level at the clear input (\overline{CLR}) resets the internal registers low. The clear function is asynchronous and overrides all other register functions.

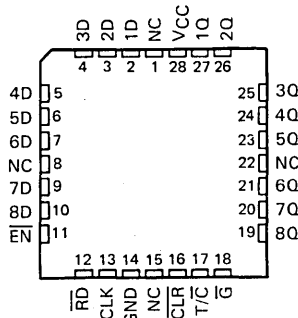
The -1 version of the SN74ALS996 is identical to the standard version except that the recommended maximum I_{OL} is increased to 48 milliamperes.

The SN74ALS996 is characterized for operation from 0°C to 70°C.

**DW OR NT PACKAGE
(TOP VIEW)**



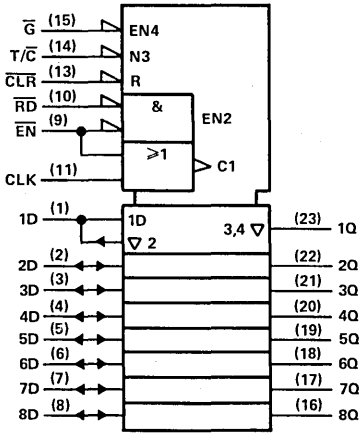
**FN PACKAGE
(TOP VIEW)**



NC—No internal connection.

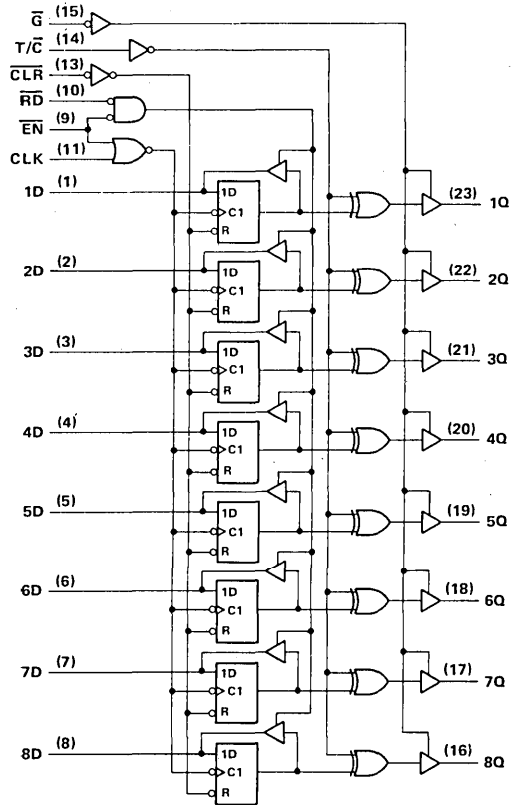
SN74ALS996 8-BIT D-TYPE EDGE-TRIGGERED READ-BACK LATCHES

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

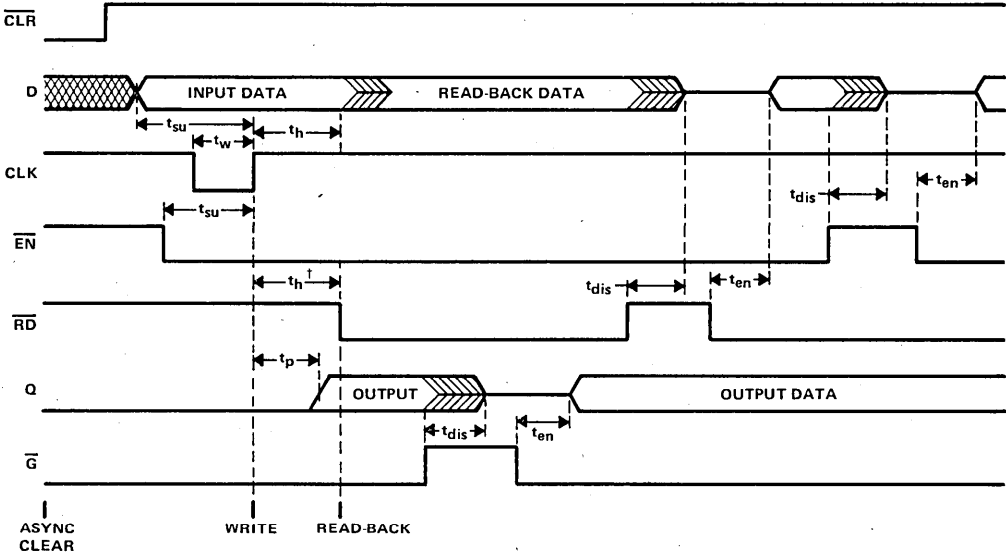


Pin numbers shown are for DW and NT packages.

SN74ALS996
8-BIT D-TYPE EDGE-TRIGGERED READ-BACK LATCHES

timing diagram

($T/\bar{C} = H$)



This hold time ensures the readback circuit will not create a conflict on the input data bus.

2
LSI Devices

SN74ALS996

8-BIT D-TYPE EDGE-TRIGGERED READ-BACK LATCHES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage (\overline{G} , \overline{RD} , \overline{EN} , CLK , \overline{CLR} , and T/\overline{C})	7 V
Voltage applied to D inputs and to disabled 3-state outputs	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	Q		2.6	mA
		D		-0.4	
I_{OL}	Low-level output current	Q		24	mA
		D		48 [†]	
f_{clock}	Clock frequency	0		35	MHz
t_w	Pulse duration	\overline{CLR} low		10	ns
		CLK low		14.5	
		CLK high		14.5	
t_{su}	Setup time	Data before $CLK\uparrow$		15	ns
		\overline{EN} low before $CLK\uparrow$		10	
		CLK high before $\overline{EN}\uparrow$ [‡]		15	
		\overline{CLR} high (inactive) before $CLK\uparrow$		10	
t_h	Hold time	Data after $CLK\uparrow$		0	ns
		\overline{EN} low after $CLK\uparrow$		5	
		\overline{RD} high after $CLK\uparrow$ [§]		5	
T_A	Operating free-air temperature	0		70	°C

[†]The 48-mA limit applies for the SN74ALS966-1 only and only if V_{CC} is maintained between 4.75 V and 5.25 V.

[‡]This setup time guarantees that \overline{EN} will not false clock the data register.

[§]This hold time ensures there will be no conflict on the input data bus.

SN74ALS996

8-BIT D-TYPE EDGE-TRIGGERED READ-BACK LATCHES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
V_{IK}		$V_{CC} = 4.5 \text{ V}$,	$I_I = -18 \text{ mA}$			-1.2	V	
V_{OH}	All outputs	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$,	$I_{OH} = -0.4 \text{ mA}$	$V_{CC} - 2$			V	
	Q	$V_{CC} = 4.5 \text{ V}$,	$I_{OH} = -2.6 \text{ mA}$	2.4	3.2			
V_{OL}	D	$V_{CC} = 4.5 \text{ V}$,	$I_{OL} = 4 \text{ mA}$		0.25	0.4	V	
		$V_{CC} = 4.5 \text{ V}$,	$I_{OL} = 8 \text{ mA}$		0.35	0.5		
	Q	$V_{CC} = 4.5 \text{ V}$,	$I_{OL} = 12 \text{ mA}$		0.25	0.4		
		$V_{CC} = 4.5 \text{ V}$,	$I_{OL} = 24 \text{ mA}$ ($I_{OL} = 48 \text{ mA}$ for -1 versions)		0.35	0.5		
I_{OZH}	Q	$V_{CC} = 5.5 \text{ V}$,	$V_I = 2.7 \text{ V}$			20	μA	
I_{OZL}		$V_{CC} = 5.5 \text{ V}$,	$V_I = 0.4 \text{ V}$			-20		
I_I	D inputs	$V_{CC} = 5.5 \text{ V}$,	$V_I = 5.5 \text{ V}$			0.1	mA	
	All others	$V_{CC} = 5.5 \text{ V}$,	$V_I = 7 \text{ V}$			0.1		
I_{IH}	D inputs‡	$V_{CC} = 5.5 \text{ V}$,	$V_I = 2.7 \text{ V}$			20	μA	
	All others					20		
I_{IL}	D inputs‡	$V_{CC} = 5.5 \text{ V}$,	$V_I = 0.4 \text{ V}$			-0.1	mA	
	All others					-0.1		
I_O^{\S}		$V_{CC} = 5.5 \text{ V}$,	$V_O = 2.25 \text{ V}$	-30		-112	mA	
I_{CC}		$V_{CC} = 5.5 \text{ V}$,	Q outputs high			35	55	mA
			Q outputs low			55	85	
			\overline{OERB} high			42	65	

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been chosen to produce current that closely approximates one half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V}$, $C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$			$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $T_A = 0^\circ\text{C to } 70^\circ\text{C}$		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}				40			35	MHz
t_{PLH}	CLK	Q		16	24		5	28
t_{PHL}			($T/\overline{C} = \text{H or L}$)		16	24		5
t_{PLH}	\overline{CLR} ($T/\overline{C} = \text{L}$)	Q		15	23		7	27
t_{PHL}			($T/\overline{C} = \text{H}$)		13	19		7
t_{PLH}	T/\overline{C}	Q		13	20		5	23
t_{PHL}					13	20		5
t_{PHL}	\overline{CLR}	D		19	25		8	30
t_{en}	\overline{RD}	D		9	15		3	16
t_{dis}					10	16		3
t_{en}	\overline{EN}	D		9	14		3	16
t_{dis}					10	16		3
t_{en}	\overline{C}	Q		8	13		4	15
t_{dis}					4	8		1

$t_{en} = t_{PZH}$ or t_{PZL}

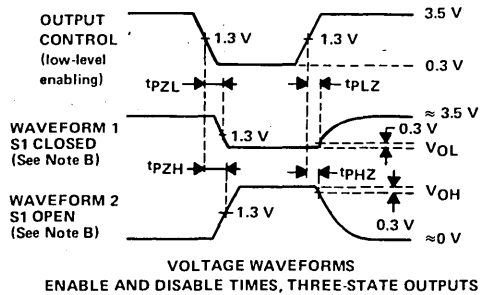
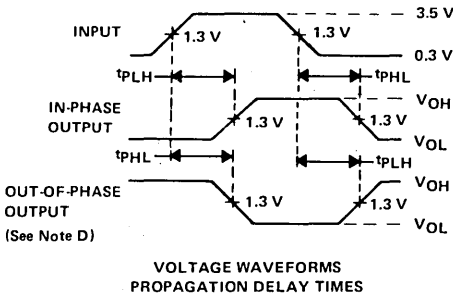
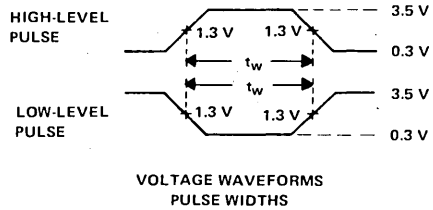
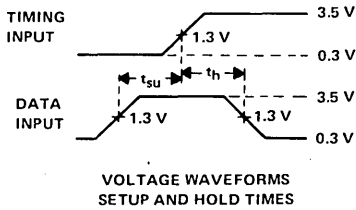
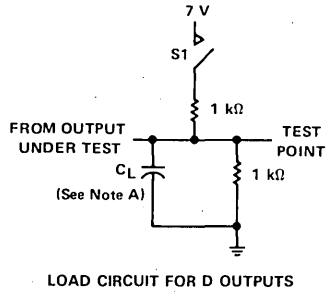
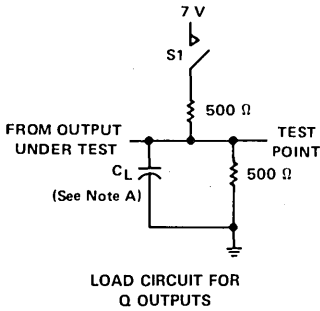
$t_{dis} = t_{PHZ}$ or t_{PLZ}

2

LSI Devices

SN74ALS996
8-BIT D-TYPE EDGE-TRIGGERED READ-BACK LATCHES

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

FIGURE 1

2

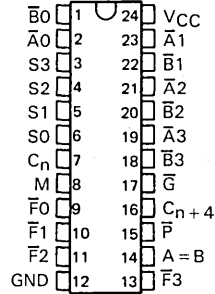
LSI Devices

SN54AS1181, SN74AS1181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

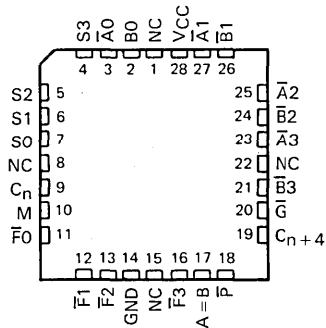
D1915, MAY 1985

- Package Options Include Compact 300-mil or Standard 600-mil DIPs and Both Plastic and Ceramic Chip Carriers
- Full Look-Ahead for High-Speed Operations on Long Words
- Arithmetic Operating Modes:
 - Addition
 - Subtraction
 - Shift Operand A One Position
 - Magnitude Comparison
 - Plus Twelve Other Arithmetic Operations
- Logic Function Modes
 - Exclusive-OR
 - Comparator
 - AND, NAND, OR, NOR
- Dependable Texas Instruments Quality and Reliability

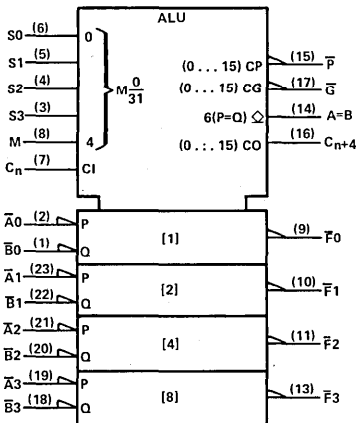
SN54AS1181 . . . JT OR JW PACKAGE
SN74AS1181 . . . DW, NT, OR NW PACKAGE
(TOP VIEW)



SN54AS1181 . . . FK PACKAGE
SN74AS1181 . . . FN PACKAGE
(TOP VIEW)



logic symbol †



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, JW, NT, and NW packages.

TYPICAL ADDITION TIMES ($C_L = 15 \text{ pF}$, $R_L = 280 \Omega$, $T_A = 25^\circ\text{C}$)

NUMBER OF BITS	ADDITION TIMES			PACKAGE COUNT		CARRY METHOD BETWEEN ALUs
	USING 'AS1181 AND 'AS882	USING 'AS181A AND 'AS882	USING 'S181 AND 'S182	ARITHMETIC LOGIC UNITS	LOOK-AHEAD CARRY GENERATORS	
1 to 4	5 ns	5 ns	11 ns	1		NONE
5 to 8	10 ns	10 ns	18 ns	2		RIPPLE
9 to 16	14 ns	14 ns	19 ns	3 or 4	1	FULL LOOK-AHEAD
17 to 64	19 ns	19 ns	28 ns	5 to 16	2 to 5	FULL LOOK-AHEAD

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2

LSI Devices

SN54AS1181, SN74AS1181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

description

The 'AS1181 arithmetic logic units (ALU)/function generators have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the SN54AS882 or SN74AS882 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown previously illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading 'AS882 circuits with these ALUs to provide multilevel full carry look-ahead is illustrated under signal designations.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The 'AS1181 will accommodate active-high or active-low data if the pin designations are interpreted as follows:

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-low data (Table 1)	$\bar{A}0$	$\bar{B}0$	$\bar{A}1$	$\bar{B}1$	$\bar{A}2$	$\bar{B}2$	$\bar{A}3$	$\bar{B}3$	$\bar{F}0$	$\bar{F}1$	$\bar{F}2$	$\bar{F}3$	C_n	C_{n+4}	\bar{P}	\bar{G}
Active-high data (Table 2)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	\bar{C}_n	\bar{C}_{n+4}	X	Y

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is $A - B - 1$, which requires an end-around or forced carry to provide $A - B$.

The 'AS1181 can also be utilized as a comparator. The $A = B$ output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality ($A = B$). The ALU must be in the subtract mode with $C_n = H$ when performing this comparison. The $A = B$ output is open-collector so that it can be wired-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select input S3, S2, S1, S0 at L, H, H, L, respectively.

INPUT C_n	OUTPUT C_{n+4}	ACTIVE-LOW DATA (FIGURE 1)	ACTIVE-HIGH DATA (FIGURE 2)
H	H	$A \geq B$	$A \leq B$
H	L	$A < B$	$A > B$
L	H	$A > B$	$A < B$
L	L	$A \leq B$	$A \geq B$

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

SN54AS1181, SN74AS1181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

signal designations

In both Figures 1 and 2, the polarity indicators (∇) indicate that the associated input or output is active-low with respect to the function shown inside the symbol and the symbols are the the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data, and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accommodate the logic functions and arithmetic operations for the active-high data given in Table 2. The 'AS1181 together with 'AS882 and 'S182 can be used with the signal designation of either Figure 1 or Figure 2.

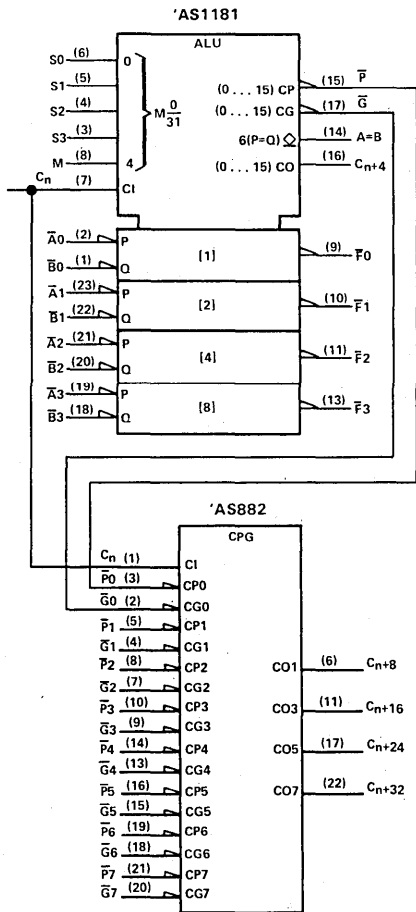


FIGURE 1
(USE WITH TABLE 1)

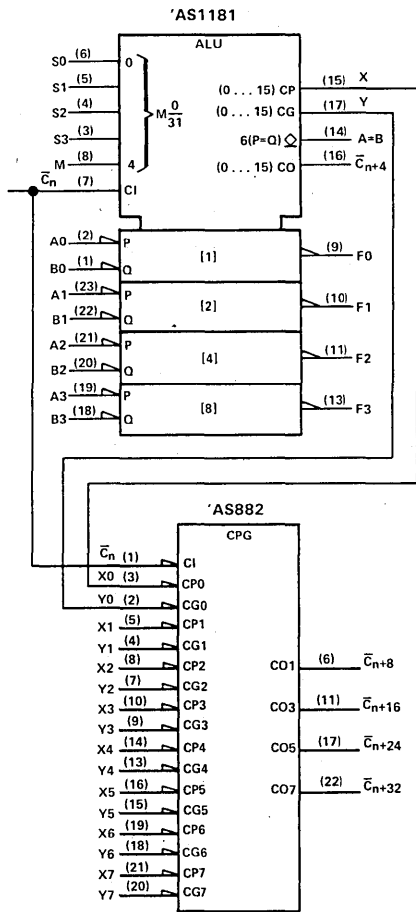


FIGURE 2
(USE WITH TABLE 2)

Pin numbers shown for the 'AS1181 are for DW, JT, JW, NT, and NW packages.

2
LSI Devices

SN54AS1181, SN74AS1181
 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

TABLE 1

SELECTION	M = H LOGIC FUNCTIONS			ACTIVE-LOW DATA	
				M = L; ARITHMETIC OPERATIONS	
				$\bar{C}_n = L$ (no carry)	$C_n = H$ (with carry)
L L L L	$F = \bar{A}$	F = A MINUS 1	F = A		
L L L H	$F = \bar{A}\bar{B}$	F = AB MINUS 1	F = AB		
L L H L	$F = \bar{A} + B$	F = $\bar{A}\bar{B}$ MINUS 1	F = $\bar{A}\bar{B}$		
L L H H	F = 1	F = MINUS 1 (2's COMPL)	F = ZERO		
L H L L	$F = \overline{A+B}$	F = A PLUS (A + \bar{B})	F = A PLUS (A + \bar{B}) PLUS 1		
L H L H	$F = \bar{B}$	F = AB PLUS (A + \bar{B})	F = AB PLUS (A + \bar{B}) PLUS 1		
L H H L	$F = A \odot B$	F = A MINUS B MINUS 1	F = A MINUS B		
L H H H	$F = A + \bar{B}$	F = A + \bar{B}	F = (A + \bar{B}) PLUS 1		
H L L L	$F = \bar{A}\bar{B}$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1		
H L L H	$F = A \oplus B$	F = A PLUS B	F = A PLUS B PLUS 1		
H L H L	$F = B$	F = $\bar{A}\bar{B}$ PLUS (A + B)	F = $\bar{A}\bar{B}$ PLUS (A + B) PLUS 1		
H L H H	$F = A + B$	F = (A + B)	F = (A + B) PLUS 1		
H H L L	F = 0	F = A PLUS A [†]	F = A PLUS A PLUS 1		
H H L H	$F = A\bar{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1		
H H H L	F = AB	F = $\bar{A}\bar{B}$ PLUS A	F = $\bar{A}\bar{B}$ PLUS A PLUS 1		
H H H H	F = A	F = A	F = A PLUS 1		

TABLE 2

SELECTION	M = H LOGIC FUNCTIONS			ACTIVE-HIGH DATA	
				M = L; ARITHMETIC OPERATIONS	
				$\bar{C}_n = H$ (no carry)	$C_n = L$ (with carry)
L L L L	$F = \bar{A}$	F = A	F = A PLUS 1		
L L L H	$F = \overline{A+B}$	F = A + B	F = (A + B) PLUS 1		
L L H L	$F = \bar{A}\bar{B}$	F = A + \bar{B}	F = (A + \bar{B}) PLUS 1		
L L H H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO		
L H L L	$F = \bar{A}\bar{B}$	F = A PLUS $\bar{A}\bar{B}$	F = A PLUS $\bar{A}\bar{B}$ PLUS 1		
L H L H	$F = \bar{B}$	F = (A + B) PLUS $\bar{A}\bar{B}$	F = (A + B) PLUS $\bar{A}\bar{B}$ PLUS 1		
L H H L	$F = A \odot B$	F = A MINUS B MINUS 1	F = A MINUS B		
L H H H	$F = A\bar{B}$	F = $\bar{A}\bar{B}$ MINUS 1	F = $\bar{A}\bar{B}$		
H L L L	$F = \overline{A+B}$	F = A PLUS AB	F = A PLUS AB PLUS 1		
H L L H	$F = A \oplus B$	F = A PLUS B	F = A PLUS B PLUS 1		
H L H L	F = B	F = (A + \bar{B}) PLUS AB	F = (A + \bar{B}) PLUS AB PLUS 1		
H L H H	F = AB	F = AB MINUS 1	F = AB		
H H L L	F = 1	F = A PLUS A [†]	F = A PLUS A PLUS 1		
H H L H	$F = A + \bar{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1		
H H H L	$F = A + B$	F = (A + \bar{B}) PLUS A	F = (A + \bar{B}) PLUS A PLUS 1		
H H H H	F = A	F = A MINUS 1	F = A		

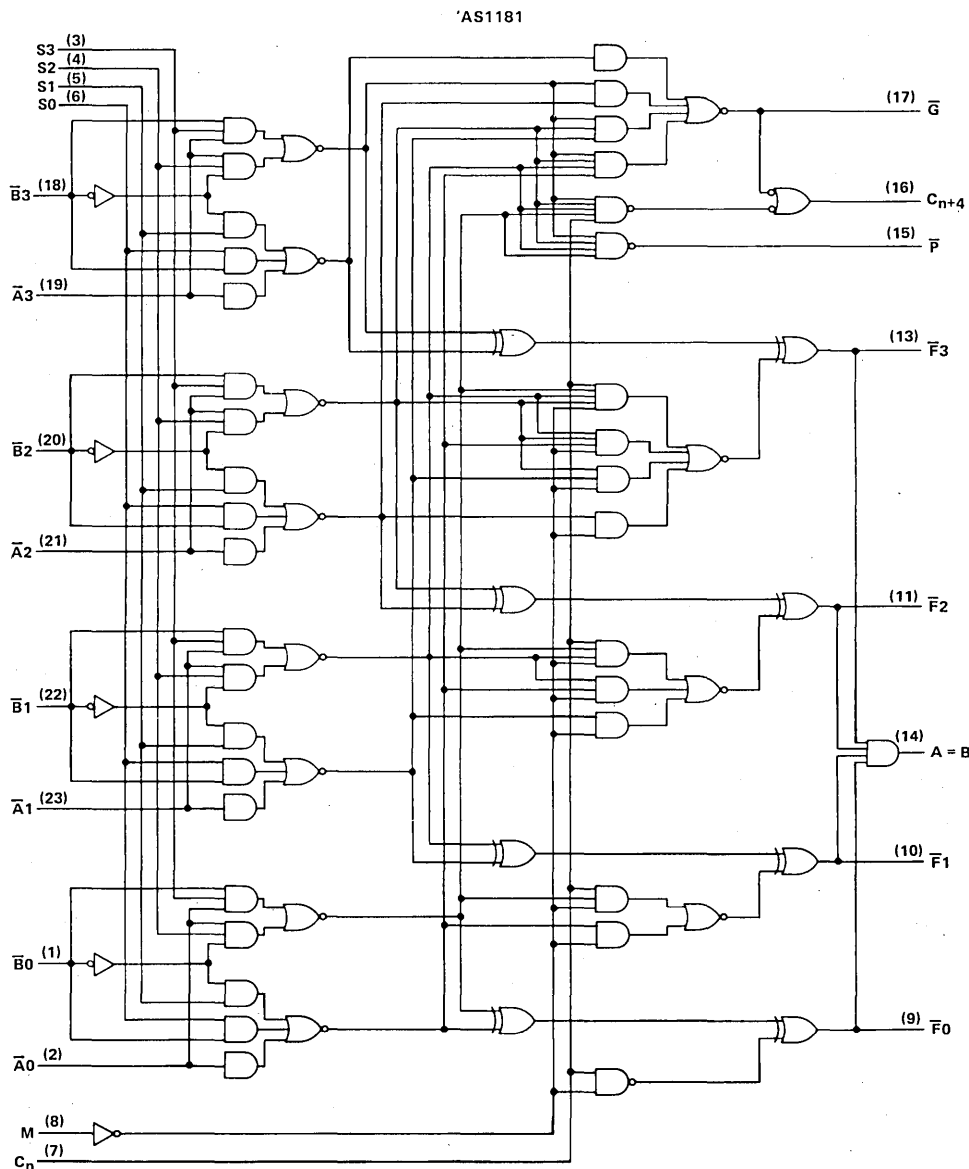
[†]Each bit is shifted to the next more significant position.

2

LSI Devices

SN54AS1181, SN74AS1181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

logic diagram (positive logic)



2
LSI Devices

SN54AS1181, SN74AS1181

ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC}	7 V
Input voltage	7 V
Off-state output voltage (A = B output only)	7 V
Operating free-air temperature range: SN54AS1181	-55°C to 125°C
SN74AS1181	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54AS1181			SN74AS1181			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage	0.8			0.8			V
V _{OH}	High-level output voltage	5.5			5.5			V
I _{OH}	High-level output current	A = B output only		5.5		5.5		mA
		All outputs except A = B and \bar{G}		-2		-2		
		\bar{G} output		-3		-3		
I _{OL}	Low-level output current	All outputs except \bar{G}		20		20		mA
		\bar{G} output		48		48		
T _A	Operating free-air temperature	-55	125		0	70		°C

2

LSI Devices

SN54AS1181, SN74AS1181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS1181			SN74AS1181			UNIT	
		MIN	TYP†	MAX	MIN	TYP†	MAX		
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$	-1.2			-1.2			V	
V_{OH}	Any output except A = B	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $I_{OH} = -2 \text{ mA}$			$V_{CC} - 2$			V	
	\bar{G}	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -3 \text{ mA}$	2.4	3	2.4	3		V	
I_{OH}	A = B	$V_{CC} = 4.5 \text{ V}$, $V_{OH} = 5.5 \text{ V}$	0.1			0.1			mA
V_{OL}	Any output except \bar{G}	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 20 \text{ mA}$	0.3	0.5	0.3	0.5		V	
	\bar{G}	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 48 \text{ mA}$	0.4	0.5	0.4	0.5		V	
I_I	M input	$V_{CC} = 5.5 \text{ V}$, $V_I = 7 \text{ V}$	0.1			0.1			mA
	Any A or B input		0.3			0.3			
	Any S input		0.4			0.4			
	Carry input		0.6			0.6			
I_{IH}	M input	$V_{CC} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$	20			20			μA
	Any A or B input		60			60			
	Any S input		80			80			
	Carry input		120			120			
I_{IL}	M input	$V_{CC} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$	-0.5			-0.5			mA
	Any A or B input		-1.5			-1.5			
	Any S input		-2			-2			
	Carry input		-3			-3			
I_O^\ddagger	All outputs except A = B and \bar{G}	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.25 \text{ V}$	-30	-112	-30	-112		mA	
	\bar{G}		-30	-125	-30	-125			
I_{CC}	$V_{CC} = 5.5 \text{ V}$		74	117	74	117		mA	

†All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

2

LSI Devices

SN54AS1181, SN74AS1181
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX				UNIT
				SN54AS1181		SN74AS1181		
				MIN	MAX	MIN	MAX	
t _{PLH}	C _n	C _{n+4}		3	9	3	8.5	ns
t _{PHL}				2	7	2	6.5	
t _{PLH}	Any A or B	C _{n+4}	M=0 V, S1=S2=0 V, S0=S3=4.5 V (SUM mode)	3.5	13	5	12	ns
t _{PHL}				3.5	12.5	5	12	
t _{PLH}	Any A or B	C _{n+4}	M=0 V, S0=S3=0 V, S1=S2=4.5 V (DIFF mode)	5	14.5	5	13	ns
t _{PHL}				5	13.5	5	12.5	
t _{PLH}	C _n	Any F	M=0 V (SUM or DIFF mode)	3	10.5	3	9	ns
t _{PHL}				3	8	3	7.5	
t _{PLH}	Any A or B	G	M=0 V, S1=S2=0 V, S0=S3=4.5 V (SUM mode)	3	8.5	3	8	ns
t _{PHL}				2	7	2	6	
t _{PLH}	Any A or B	G	M=0 V, S0=S3=0 V, S1=S2=4.5 V (DIFF mode)	3	10.5	3	9.5	ns
t _{PHL}				2	9	2	7	
t _{PLH}	Any A or B	P	M=0 V, S1=S2=0 V, S0=S3=4.5 V (SUM mode)	3	8.5	3	7.5	ns
t _{PHL}				2	7.5	2	6	
t _{PLH}	Any A or B	P	M=0 V, S0=S3=0 V, S1=S2=4.5 V (DIFF mode)	3	10.5	3	9	ns
t _{PHL}				3	8.5	3	8	
t _{PLH}	Ai or Bi	Fi	M=0 V, S1=S2=0 V, S0=S3=4.5 V (SUM mode)	3	11	3	9.5	ns
t _{PHL}				3	9	3	7.5	
t _{PLH}	Ai or Bi	Fi	M=0 V, S0=S3=0 V, S1=S2=4.5 V (DIFF mode)	3	12	3	10.5	ns
t _{PHL}				3	11	3	9.5	
t _{PLH}	Any A or B	Any F	M=0 V, S1=S2=0 V, S0=S3=4.5 V (SUM mode)	3	13.5	3	12	ns
t _{PHL}				3	13	3	11.5	
t _{PLH}	Any A or B	Any F	M=0 V, S0=S3=0 V, S1=S2=4.5 V (DIFF mode)	3	16	3	14.5	ns
t _{PHL}				3	13	3	12.5	
t _{PLH}	Ai or Bi	Fi	M=4.5 V (LOGIC mode)	3	12.5	3	11	ns
t _{PHL}				3	10	3	9.5	
t _{PLH}	Any A or B	A=B	M=0 V, S0=S3=0 V, S1=S2=4.5 V (DIFF mode)	4	19	4	17	ns
t _{PHL}				5	18.5	5	15	
t _{PLH}	Any S	Any F	M=0 V (ARITH mode)	3	12.5	3	11	ns
t _{PHL}				3	11.5	3	11	
t _{PLH}	Any S	A=B	M=0 V (ARITH mode)	5	20	5	18	ns
t _{PHL}				5	21	5	18	
t _{PLH}	Any S	C _{n+4}	M=4.5 V (LOGIC mode)	2	16.5	4.5	15.5	ns
t _{PHL}				3	12.5	3	12	
t _{PLH}	Any S	G	M=0 V (ARITH mode)	3	9.5	3	9	ns
t _{PHL}				2	6.5	2	6	
t _{PLH}	Any S	P	M=4.5 V (LOGIC mode)	3	8.5	3	7.5	ns
t _{PHL}				2	6.5	2	6.5	
t _{PLH}	M	Any F	S1=S2=0 V, S0=S3=4.5 V (SUM mode)	5	12	5	11.5	ns
t _{PHL}				5	12	5	11.5	
t _{PLH}	M	A=B	S1=S2=0 V, S0=S3=4.5 V (SUM mode)	7	19	7	17.5	ns
t _{PHL}				8	21	8	17.5	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

2
LSI Devices

SN54AS1181, SN74AS1181
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

PARAMETER MEASUREMENT INFORMATION

SUM MODE TEST TABLE
 FUNCTION INPUTS: S0 - S3 = 4.5 V, S1 - S2 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH}	\bar{A}_i	\bar{B}_i	None	Remaining \bar{A} and \bar{B}	C_n	\bar{F}_i	In-Phase
t_{PHL}							
t_{PLH}	B_i	\bar{A}_i	None	Remaining \bar{A} and \bar{B}	C_n	\bar{F}_i	In-Phase
t_{PHL}							
t_{PLH}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{P}	In-Phase
t_{PHL}							
t_{PLH}	B_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{P}	In-Phase
t_{PHL}							
t_{PLH}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{B}	Remaining \bar{A} , C_n	\bar{G}	In-Phase
t_{PHL}							
t_{PLH}	B_i	None	\bar{A}_i	Remaining \bar{B}	Remaining \bar{A} , C_n	\bar{G}	In-Phase
t_{PHL}							
t_{PLH}	C_n	None	None	All \bar{A}	All \bar{B}	Any \bar{F} or C_{n+4}	In-Phase
t_{PHL}							
t_{PLH}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{B}	Remaining \bar{A} , C_n	C_{n+4}	Out-of-Phase
t_{PHL}							
t_{PLH}	B_i	None	\bar{A}_i	Remaining \bar{B}	Remaining \bar{A} , C_n	C_{n+4}	Out-of-Phase
t_{PHL}							
t_{PLH}	Any \bar{A}	None	\bar{B}_i	Remaining \bar{B} , \bar{A}_3	Remaining \bar{A} , C_n	Any \bar{F}	In-Phase
t_{PHL}							
t_{PLH}	Any \bar{B}	None	\bar{A}_i	Remaining \bar{A} , \bar{B}_3	Remaining \bar{B} , C_n	Any \bar{F}	In-Phase
t_{PHL}							

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

2

LSI Devices

SN54AS1181, SN74AS1181
 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

PARAMETER MEASUREMENT INFORMATION

DIFF MODE TEST TABLE
 FUNCTION INPUTS: S1-S2=4.5 V, S0-S3=M=0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t _{PLH}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{A}	Remaining \bar{B}, C_n	\bar{F}_i	In-Phase
t _{PHL}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{A}	Remaining \bar{B}, C_n	\bar{F}_i	In-Phase
t _{PLH}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A}	Remaining \bar{B}, C_n	\bar{F}_i	Out-of-Phase
t _{PHL}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A}	Remaining \bar{B}, C_n	\bar{F}_i	Out-of-Phase
t _{PLH}	\bar{A}_i	None	\bar{B}_i	None	Remaining \bar{A} and \bar{B}, C_n	\bar{P}	In-Phase
t _{PHL}	\bar{A}_i	None	\bar{B}_i	None	Remaining \bar{A} and \bar{B}, C_n	\bar{P}	In-Phase
t _{PLH}	\bar{B}_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B}, C_n	\bar{P}	Out-of-Phase
t _{PHL}	\bar{B}_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B}, C_n	\bar{P}	Out-of-Phase
t _{PLH}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B}, C_n	\bar{G}	In-Phase
t _{PHL}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B}, C_n	\bar{G}	In-Phase
t _{PLH}	\bar{B}_i	None	\bar{A}_i	None	Remaining \bar{A} and \bar{B}, C_n	\bar{G}	Out-of-Phase
t _{PHL}	\bar{B}_i	None	\bar{A}_i	None	Remaining \bar{A} and \bar{B}, C_n	\bar{G}	Out-of-Phase
t _{PLH}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{A}	Remaining \bar{B}, C_n	A = B	In-Phase
t _{PHL}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{A}	Remaining \bar{B}, C_n	A = B	In-Phase
t _{PLH}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A}	Remaining \bar{B}, C_n	A = B	Out-of-Phase
t _{PHL}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A}	Remaining \bar{B}, C_n	A = B	Out-of-Phase
t _{PLH}	C_n	None	None	All \bar{A} and \bar{B}	None	$C_n + 4$ or any \bar{F}	In-Phase
t _{PHL}	C_n	None	None	All \bar{A} and \bar{B}	None	$C_n + 4$ or any \bar{F}	In-Phase
t _{PLH}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A}, \bar{B}, C_n	$C_n + 4$	Out-of-Phase
t _{PHL}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A}, \bar{B}, C_n	$C_n + 4$	Out-of-Phase
t _{PLH}	\bar{B}_i	None	\bar{A}_i	None	Remaining \bar{A}, \bar{B}, C_n	$C_n + 4$	In-Phase
t _{PHL}	\bar{B}_i	None	\bar{A}_i	None	Remaining \bar{A}, \bar{B}, C_n	$C_n + 4$	In-Phase
t _{PLH}	Any \bar{A}	\bar{B}_i	None	\bar{A}_3	Remaining \bar{A}, \bar{B}, C_n	Any \bar{F}	In-Phase
t _{PHL}	Any \bar{A}	\bar{B}_i	None	\bar{A}_3	Remaining \bar{A}, \bar{B}, C_n	Any \bar{F}	In-Phase
t _{PLH}	Any \bar{B}	None	\bar{A}_i	\bar{A}_3	Remaining \bar{A}, \bar{B}, C_n	Any \bar{F}	Out-of-Phase
t _{PHL}	Any \bar{B}	None	\bar{A}_i	\bar{A}_3	Remaining \bar{A}, \bar{B}, C_n	Any \bar{F}	Out-of-Phase

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54AS1181, SN74AS1181
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

PARAMETER MEASUREMENT INFORMATION

LOGIC MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t _{PLH}	\bar{A}_i	\bar{B}	None	None	Remaining \bar{A} and \bar{B} , C _n	\bar{F}_i	Out-of-Phase
t _{PHL}							
t _{PLH}	\bar{B}_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B} , C _n	\bar{F}_i	Out-of-Phase
t _{PHL}							

INPUT BITS EQUAL/NOT EQUAL TEST TABLE

FUNCTION INPUTS: S0 = S3 = M = 4.5 V, S1 = S2 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t _{PLH}	\bar{A}_i	\bar{B}_i	None	Remaining \bar{A} and \bar{B} , C _n	None	\bar{P}	Out-of-Phase
t _{PHL}							
t _{PLH}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A} and \bar{B} , C _n	None	\bar{P}	Out-of-Phase
t _{PHL}							
t _{PLH}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{A} and \bar{B} , C _n	None	\bar{P}	In-Phase
t _{PHL}							
t _{PLH}	\bar{B}_i	None	\bar{A}_i	Remaining \bar{A} and \bar{B} , C _n	None	\bar{P}	In-Phase
t _{PHL}							
t _{PLH}	\bar{A}_i	\bar{B}_i	None	Remaining \bar{A} and \bar{B} , C _n	None	C _{n+4}	In-Phase
t _{PHL}							
t _{PLH}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A} and \bar{B} , C _n	None	C _{n+4}	In-Phase
t _{PHL}							
t _{PLH}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{A} and \bar{B} , C _n	None	C _{n+4}	Out-of-Phase
t _{PHL}							
t _{PLH}	\bar{B}_i	None	\bar{A}_i	Remaining \bar{A} and \bar{B} , C _n	None	C _{n+4}	Out-of-Phase
t _{PHL}							

INPUT PAIRS HIGH/NOT HIGH TEST TABLE

FUNCTION INPUTS: S2 = M = 4.5 V, S0 = S1 = S3 = 0V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5V	APPLY GND		
t _{PLH}	\bar{A}_i	\bar{B}_i	None	Remaining \bar{A} , C _n	Remaining \bar{B}	\bar{P}	In-Phase
t _{PHL}							
t _{PLH}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{B} , C _n	Remaining \bar{A}	\bar{P}	In-Phase
t _{PHL}							
t _{PLH}	\bar{A}_i	\bar{B}_i	None	Remaining \bar{A} , C _n	Remaining \bar{B}	C _{n+4}	Out-of-Phase
t _{PHL}							
t _{PLH}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{B} , C _n	Remaining \bar{A}	C _{n+4}	Out-of-Phase
t _{PHL}							

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

2
LSI Devices

SN54AS1181, SN74AS1181
 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

PARAMETER MEASUREMENT INFORMATION

SELECT INPUT/LOGIC MODE TEST TABLE
 FUNCTION INPUTS: M = 4.5 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t _{PLH}	Any	—	—	Remaining \bar{B}	\bar{A}, \bar{B}_0, C_n	C _{n+4}	Out-of-Phase
t _{PHL}	S	—	—	Remaining \bar{B}	\bar{A}, \bar{B}_0, C_n	C _{n+4}	Out-of-Phase
t _{PLH}	Any	—	—	\bar{B}, \bar{A}_2	Remaining \bar{A}, C_n	\bar{P}	In-Phase
t _{PHL}	S	—	—	\bar{B}, \bar{A}_2	Remaining \bar{A}, C_n	\bar{P}	In-Phase

SELECT INPUT/ARITH MODE TEST TABLE
 FUNCTION INPUTS: M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t _{PLH}	Any	—	—	Remaining \bar{A} and \bar{B}, C_n	\bar{A}_0, \bar{B}_0	Any \bar{F}	In-Phase
t _{PHL}	S	—	—	Remaining \bar{A} and \bar{B}, C_n	\bar{A}_0, \bar{B}_0	\bar{F}	In-Phase
t _{PLH}	Any	—	—	Remaining \bar{A} and \bar{B}, C_n	\bar{A}_0, \bar{B}_0	A = B	In-Phase
t _{PHL}	S	—	—	Remaining \bar{A} and \bar{B}, C_n	\bar{A}_0, \bar{B}_0	A = B	In-Phase
t _{PLH}	Any	—	—	Remaining \bar{A} and \bar{B}, C_n	\bar{A}_0, \bar{B}_0	\bar{G}	In-Phase
t _{PHL}	S	—	—	Remaining \bar{A} and \bar{B}, C_n	\bar{A}_0, \bar{B}_0	\bar{G}	In-Phase

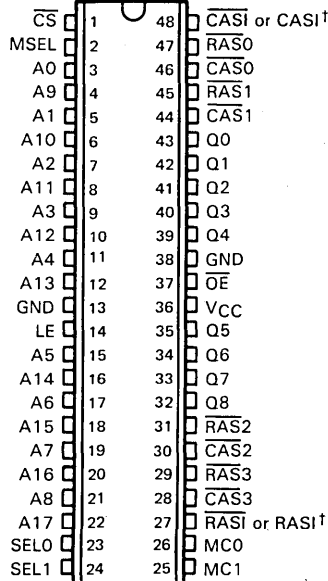
MODE INPUT/SUM MODE TEST TABLE
 FUNCTION INPUTS: S₀ - S₃ = 4.5 V, S₁ - S₂ = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t _{PLH}	M	—	—	Remaining \bar{A} and \bar{B}	$\bar{B}_2, \bar{A}_2, C_n$	Any \bar{F}	In-Phase
t _{PHL}		—	—	Remaining \bar{A} and \bar{B}	$\bar{B}_2, \bar{A}_2, C_n$	\bar{F}	In-Phase
t _{PLH}	M	—	—	Remaining \bar{A} and \bar{B}	$\bar{B}_1, \bar{A}_1, C_n$	A = B	In-Phase
t _{PHL}		—	—	Remaining \bar{A} and \bar{B}	$\bar{B}_1, \bar{A}_1, C_n$	A = B	In-Phase

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- Provides Control for 16K, 64K, and 256K Dynamic RAMs
- Highest-Order Two-Address Bits Select One of Four Banks of RAMs
- Supports Scrubbing Operations and Nibble-Mode Access
- Separate Output Enable for Multi-Channel Access to Memory
- 48-Pin Dual-In-Line Package
- 'ALS2968 is Designed to be Interchangeable with AMD AM2968

SN54ALS2967, SN54ALS2968 ... JD PACKAGE
SN74ALS2967, SN74ALS2968 ... JD OR N PACKAGE
(TOP VIEW)



description

The 'ALS2967 and 'ALS2968 dynamic memory controllers (DMCs) are designed for use in today's high-performance memory systems. The DMC acts as the address controller between any processor and dynamic memory array.

Two versions are provided that help simplify interfacing to the system dynamic timing controller. The 'ALS2967 offers active-low Row Address Strobe Input ($\overline{\text{RAS}}$) and Column Address Strobe Input ($\overline{\text{CAS}}$), while the 'ALS2968 offers active-high Row Address Strobe Input (RAS) and Column Address Strobe Input (CAS) inputs.

Using two 9-bit address latches, the DMC will hold the row and column addresses for any DRAM up to 256K. These latches and the two row/column refresh address counters feed into a 9-bit, 4-input MUX for output to the dynamic RAM address lines. A 2-bit bank select latch is provided to select one of the four RAS and CAS outputs. The two bits are normally obtained from the two highest-order address bits.

The 'ALS2967 and 'ALS2968 have two basic modes of operation, read/write and refresh. During normal read/write operations, the row and column addresses are multiplexed to the dynamic RAM, with the corresponding RAS and CAS signals activated to strobe the addresses into the RAM. In the refresh mode, the two counters cycle through the refresh addresses. If memory scrubbing is not being implemented, only the row counter is used. When memory scrubbing is being performed, both the row and column counters are used to perform read-modify-write cycles. In this mode all RAS outputs will be active (low) while only one CAS output is active at a time.

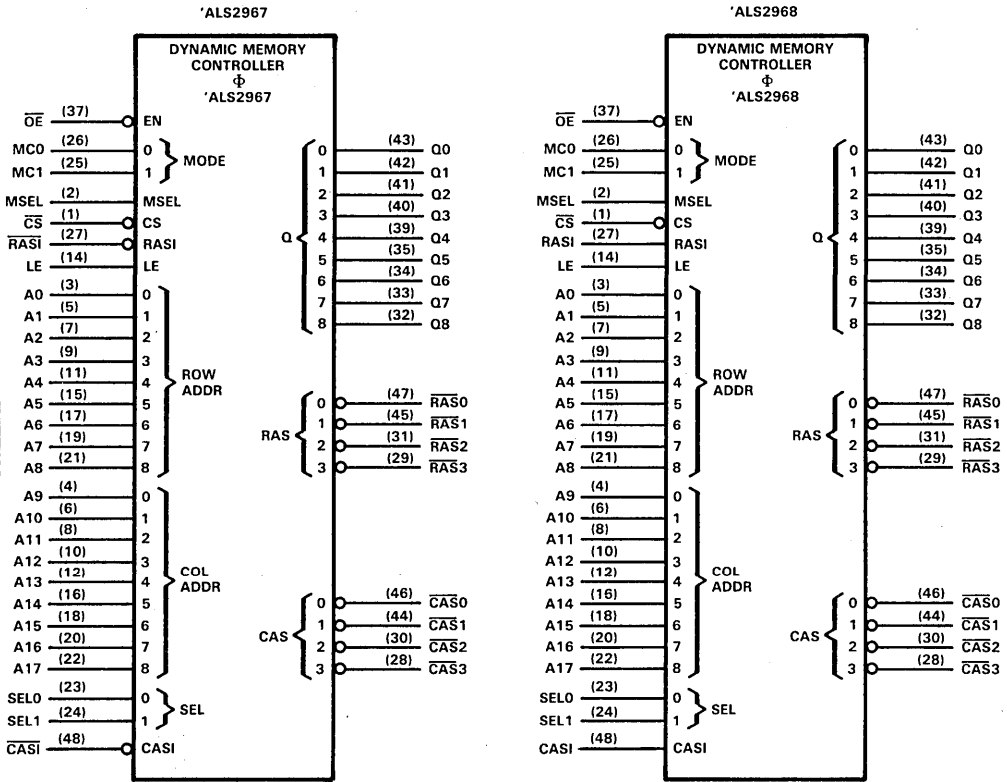
The SN54ALS2967 and SN54ALS2968 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS2967 and SN74ALS2968 are characterized for operation from 0°C to 70°C.

† 'ALS2967 has active-low inputs $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$; 'ALS2968 has active-high inputs CAS and RAS.



SN54ALS2967, SN74ALS2967, SN54ALS2968, SN74ALS2968
DYNAMIC MEMORY CONTROLLERS

logic symbols†



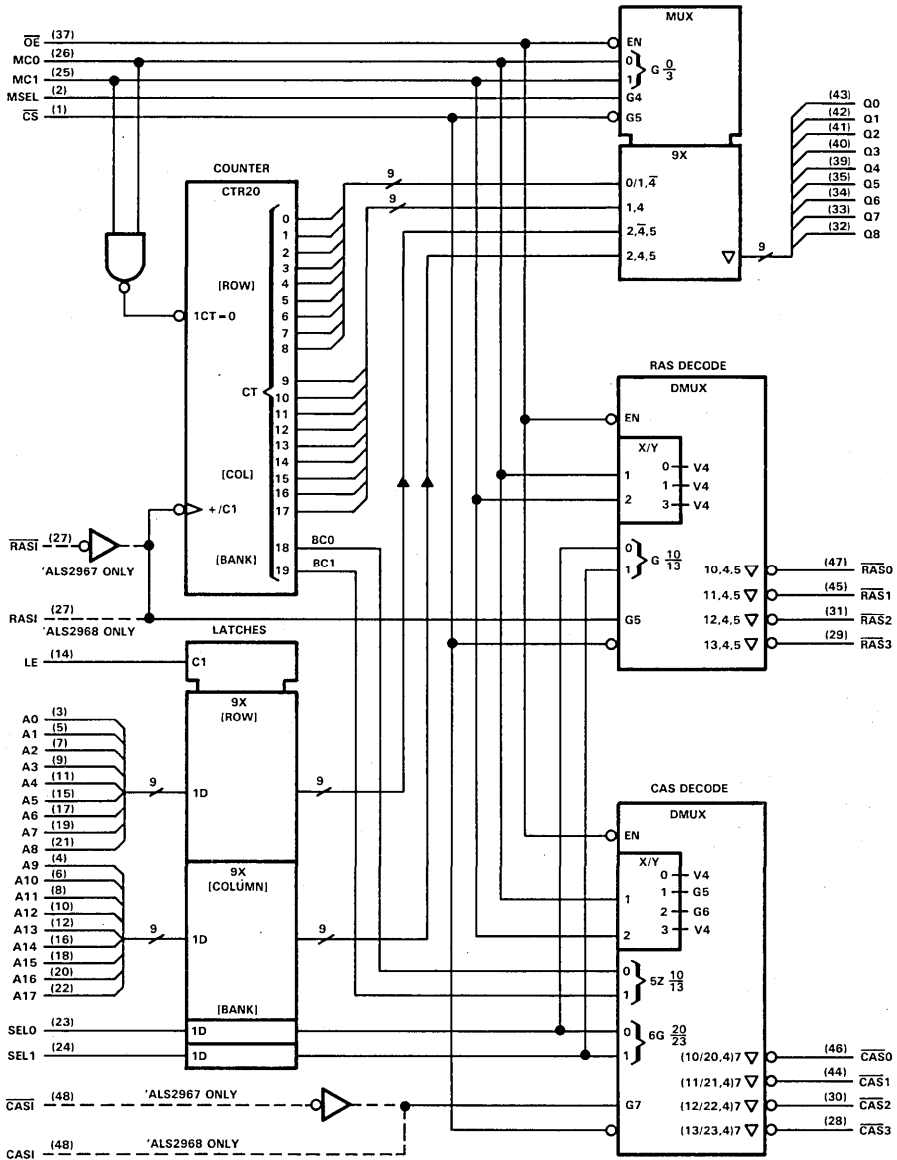
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

2

LSI Devices

SN54ALS2967, SN74ALS2967, SN54ALS2968, SN74ALS2968 DYNAMIC MEMORY CONTROLLERS

logic diagram (positive logic)



2
LSI Devices



**SN54ALS2967, SN74ALS2967, SN54ALS2968, SN74ALS2968
DYNAMIC MEMORY CONTROLLERS**

TABLE 1. PIN FUNCTION

PIN NAME	DESCRIPTION
A0-A17	Address Inputs. A0-A8 are latched in as the nine-bit row address for the DRAM. These inputs drive Q0-Q8 when the DMC is in the read/write mode and MSEL is low. A9-A17 are latched in as the column address, and will drive Q0-Q8 when MSEL is high and the DMC is in the read/write mode. The addresses are latched when the Latch Enable (LE) input signal is low.
SELO, SEL1	Bank Select. These two inputs are normally the two highest-order address bits and are used in the read/write mode to select which bank of memory will be receiving the \overline{RAS} and \overline{CAS} signals after \overline{RAS} ('ALS2967) or RASI ('ALS2968) and \overline{CAS} ('ALS2967) or CASI ('ALS2968) go active.
LE	Latch Enable. This active-high input causes the row, column, and bank select latches to become transparent, allowing the latches to accept new input data. A low input on LE latches the input data.
MSEL	Multiplexer Select. This input determines whether the row or column address will be sent to the memory address inputs. When MSEL is high, the column address is selected, while the row address is selected when MSEL is low. The address may come from either the address latch or refresh address counter depending on MCO and MC1 (see Mode Control Function Table).
\overline{CS}	Chip Select. This active-low input is used to enable the DMC. When \overline{CS} is active, the DMC operates normally in all four modes. When \overline{CS} goes high, the device will not enter the read/write mode. This allows other devices to access the same memory that the DMC is controlling.
\overline{OE}	Output Enable. This active-low input enables/disables the output signals. When \overline{OE} is high, the outputs of the DMC enter the high-impedance state.
MCO-MC1	Mode Controls. These inputs determine in which of the four modes the DMC operates. The description of each of the four operating modes is given in Table 2.
Q0-Q8	Address Outputs. These address outputs feed the DRAM address inputs and provide drive for memory systems having capacitance of up to 500 picofarads.
\overline{RAS} or RASI	Row Address Strobe Input. During the normal memory cycles, the decoded \overline{RAS} output ($\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, or $\overline{RAS3}$) is forced low after receipt of an active Row Address Strobe Input signal. In either Refresh mode, all four \overline{RAS} outputs will be low while the Row Address Strobe Input signal is active. The \overline{RAS} on the 'ALS2967 is an active-low input while on the 'ALS2968, RASI is an active-high input. (For more details see timing diagrams).
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe. Each of the Row Address Strobe outputs provides a \overline{RAS} signal to one of the four banks of dynamic memory. Each \overline{RAS} output will go low when selected by SELO and SEL1 after \overline{RAS} ('ALS2967) or RASI ('ALS2968) goes active. All four go low in response to \overline{RAS} ('ALS2967) or RASI ('ALS2968) while in the refresh mode.
\overline{CAS} or CASI	Column Address Strobe Input. This input going active causes the selected \overline{CAS} output to be forced low. The \overline{CAS} input on the 'ALS2967 is active low input while on the 'ALS2968, CASI is active high input. (For more details see timing diagrams.)
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe. During normal Read/Write cycles the two selected bits (SELO, SEL1) determine which \overline{CAS} output will go active following \overline{CAS} ('ALS2967) or CASI ('ALS2968) going active. When memory scrubbing is being performed, only the \overline{CAS} signal selected will be active. For non-scrubbing cycles, all four \overline{CAS} outputs will remain high.

**SN54ALS2967, SN74ALS2967, SN54ALS2968, SN74ALS2968
DYNAMIC MEMORY CONTROLLERS**

TABLE 2. MODE-CONTROL FUNCTION TABLE

MC1	MC0	OPERATING MODE
L	L	Refresh Mode without Scrubbing. Refresh cycles are performed with only the row counter being used to generate the addresses. In this mode, all four $\overline{\text{RAS}}$ outputs are active while the four $\overline{\text{CAS}}$ outputs remain high.
L	H	Refresh with Scrubbing/Initialize. During this mode, refresh cycles are done with both the row and column counters generating the addresses. MSEL is used to select either the row or the column counter. All four $\overline{\text{RAS}}$ outputs go low in response to $\overline{\text{RAS}}\overline{\text{I}}$ ('ALS2967) or $\overline{\text{RAS}}\overline{\text{I}}$ ('ALS2968), while only one $\overline{\text{CAS}}\overline{\text{N}}$ output goes low in response to $\overline{\text{CAS}}\overline{\text{I}}$ ('ALS2967) or $\overline{\text{CAS}}\overline{\text{I}}$ ('ALS2968). The bank counter keeps track of which $\overline{\text{CAS}}$ output goes active. This mode can also be used during system power-up so that the memory can be written with a known data pattern.
H	L	Read/Write. This mode is used to perform read/write cycles. Both the Row and Column addresses are multiplexed to the address output lines using MSEL. SEL0 and SEL1 are decoded to determine which $\overline{\text{RAS}}\overline{\text{N}}$ and $\overline{\text{CAS}}\overline{\text{N}}$ outputs will be active.
H	H	Clear Refresh Counters. This mode clears the three refresh counters (row, column, and bank) on the inactive transition of $\overline{\text{RAS}}\overline{\text{I}}$ ('ALS2967) or $\overline{\text{RAS}}\overline{\text{I}}$ ('ALS2968), putting them at start of the refresh sequence (see timing diagrams for more detail). In this mode, all four $\overline{\text{RAS}}$ outputs are driven low after the active edge of $\overline{\text{RAS}}\overline{\text{I}}$ ('ALS2967) or $\overline{\text{RAS}}\overline{\text{I}}$ ('ALS2968) so that DRAM wake-up cycles may also be performed.

SN54ALS2967, SN74ALS2967, SN54ALS2968, SN74ALS2968
DYNAMIC MEMORY CONTROLLERS

TABLE 3. ADDRESS OUTPUT FUNCTIONS

MODE	INPUTS				OUTPUTS Q0-Q8
	MC1	MC0	MSEL	\overline{CS}	
Refresh without scrubbing	L	L	X	X	Row counter address
Refresh with scrubbing	L	H	L	X	Row counter address
			H	X	Column counter address
Read/write	H	L	L	L	Row address [†]
			H	L	Column address [†]
			X	H	All L
Clear refresh counter [‡]	H	H	X	X	All L

TABLE 4. RAS OUTPUT FUNCTIONS

INPUTS						OUTPUTS				
'ALS2967 RASI	'ALS2968 RASI	MC1	MC0	SEL1 [†]	SEL0 [†]	\overline{CS}	RAS0	RAS1	RAS2	RAS3
L	H	L	L	X	X	X	L	L	L	L
L	H	L	H	X	X	X	L	L	L	L
L	H	H	L	L	L	L	L	H	H	H
				L	H	L	H	L	H	H
				H	L	L	H	H	L	H
				H	H	L	H	H	H	L
				X	X	H	H	H	H	
L	H	H	H	X	X	X	L	L	L	L
H	L	X	X	X	X	X	H	H	H	H

TABLE 5. CAS OUTPUT FUNCTIONS

INPUTS						OUTPUTS						
'ALS2967 CASI	'ALS2968 CASI	MC1	MC0	SEL1 [†]	SEL0 [†]	INTERNAL		\overline{CS}	$\overline{CAS0}$	$\overline{CAS1}$	$\overline{CAS2}$	$\overline{CAS3}$
						BC1	BC0					
L	H	L	L	X	X	X	X	X	H	H	H	H
L	H	L	H	X	X	L	L	X	L	H	H	H
						L	H	X	H	L	H	H
						H	L	X	H	H	L	H
						H	H	X	H	H	H	L
L	H	H	L	L	L	X	X	L	L	H	H	H
				L	H	X	X	L	H	L	H	H
				H	L	X	X	L	H	H	L	H
				H	H	X	X	L	H	H	H	L
				X	X	X	X	H	H	H	H	H
L	H	H	H	X	X	X	X	X	H	H	H	H
H	L	X	X	X	X	X	X	X	H	H	H	H

[†] If LE is low, outputs will be the levels entered when LE was last high. If LE is high, outputs will follow address inputs as selected by MSEL.
[‡] For 'ALS2967, clearing occurs on the low-to-high transition of RASI; for 'ALS2968, clearing occurs on the high-to-low transition of RASI.

SN54ALS2967, SN74ALS2967, SN54ALS2968, SN74ALS2968 DYNAMIC MEMORY CONTROLLERS

read/write operation details

During normal read/write operations, the row and column addresses are multiplexed to the dynamic RAM controlled by the MSEL input. The corresponding RASn and CASn output signals strobe the addresses into memory. The block diagram in Figure 1 shows a typical system interface for a one-megaword dynamic memory. The DMC is used to control the four banks of 256K memory.

For systems where addresses and data are multiplexed onto a single bus, the DMC uses latches (row, column, and bank) to hold the address information. Figure 5 shows a typical timing diagram using the input latches. The twenty input latches are transparent when latch enable (LE) is high, and latch the input data whenever LE is taken low. For systems in which the processor has separate address and data buses, LE may be permanently high (see timing diagram in Figure 4).

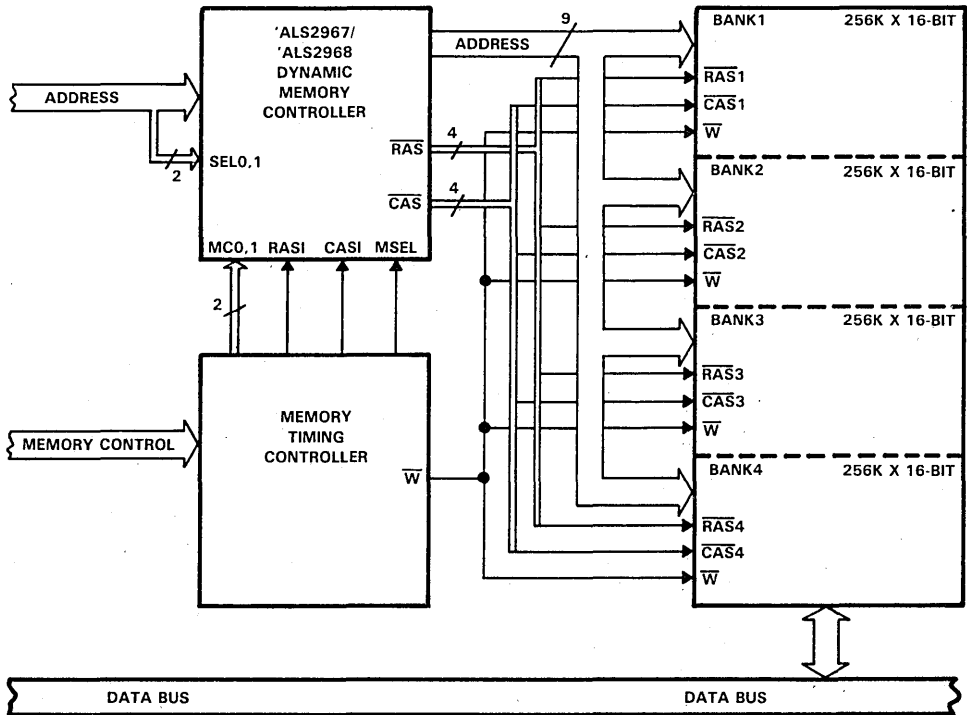


FIGURE 1. 1-MEGAWORD X 16-BIT DYNAMIC MEMORY

2
LSI Devices

**SN54ALS2967, SN74ALS2967, SN54ALS2968, SN74ALS2968
DYNAMIC MEMORY CONTROLLERS**

read/write operations (continued)

The DMC is designed with heavy-duty outputs that are capable of driving four banks of 16-bit words, including six checkbits used for error detection and correction.

In addition to heavy-duty output drivers, the outputs are designed with balanced output impedances (25 Ω both high and low). This feature optimizes the drive low characteristics, based on safe undershoot, while providing symmetrical drive high characteristics. It also eliminates the external resistors required to pull the outputs up to the MOS V_{OH} level ($V_{CC} - 1.5$ V).

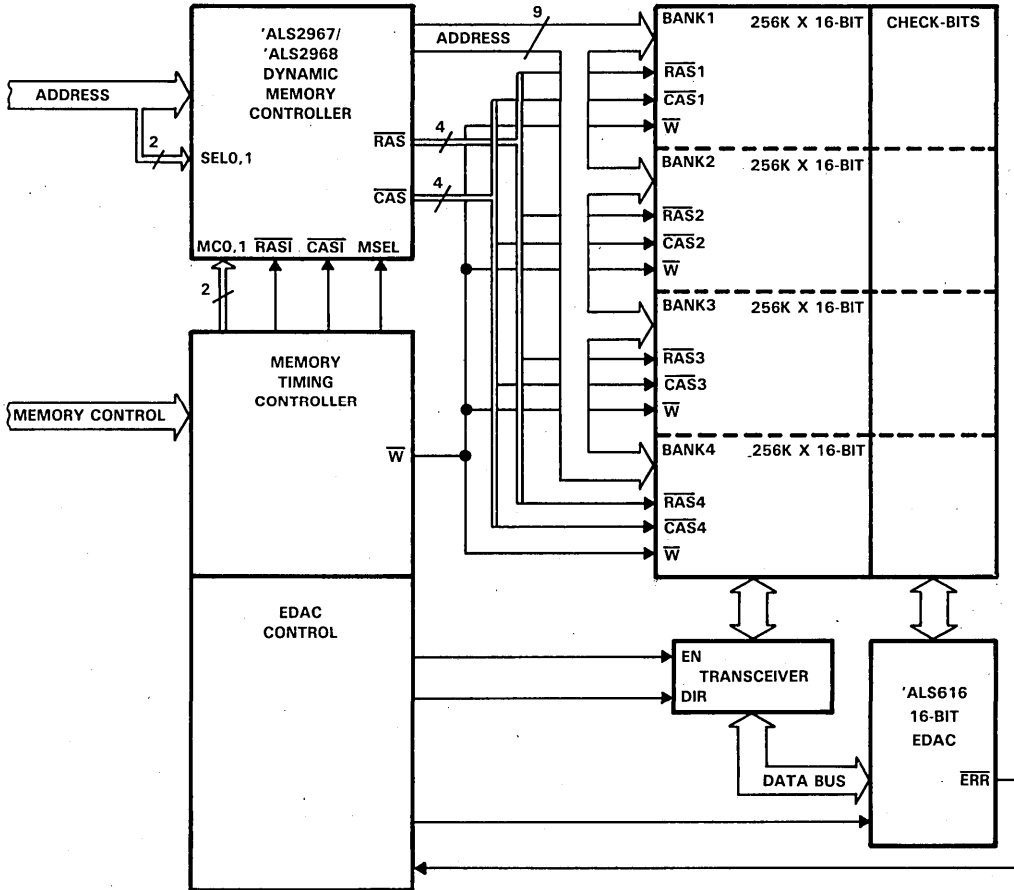


FIGURE 2. 1-MEGAWORD X 16-BIT DYNAMIC MEMORY WITH ERROR DETECTION AND CORRECTION

SN54ALS2967, SN74ALS2967, SN54ALS2968, SN74ALS2968 DYNAMIC MEMORY CONTROLLERS

memory expansion

With a 9-bit address path, the DMC can control up to one megaword when using 256K dynamic RAMs. If a larger memory size is desired, the DMC's chip select (\overline{CS}) makes it easy to expand the memory size by using additional DMCs. A four-megaword memory system is shown in Figure 3.

To maintain maximum performance in 32-bit applications, it is recommended that individual bus drivers be used for each bank.

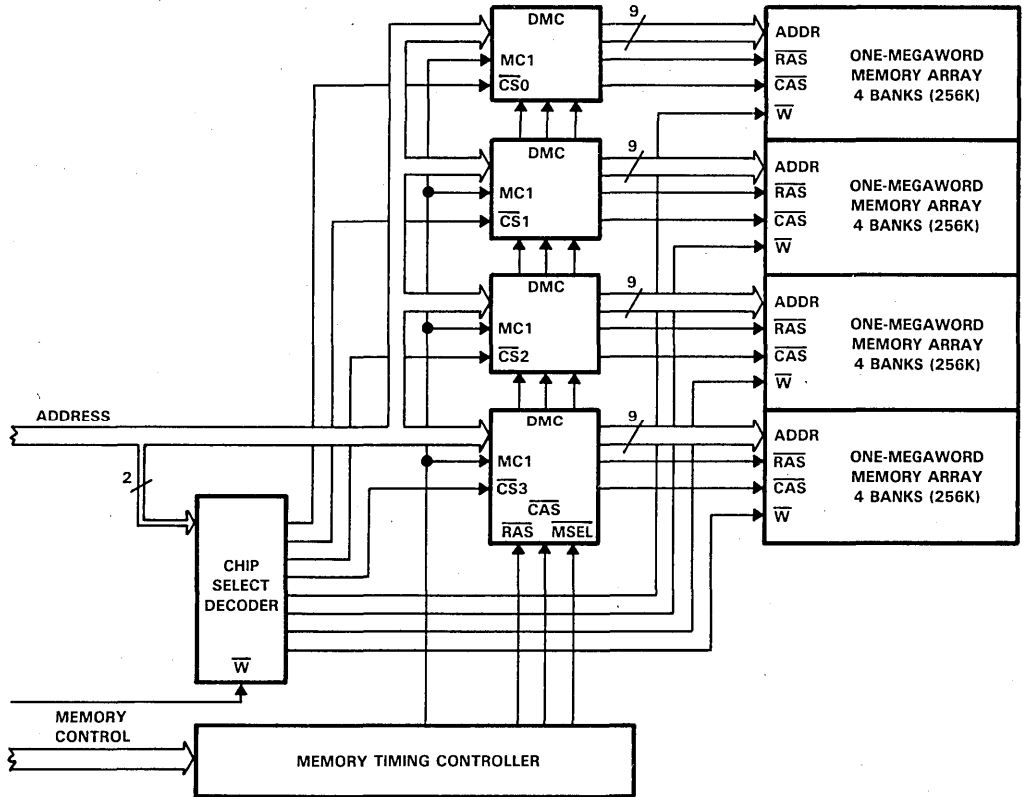


FIGURE 3. 4-MEGAWORD X 16-BIT DYNAMIC MEMORY

SN54ALS2967, SN74ALS2967, SN54ALS2968, SN74ALS2968 DYNAMIC MEMORY CONTROLLERS

refresh operations

The two 9-bit counters in the 'ALS2967 and 'ALS2968 support 128-, 256-, and 512-line refresh operations. Transparent, burst, synchronous, or asynchronous refresh modes are all possible. The refresh counters are advanced on the low-to-high transition of $\overline{\text{RASI}}$ on the 'ALS2967, and on the high-to-low transition of $\overline{\text{RASI}}$ on the 'ALS2968. The refresh counters are reset to zero on the low-to-high transition of $\overline{\text{RASI}}$ on the 'ALS2967, and on the high-to-low transition of $\overline{\text{RASI}}$ on the 'ALS2968, if MC1 and MCO are at a low logic level. See Figure 8 for additional timing details.

When performing refresh cycles without memory scrubbing (MC1 and MCO both low), all four $\overline{\text{RAS}}$ outputs go low, while all $\overline{\text{CAS}}$ outputs are driven high. Typical timing for this mode of operation is shown in Figure 6.

SN54ALS2967, SN74ALS2967, SN54ALS2968, SN74ALS2968 DYNAMIC MEMORY CONTROLLERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Voltage applied to disabled 3-state output	5.5 V
Operating free-air temperature range: SN54ALS2967, SN54ALS2968	-55°C to 125°C
SN74ALS2967, SN74ALS2968	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54ALS2967			SN74ALS2967			UNIT
		SN54ALS2968			SN74ALS2968			
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage	0.8			0.8			V
I_{OH}	High-level output current	-1			-2.6			mA
I_{OL}	Low-level output current	12			12			mA
t_w	Pulse duration	(23) \overline{RAS} low or RAS high		15	15		ns	
		(24) \overline{RAS} high or RAS low		15	15			
		(25) LE high		20	20			
t_{su}	Setup time	(26) A_n before $LE\downarrow$		5	5		ns	
		(27) $SELn$ before $LE\downarrow$		5	5			
		(28) MCO or $MC1$ before $\overline{RAS}\uparrow$ or $RAS\downarrow$		25	25			
		(29) $SELn$ before $\overline{RAS}\downarrow$ or $RAS\uparrow$		15	15			
t_h	Hold time	(30) A_n after $LE\downarrow$		5	5		ns	
		(31) $SELn$ after $LE\downarrow$		5	5			
T_A	Operating free-air temperature	-55		125	0		70	°C



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS2967		SN74ALS2967		UNIT
		SN54ALS2968		SN74ALS2968		
		MIN	TYP [†] MAX	MIN	TYP [†] MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$	-1.5		-1.5		V
V_{OH}	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -1\text{ mA}$	2.4	3.3			V
	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -2.6\text{ mA}$			2.4	3.2	
V_{OL}	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 1\text{ mA}$	0.15	0.5	0.15	0.5	V
	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 12\text{ mA}$	0.35	0.8	0.35	0.8	
I_{OL}^{\ddagger}	$V_{CC} = 4.5\text{ V}$, $V_O = 2\text{ V}$	30		30		mA
I_{OZH}	$V_{CC} = 5.5\text{ V}$, $V_O = 2.7\text{ V}$	20		20		μA
I_{OZL}	$V_{CC} = 5.5\text{ V}$, $V_O = 0.4\text{ V}$	-20		-20		μA
I_I	$V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$	0.1		0.1		mA
I_{IH}	$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$	20		20		μA
I_{IL}	$V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$	-0.1		-0.1		mA
I_O^{\S}	$V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$	-30	-112	-30	-112	mA
I_{CC}	$V_{CC} = 5.5\text{ V}$					mA

[†] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] Not more than one output should be tested at a time, and duration should not exceed 1 second.

[§] The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit output current, I_{OS} .

SN54ALS2967, SN74ALS2967 DYNAMIC MEMORY CONTROLLERS

ALS2967 switching characteristics, $C_L = 50 \text{ pF}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS [†]	SN54ALS2967			SN74ALS2967			UNIT
				MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
$t_{pd(1)}$	RAS \bar{I}	Any Q	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$ $T_A = \text{MIN to MAX}$		12			12		ns
$t_{pd(2)}$	RAS \bar{I}	RASn			10			10		ns
$t_{pd(3)}$	CAS \bar{I}	CASn			8			8		ns
$t_{pd(4)}$	Any A	Any Q			22			22		ns
$t_{pd(5)}$	MSEL	Any Q			14			14		ns
$t_{pd(6)}$	LE \bar{I}	Any Q			15			15		ns
$t_{pd(7)}$	LE \bar{I}	Any RAS			15			15		ns
$t_{pd(8)}$	LE \bar{I}	Any CAS			14			14		ns
$t_{pd(9)}$	MCO or MC1	Any Q			15			15		ns
$t_{pd(10)}$	MCO or MC1	Any RAS			14			14		ns
$t_{pd(11)}$	MCO or MC1	Any CAS			12			12		ns
$t_{pd(12)}$	\bar{CS}	Any Q			16			16		ns
$t_{pd(13)}$	\bar{CS}	Any RAS			12			12		ns
$t_{pd(14)}$	\bar{CS}	Any CAS			11			11		ns
$t_{pd(15)}$	SELO or SEL1	Any RAS			12			12		ns
$t_{pd(16)}$	SELO or SEL1	Any CAS			11			11		ns
$t_{en(17)}$	$\bar{OE}\bar{I}$	Any Q			14			14		ns
$t_{en(18)}$	$\bar{OE}\bar{I}$	Any RAS			13			13		ns
$t_{en(19)}$	$\bar{OE}\bar{I}$	Any CAS			13			13		ns
$t_{dis(20)}$	$\bar{OE}\bar{I}$	Any Q			15			15		ns
$t_{dis(21)}$	$\bar{OE}\bar{I}$	Any RAS			13			13		ns
$t_{dis(22)}$	$\bar{OE}\bar{I}$	Any CAS			13			13		ns

ALS2967 switching characteristics, $C_L = 150 \text{ pF}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS [†]	SN54ALS2967			SN74ALS2967			UNIT
				MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
$t_{pd(1)}$	RAS \bar{I}	Any Q	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$ $T_A = \text{MIN to MAX}$		17			17		ns
$t_{pd(2)}$	RAS \bar{I}	RASn			15			15		ns
$t_{pd(3)}$	CAS \bar{I}	CASn			14			14		ns
$t_{pd(4)}$	Any A	Any Q			27			27		ns
$t_{pd(5)}$	MSEL	Any Q			19			19		ns
$t_{pd(6)}$	LE \bar{I}	Any Q			20			20		ns
$t_{pd(7)}$	LE \bar{I}	Any RAS			20			20		ns
$t_{pd(8)}$	LE \bar{I}	Any CAS			19			19		ns
$t_{pd(9)}$	MCO or MC1	Any Q			20			20		ns
$t_{pd(10)}$	MCO or MC1	Any RAS			19			19		ns
$t_{pd(11)}$	MCO or MC1	Any CAS			17			17		ns
$t_{pd(12)}$	\bar{CS}	Any Q			19			19		ns
$t_{pd(13)}$	\bar{CS}	Any RAS			14			14		ns
$t_{pd(14)}$	\bar{CS}	Any CAS			14			14		ns
$t_{pd(15)}$	SELO or SEL1	Any RAS			15			15		ns
$t_{pd(16)}$	SELO or SEL1	Any CAS			14			14		ns

[†] See Figures 10, 11, 12, and 13 for test circuit and switching waveforms.

[‡] All typical values at $V_{CC} = 5 \text{ V, } T_A = 25^\circ\text{C}$.

SN54ALS2968, SN74ALS2968 DYNAMIC MEMORY CONTROLLERS

ALS2968 switching characteristics, $C_L = 50$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS†	SN54ALS2968			SN74ALS2968			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t _{pd(1)}	RASi	Any Q	V _{CC} = 4.5 V to 5.5 V, T _A = MIN to MAX	5	12	20	5	12	20	ns
t _{pd(2)}	RASi	RASn		3	10	18	3	10	18	ns
t _{pd(3)}	CASi	CASn		3	8	17	3	8	17	ns
t _{pd(4)}	Any A	Any Q		5	22	30	5	22	30	ns
t _{pd(5)}	MSEL	Any Q		3	14	20	3	14	20	ns
t _{pd(6)}	LE†	Any Q		15	25		15	25		ns
t _{pd(7)}	LE†	Any RAS		15	25		15	25		ns
t _{pd(8)}	LE†	Any CAS		14	24		14	24		ns
t _{pd(9)}	MCO or MC1	Any Q		5	15	25	5	15	25	ns
t _{pd(10)}	MCO or MC1	Any RAS		3	14	21	3	14	21	ns
t _{pd(11)}	MCO or MC1	Any CAS		3	12	19	3	12	19	ns
t _{pd(12)}	CS	Any Q		16	23		16	23		ns
t _{pd(13)}	CS	Any RAS		12	20		12	20		ns
t _{pd(14)}	CS	Any CAS		11	19		11	19		ns
t _{pd(15)}	SELO or SEL1	Any RAS		12	20		12	20		ns
t _{pd(16)}	SELO or SEL1	Any CAS		11	18		11	18		ns
t _{en(17)}	OE†	Any Q		14	21		14	21		ns
t _{en(18)}	OE†	Any RAS		13	19		13	19		ns
t _{en(19)}	OE†	Any CAS		13	19		13	19		ns
t _{dis(20)}	OE†	Any Q		15	22		15	22		ns
t _{dis(21)}	OE†	Any RAS		13	20		13	20		ns
t _{dis(22)}	OE†	Any CAS		13	20		13	20		ns

ALS2968 switching characteristics, $C_L = 150$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS†	SN54ALS2968			SN74ALS2968			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t _{pd(1)}	RASi	Any Q	V _{CC} = 4.5 V to 5.5 V, T _A = MIN to MAX	12	17	30	12	17	30	ns
t _{pd(2)}	RASi	RASn		9	15	23	9	15	23	ns
t _{pd(3)}	CASi	CASn		9	14	22	9	14	22	ns
t _{pd(4)}	Any A	Any Q		10	27	35	10	27	35	ns
t _{pd(5)}	MSEL	Any Q		9	19	26	9	19	26	ns
t _{pd(6)}	LE†	Any Q		20	28		20	28		ns
t _{pd(7)}	LE†	Any RAS		20	28		20	28		ns
t _{pd(8)}	LE†	Any CAS		19	27		19	27		ns
t _{pd(9)}	MCO or MC1	Any Q		10	20	27	10	20	27	ns
t _{pd(10)}	MCO or MC1	Any RAS		9	19	25	9	19	25	ns
t _{pd(11)}	MCO or MC1	Any CAS		9	17	23	9	17	23	ns
t _{pd(12)}	CS	Any Q		19	27		19	27		ns
t _{pd(13)}	CS	Any RAS		14	22		14	22		ns
t _{pd(14)}	CS	Any CAS		14	22		14	22		ns
t _{pd(15)}	SELO or SEL1	Any RAS		15	23		15	23		ns
t _{pd(16)}	SELO or SEL1	Any CAS		14	22		14	22		ns

† See Figures 10, 11, 12, and 13 for test circuit and switching waveforms.

‡ All typical values at V_{CC} = 5 V, T_A = 25°C.

2

LSI Devices

SN54ALS2967, SN74ALS2967, SN54ALS2968, SN74ALS2968 DYNAMIC MEMORY CONTROLLERS

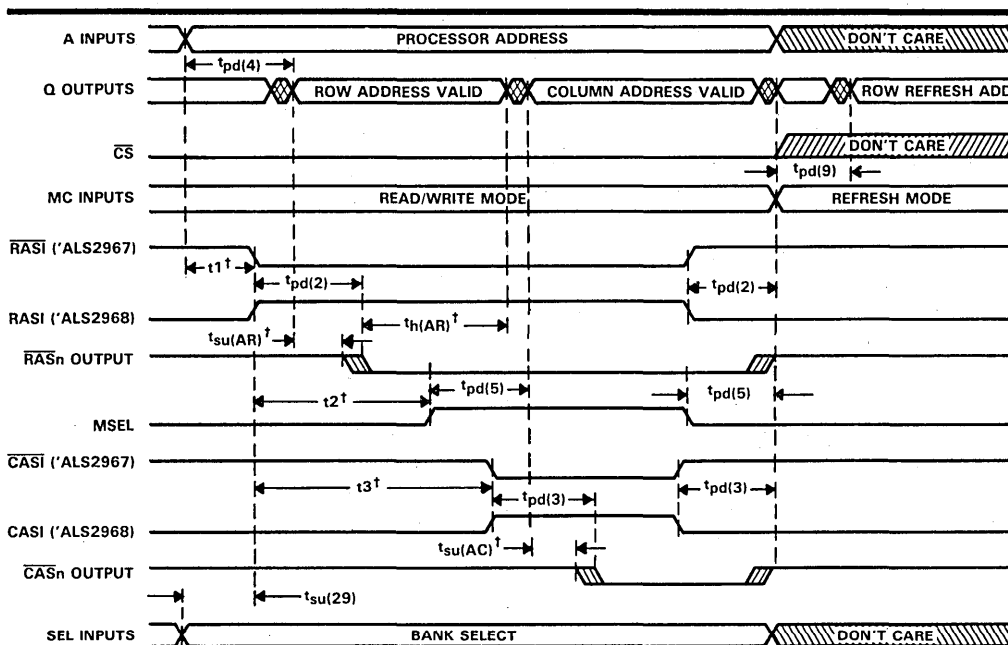


FIGURE 4. READ/WRITE CYCLE TIMING (MC1, MC0 = 1, 0), (LE = H)

[†] Parameters $t_{su(AR)}$, $t_{su(AC)}$, and $t_{h(AR)}$ are timing requirements of the dynamic RAM. Parameters $t1$, $t2$, and $t3$ represent the minimum timing requirements at the inputs to the DMC that guarantee DRAM timing specifications and maximum system performance. The minimum requirements for $t1$, $t2$, and $t3$ are as follows:

$$t1(\min) = t_{pd(4)} \max + t_{su(AR)} \min - t_{pd(2)} \min$$

$$t2(\min) = t_{pd(2)} \max + t_{h(AR)} \min - t_{pd(5)} \min$$

$$t3(\min) = t2 \min + t_{pd(5)} \max + t_{su(AC)} - t_{pd(3)} \min$$

See the DRAM data sheet for applicable $t_{su(AR)}$, $t_{su(AC)}$, and $t_{h(AR)}$. In addition, note that propagation delay times given in the above equations are functions of capacitive loading. The values used in these equations must relate to actual system capacitive loading.

**SN54ALS2967, SN74ALS2967, SN54ALS2968, SN74ALS2968
DYNAMIC MEMORY CONTROLLERS**

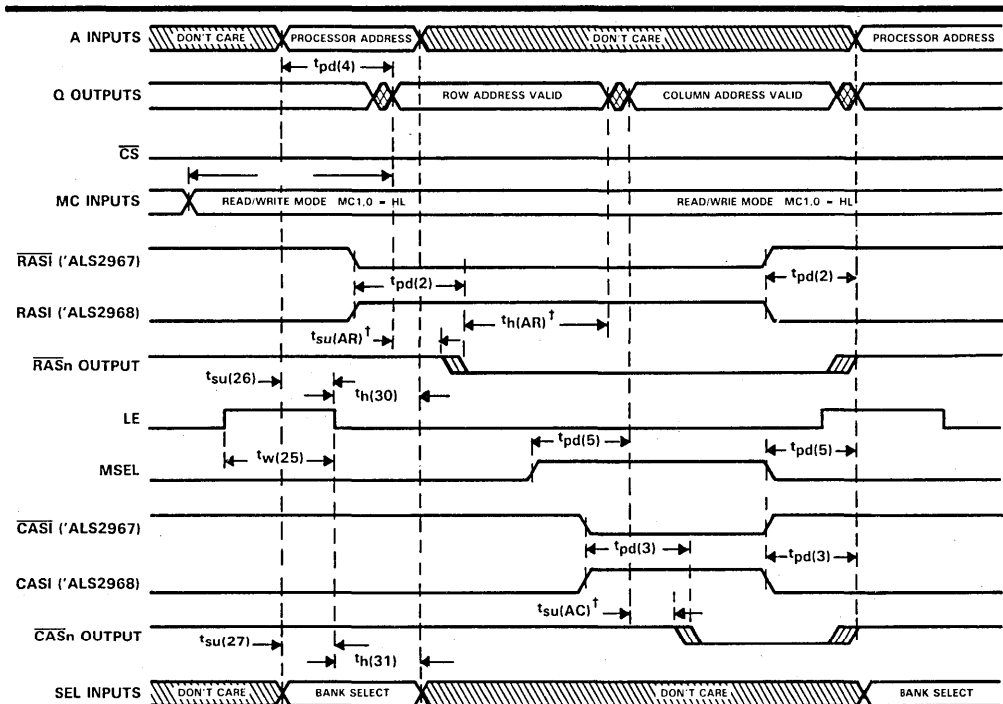


FIGURE 5. READ/WRITE CYCLE TIMING USING INPUT LATCHES (MC1, MCO = H, L)

[†] $t_{su(AR)}$, $t_{su(AC)}$, and $t_{h(AR)}$ are timing requirements of the dynamic RAM. See the DRAM data sheet for applicable specifications.

SN54ALS2967, SN74ALS2967, SN54ALS2968, SN74ALS2968
DYNAMIC MEMORY CONTROLLERS

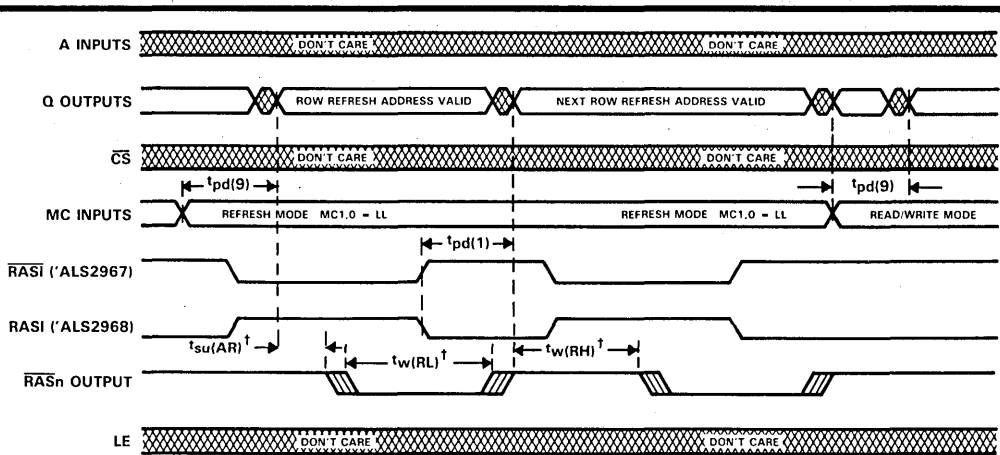


FIGURE 6. REFRESH CYCLE TIMING (MC1, MC0 = L, L) WITHOUT SCRUBBING

$t_{su(AR)}$, $t_{w(RL)}$, and $t_{w(RH)}$ are timing requirements of the dynamic RAM. See DRAM data sheet for applicable specifications.

2

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SN54ALS2967, SN74ALS2967, SN54ALS2968, SN74ALS2968
DYNAMIC MEMORY CONTROLLERS

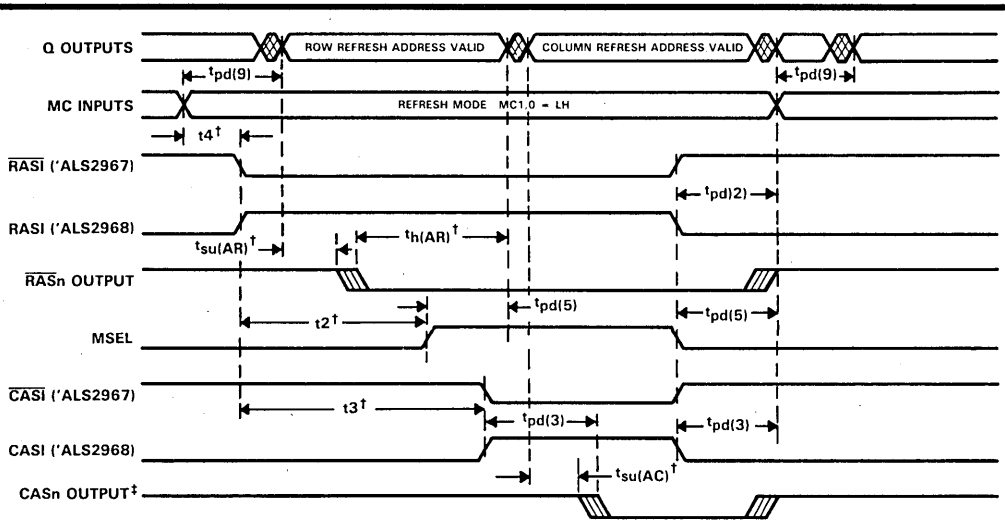


FIGURE 7. REFRESH CYCLE TIMING (MC1, MC0 = L, H) WITH MEMORY SCRUBBING

† Parameters $t_{su(AR)}$, $t_{su(AC)}$, and $t_{h(AR)}$ are timing requirements of the dynamic RAM. Parameters t_2 , t_3 , and t_4 represent the minimum timing requirements at the inputs to the DMC that guarantee DRAM timing specifications and maximum system performance. The minimum requirement for t_2 , t_3 , and t_4 are as follows:

$$t_2(\min) = t_{pd(2)} \max + t_{h(AR)} \min - t_{pd(5)} \min$$

$$t_3(\min) = t_2 \min + t_{pd(5)} \max + t_{su(AC)} - t_{pd(3)} \min$$

$$t_4(\min) = t_{pd(9)} \max + t_{su(AR)} \min - t_{pd(2)} \min$$

See the DRAM data sheet for applicable $t_{su(AR)}$, $t_{su(AC)}$, and $t_{h(AR)}$. In addition, note that propagation delay times given in the above equations are functions of capacitive loading. The values used in these equations must correspond to actual system capacitive loading.

† A \overline{CASn} output is selected by the bank counter. All other \overline{CASn} outputs will remain high.

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SN54ALS2967, SN74ALS2967, SN54ALS2968, SN74ALS2968
 DYNAMIC MEMORY CONTROLLERS

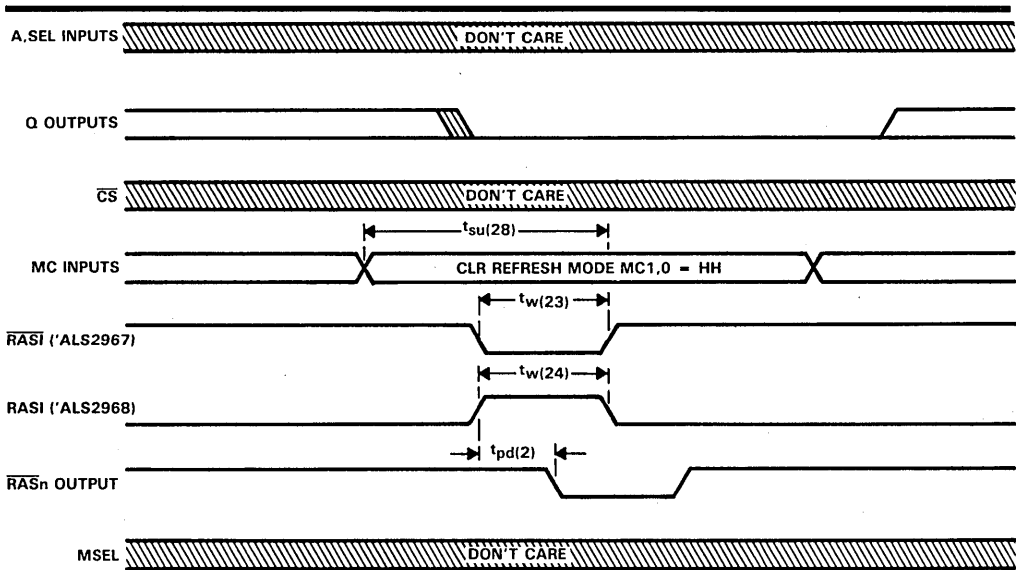
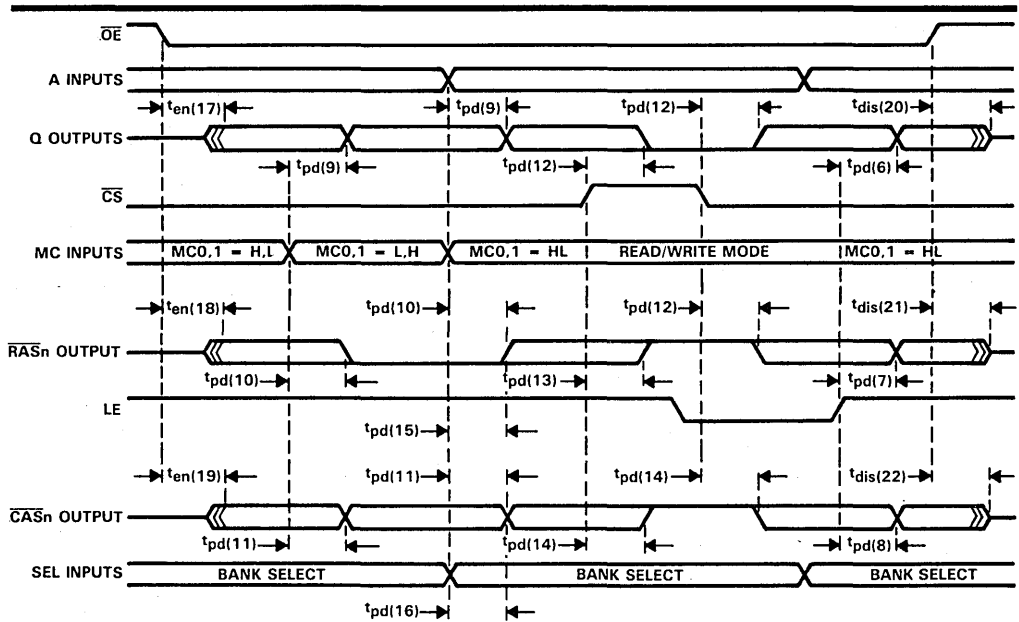


FIGURE 8. REFRESH COUNTER RESET (MC1, MC0 = H, H)

SN54ALS2967, SN74ALS2967, SN54ALS2968, SN74ALS2968
DYNAMIC MEMORY CONTROLLERS



$\overline{\text{RASn}}$ ('ALS2967) = L, RASn ('ALS2968) = H, MSEL = H or L, $\overline{\text{CASn}}$ ('ALS2967) = L, CASn ('ALS2968) = H

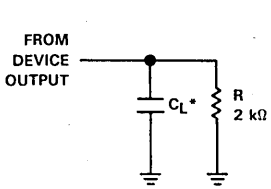
FIGURE 9. MISCELLANEOUS TIMING

2

LSI Devices

SN54ALS2967, SN74ALS2967, SN54ALS2968, SN74ALS2968
DYNAMIC MEMORY CONTROLLERS

SWITCHING TEST CIRCUIT



* t_{pd} specified at $C_L = 50, 150 \text{ pF}$

FIGURE 10. CAPACITIVE LOAD SWITCHING

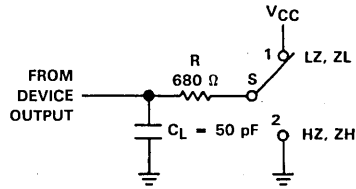


FIGURE 11. THREE-STATE ENABLE/DISABLE

TYPICAL SWITCHING CHARACTERISTICS

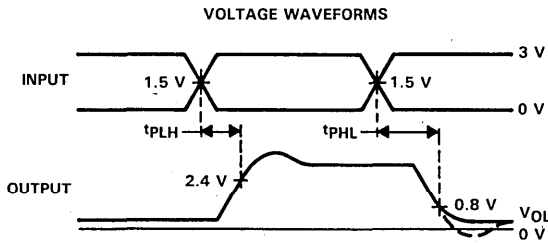
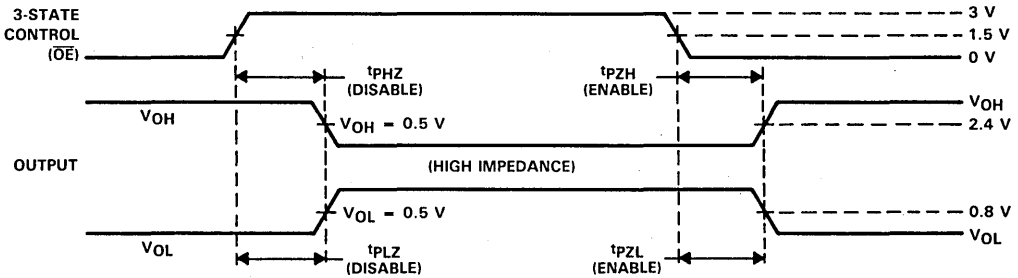


FIGURE 12. OUTPUT DRIVE LEVELS

THREE-STATE TIMING



NOTE: Decoupling is needed for all AC tests

FIGURE 13. THREE-STATE CONTROL LEVELS

- Provides Control for 16K, 64K, 256K, and 1M Dynamic RAMs
- Highest-Order Two-Address Bits Select One of Four Banks of RAMs
- Supports Scrubbing Operations and Nibble-Mode Access
- Separate Output Enable for Multi-Channel Access to Memory
- 52-Pin Dual-In-Line Package

description

The 'ALS6301 and 'ALS6302 dynamic memory controllers (DMCs) are designed for use in today's high-performance memory systems. The DMC acts as the address controller between any processor and dynamic memory array.

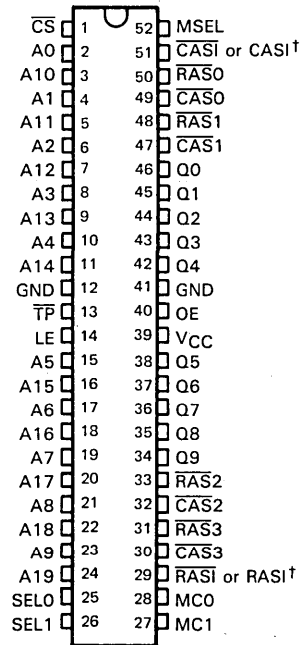
Two versions are provided that help simplify interfacing to the system dynamic timing controller. The 'ALS6301 offers active-low Row Address Strobe Input ($\overline{\text{RAS}}$) and Column Address Strobe Input ($\overline{\text{CAS}}$), while the 'ALS6302 offers active-high Row Address Strobe Input (RASI) and Column Address Strobe Input (CASI) inputs.

Using two 10-bit address latches, the DMC will hold the row and column addresses for any DRAM up to 1M. These latches and the two row/column refresh address counters feed into a 10-bit, 4-input MUX for output to the dynamic RAM address lines. A 2-bit bank select latch is provided to select one of the four $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ outputs. The two bits are normally obtained from the two highest-order address bits.

The 'ALS6301 and 'ALS6302 have two basic modes of operation, read/write and refresh. During normal read/write operations, the row and column addresses are multiplexed to the dynamic RAM, with the corresponding $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals activated to strobe the addresses into the RAM. In the refresh mode, the two counters cycle through the refresh addresses. If memory scrubbing is not being implemented, only the row counter is used. When memory scrubbing is being performed, both the row and column counters are used to perform read-modify-write cycles. In this mode all $\overline{\text{RAS}}$ outputs will be active (low) while only one $\overline{\text{CAS}}$ output is active at a time.

The SN54ALS6301 and SN54ALS6302 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS6301 and SN74ALS6302 are characterized for operation from 0°C to 70°C .

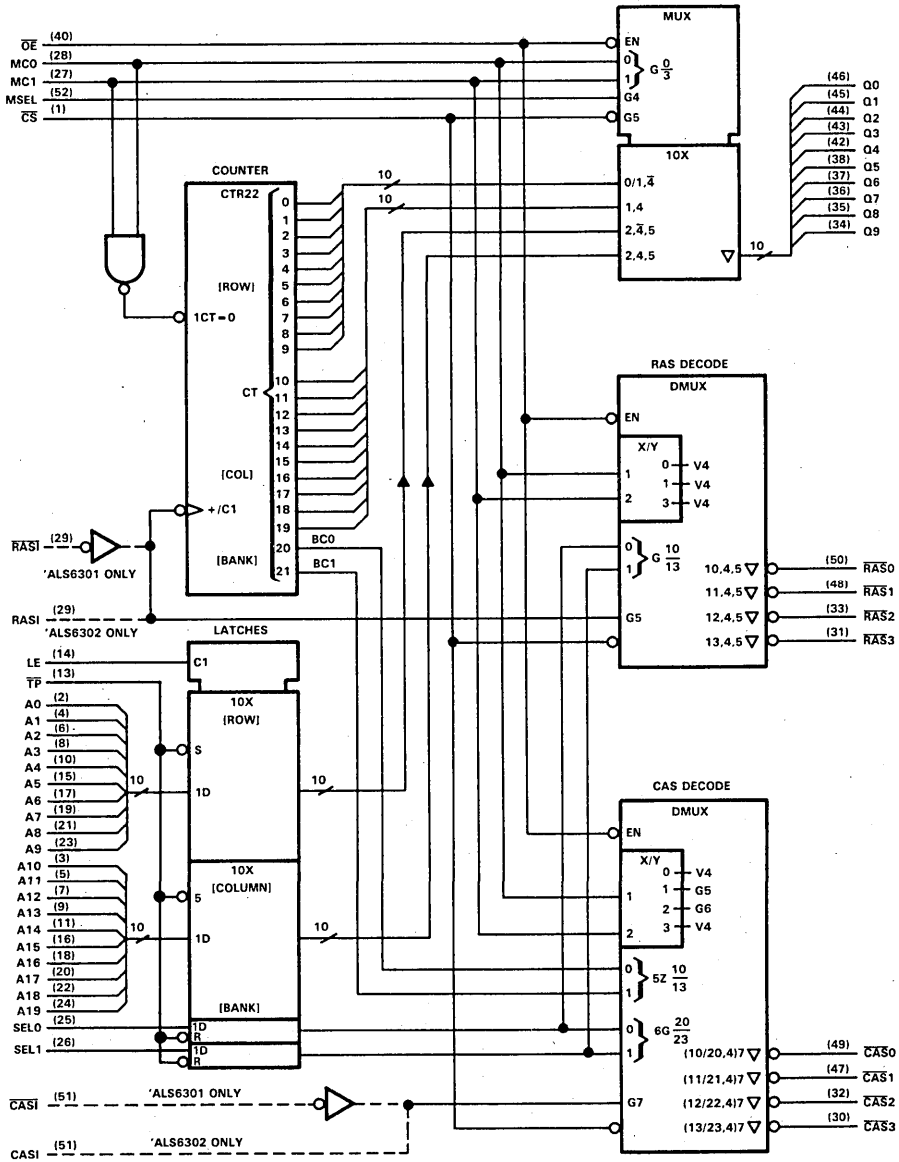
SN54ALS6301, SN54ALS6302 . . . JD PACKAGE
SN74ALS6301, SN74ALS6302 . . . JD OR N PACKAGE
(TOP VIEW)



† 'ALS6301 has active-low inputs $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$; 'ALS6302 has active-high inputs CASI and RASI.

SN54ALS6301, SN74ALS6301, SN54ALS6302, SN74ALS6302
DYNAMIC MEMORY CONTROLLERS

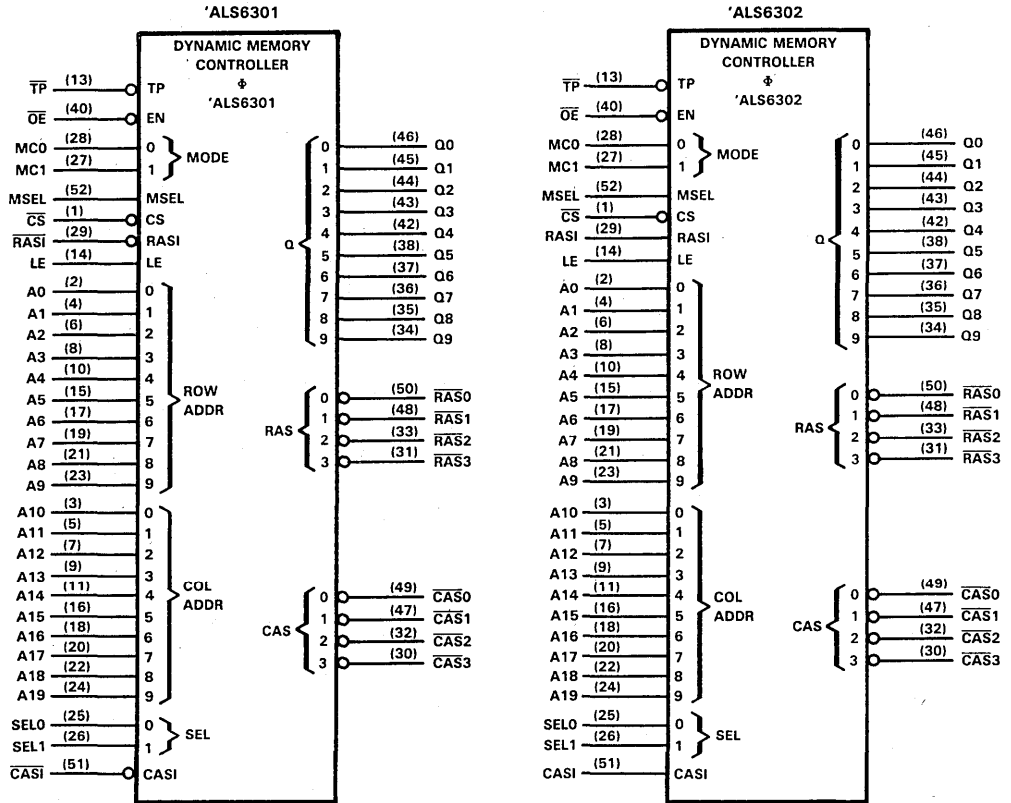
logic diagram (positive logic)



2
LSI Devices

SN54ALS6301, SN74ALS6301, SN54ALS6302, SN74ALS6302 DYNAMIC MEMORY CONTROLLERS

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std-91-1984 and IEC Publication 617-12.

2
LSI Devices

SN54ALS6301, SN74ALS6301, SN54ALS6302, SN74ALS6302
DYNAMIC MEMORY CONTROLLERS

TABLE 1. PIN FUNCTION

PIN NAME	DESCRIPTION
A0-A19	Address Inputs. A0-A9 are latched in as the nine-bit row address for the DRAM. These inputs drive Q0-Q9 when the DMC is in the read/write mode and MSEL is low. A10-A19 are latched in as the column address, and will drive Q0-Q8 when MSEL is high and the DMC is in the read/write mode. The addresses are latched when the Latch Enable (LE) input signal is low.
SELO, SEL1	Bank Select. These two inputs are normally the two highest-order address bits and are used in the read/write mode to select which bank of memory will be receiving the RAS and CAS signals after RAS \bar{I} ('ALS6301) or RASI ('ALS6302) and $\bar{C}AS\bar{I}$ ('ALS6301) or CASI ('ALS6302) go active.
LE	Latch Enable. This active-high input causes the row, column, and bank select latches to become transparent, allowing the latches to accept new input data. A low input on LE latches the input data.
MSEL	Multiplexer Select. This input determines whether the row or column address will be sent to the memory address inputs. When MSEL is high, the column address is selected, while the row address is selected when MSEL is low. The address may come from either the address latch or refresh address counter depending on MCO and MC1 (see Mode Control Function Table).
$\bar{C}S$	Chip Select. This active-low input is used to enable the DMC. When $\bar{C}S$ is active, the DMC operates normally in all four modes. When $\bar{C}S$ goes high, the device will not enter the read/write mode. This allows other devices to access the same memory that the DMC is controlling.
$\bar{O}E$	Output Enable. This active-low input enables/disables the output signals. When $\bar{O}E$ is high, the outputs of the DMC enter the high-impedance state.
MCO-MC1	Mode Controls. These inputs determine in which of the four modes the DMC operates. The description of each of the four operating modes is given in Table 2.
Q0-Q8	Address Outputs. These address outputs feed the DRAM address inputs and provide drive for memory systems having capacitance of up to 500 picofarads.
RAS \bar{I} or RASI	Row Address Strobe Input. During the normal memory cycles, the decoded RASn output (RAS0, RAS1, RAS2, or RAS3) is forced low after receipt of an active Row Address Strobe Input signal. In either Refresh mode, all four RAS outputs will be low while the Row Address Strobe Input signal is active. The RAS \bar{I} on the 'ALS6301 is an active-low input while on the 'ALS6302, RASI is an active-high input. (For more details see timing diagrams.)
RAS0-RAS3	Row Address Strobe. Each of the Row Address Strobe outputs provides a RAS signal to one of the four banks of dynamic memory. Each RASn output will go low when selected by SELO and SEL1 after RAS \bar{I} ('ALS6301) or RASI ('ALS6302) goes active. All four go low in response to RAS \bar{I} ('ALS6301) or RASI ('ALS6302) while in the refresh mode.
$\bar{C}AS\bar{I}$ or CASI	Column Address Strobe Input. This input going active causes the selected $\bar{C}AS$ output to be forced low. The $\bar{C}AS\bar{I}$ input on the 'ALS6301 is active low input while on the 'ALS6302, CASI is active high input. (For more details see timing diagrams.)
CAS0-CAS3	Column Address Strobe. During normal Read/Write cycles the two selected bits (SELO, SEL1) determine which $\bar{C}AS$ output will go active following $\bar{C}AS\bar{I}$ ('ALS6301) or CASI ('ALS6302) going active. When memory scrubbing is being performed, only the $\bar{C}ASn$ signal selected will be active. For non-scrubbing cycles, all four $\bar{C}AS$ outputs will remain high.
TP	This active-low test input asynchronously sets the row and column input latches high, while forcing the two bank select latches low. In normal operation, TP is tied high.

**SN54ALS6301, SN74ALS6301, SN54ALS6302, SN74ALS6302
DYNAMIC MEMORY CONTROLLERS**

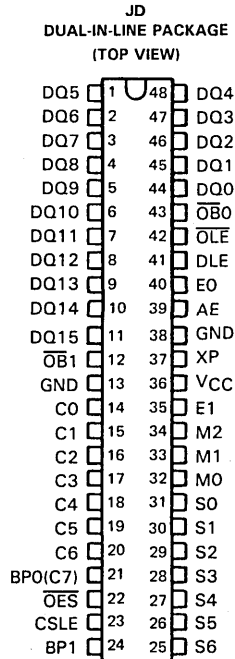
TABLE 2. MODE-CONTROL FUNCTION TABLE

MC1	MC0	OPERATING MODE
L	L	Refresh Mode without Scrubbing. Refresh cycles are performed with only the row counter being used to generate the addresses. In this mode, all four \overline{RAS} outputs are active while the four \overline{CAS} outputs remain high.
L	H	Refresh with Scrubbing/Initialize. During this mode, refresh cycles are done with both the row and column counters generating the addresses. MSEL is used to select either the row or the column counter. All four \overline{RAS} outputs go low in response to \overline{RASi} ('ALS6301) or $RASi$ ('ALS6302), while only one \overline{CASn} output goes low in response to \overline{CASi} ('ALS6301) or $CASi$ ('ALS6302). The bank counter keeps track of which \overline{CAS} output goes active. This mode can also be used during system power-up so that the memory can be written with a known data pattern.
H	L	Read/Write. This mode is used to perform read/write cycles. Both the Row and Column addresses are multiplexed to the address output lines using MSEL. SEL0 and SEL1 are decoded to determine which \overline{RASn} and \overline{CASn} outputs will be active.
H	H	Clear Refresh Counters. This mode clears the three refresh counters (row, column, and bank) on the inactive transition of \overline{RASi} ('ALS6301) or $RASi$ ('ALS6302), putting them at start of the refresh sequence (see timing diagrams for more detail). In this mode, all four \overline{RAS} outputs are driven low after the active edge of \overline{RASi} ('ALS6301) or $RASi$ ('ALS6302) so that DRAM wake-up cycles may also be performed.

2

LSI Devices

- Direct Replacement for National Semiconductor DP8400
- Fast Single- and Double-Error Detection
- Fast Single-Error Correction and Functionally Expandable to 100% Double-Error Correction Capability
- Double-Error Correction after Catastrophic Failure without Additional Check Bits or ICs
- Functionally Expandable Capability Up to Triple-Error Detection
- Expandable to and beyond 64 Bits with Additional 'ALS8400s
- Complete Error Recording
- Byte Parity Generating and Checking
- Separate Byte Controls for Data Output in Byte-Write Operation
- Syndrome I/O Port for Error Logging and Management
- Full Memory Check Diagnostic and Check Bits Simulation Diagnostics Capability
- Self-Test of 'ALS8400 on the Memory Card Under Processor Control
- Complete Memory Failure Detection
- Power-On Clears Data and Syndrome Latches



description

The 'ALS8400 is a monolithic Advanced Low-Power Schottky error checker and corrector (ECC) integrated circuit designed to aid in system reliability and integrity by detecting errors in memory data and correcting single- or double-bit errors. The ECC has a separate syndrome I/O bus, which can be used for error logging or error management. It can also be used in BYTE-WRITE applications (for up to 72 data bits) because it has separate byte controls for the data buffers. In 16- or 32-bit systems, the 'ALS8400 will generate and check system byte parity, if required, for integrity of the data supplied from or to the processor. There are three latch controls to enable latching of data in various modes and configurations.

The 'ALS8400 is easily expandable to other data configurations. For 32-bit data bus with seven check bits, two 'ALS8400s can be used in cascade with no other ICs. Three 'ALS8400s can be used for 48 bits, and four 'ALS8400s for 64 data bits, both using eight check bits. In all these configurations, single-error and double-error detection and single-error correction are easy to implement.

The 'ALS8400 is characterized for operation from °C to 70°C.

SN74ALS8400

EXPANDABLE ERROR CHECKER AND CORRECTOR

2

LSI Devices

PIN NAMES	I/O	DESCRIPTION
AE	O	Any error output. In the normal read mode, when low, AE indicates no error and when high, indicates that an error has occurred. In any write mode, AE is permanently low.
BPO/C7	I/O	Byte parity 0/check bit 7. When XP is at 0 V, this pin is byte-0 parity I/O. In the normal write mode, BPO receives system byte-0 parity, and in the normal read mode, outputs system byte-0 parity. When the XP pin is open or at V _{CC} , the BPO/C7 pin becomes the check bit C7 I/O, the eighth check bit for the memory check bits, for 48-bit expansion configuration and beyond.
BP1/S7	I/O	Byte parity 1/syndrome bit 7. When XP pin is at 0 V, this pin is byte 1 parity I/O. In the normal write mode, BP1 receives system byte-1 parity, and in the normal read mode outputs system byte-1 parity. When the XP pin is open or at V _{CC} , the BP1/S7 pin becomes the syndrome bit S7 I/O, the eighth syndrome bit, for 48-bit expansion configuration and beyond.
CSLE	I	Input check bit and syndrome latch enable. When high, the outputs of the check bit input latches follow input check bit and, if \overline{OES} is low, the outputs of the syndrome input latches follow the syndrome bit bus.
CO-C6	I/O	Check-bit I/O port. A 7-bit bidirectional bus connected to the input of the check-bit input latches and the outputs of the check-bit output buffers. The check-bit output buffers are enabled whenever M2 pin is low.
DLE	I	Input data latch enable. When high, outputs of the data input latches follow the input data bus. When low, the data input latches store the input data.
DQ0-DQ15	I/O	Data I/O port. A 16-bit bidirectional data bus connected to the input of the data input latches and the outputs of the data output buffers, with DQ8-DQ15 also connected to the check-bit input latches.
E0	O	Error 0 output. In the normal read mode, E0 is high for a single-data error and low for other conditions. In the normal write mode, E0 becomes PE0 and is low if a parity error exists in byte-0 as transmitted from the processor.
E1	O	Error 1 output. In the normal read mode, E1 is high for a single-data error or a single check-bit error, and low for no error or a double error. In the normal write mode, E1 becomes PE1 and is low if a parity error exists in byte 1 as transmitted from the processor.
GND		System ground
M0-M2	I	Mode control inputs. These three controls define the eight major operational modes of the ECC. Table 1 describes the modes.
$\overline{OB0}, \overline{OB1}$	I	Output byte 0 and Output byte 1 enables. These inputs, when low, enable the outputs of the data output latches through the data output buffers onto the data bus. When $\overline{OB0}$ and $\overline{OB1}$ are high, the outputs of the data output buffers are placed in the high-impedance state.
\overline{OES}	I	Output enable syndromes. I/O control of the syndrome latches. When high, the outputs of the syndrome output buffers are placed in the high-impedance state and external syndromes pass through the syndrome input latches with CSLE high. When \overline{OES} is low, the outputs of the syndrome output buffers are enabled and the generated syndromes appear on the syndrome bus, also CSLE is inhibited internally to the syndrome input latches.
\overline{OLE}	I	Output latch enable. When low, \overline{OLE} enables the internally generated data to enter the data output latches, check bit output latches, and syndrome output latches. When \overline{OLE} is high, the latches store the data.
S0-S6	I/O	Syndrome I/O port. A 7-bit bidirectional bus connected to the input of the syndrome input latches and the outputs of the syndrome output buffers.
V _{CC}	I	5-volt supply voltage input.
XP	I	Multiexpansion input to a three-level comparator. With XP at 0 V, only 6 or 7 check bits are available for expansion up to 40 bits, allowing byte parity capability. With XP open or at V _{CC} , expansion beyond 40 bits is possible, but byte-parity capability is no longer available. When XP is at V _{CC} , check-bit generator bits 6 and 7, the internally generated upper two check bits, are set low. When XP is open, check-bit generator bits 6 and 7 are set to word parity.

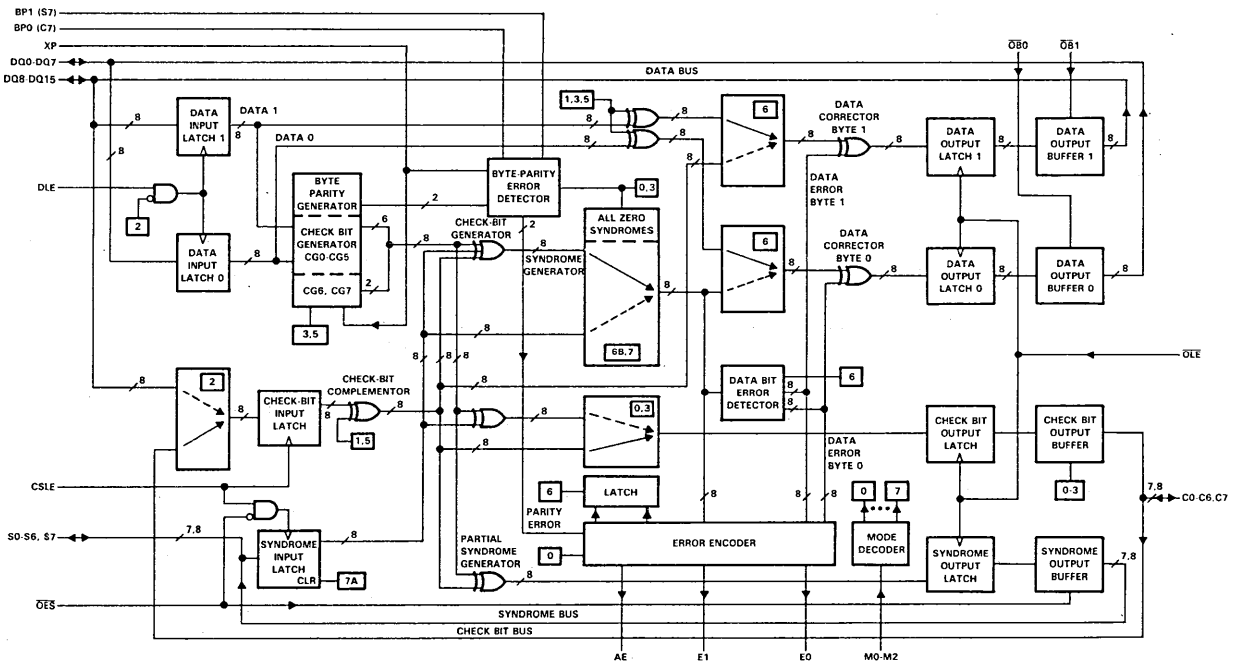
functional description

The 'ALS8400, with its 16-bit bidirectional data bus connected to the memory data bus, monitors data between the processor and memory. It uses an encoding matrix to generate six check bits from the 16 bits of data. In a write cycle, the data word and the corresponding check bits are written into memory. When the same location of memory is subsequently read, the ECC generates six new check bits from the memory data and compares them with the six check bits read from memory to create six syndrome bits. If there is a difference (causing some syndrome bits to go high), then that memory location contains an error and the ECC indicates the type of error with three error flags. If the error is a single-bit error, the ECC will automatically correct it.

When the memory has more than one error, or better system integrity is preferred, double-error correction can be performed. One approach requires a further write-read cycle using complemented data and check bits from the ECC. If at least one of the two errors is a hard error, the ECC will correct both errors. This implementation requires no more memory check bits or ECCs than the single-error correct configuration.

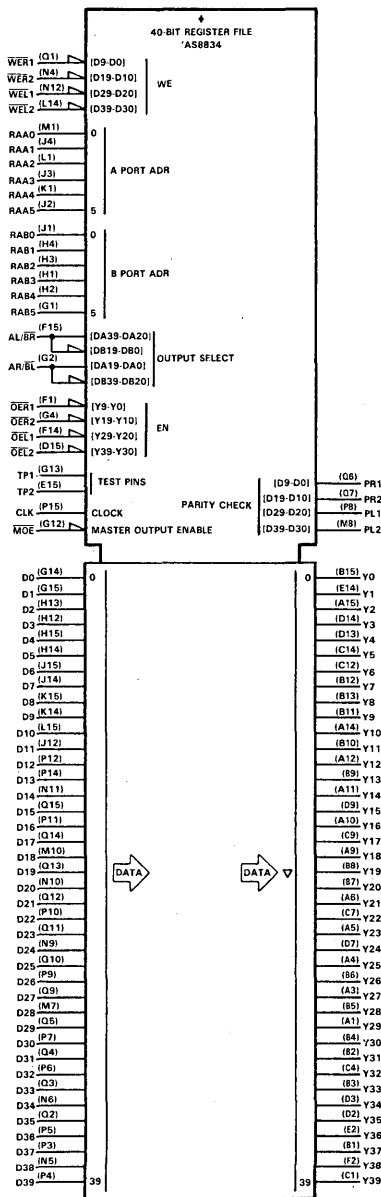
SN74ALS8400
EXPANDABLE ERROR CHECKER AND CORRECTOR

functional block diagram (positive logic)



- Advanced Schottky IMPACT-X™ Process
- Three-Operand, 64-Word by 40-Bit Register File
- Supports 'AS888 and 'AS8832 Register File Expansion
- Four 10-Bit Input Ports with Individual Parity Checkers and Write Enables
- Four 10-Bit Output Ports with Individual Three-State Enables
- Two Write Address Ports
- Two Read Address Ports and Y Output Mux Permit LSH/MSH Swap Operations
- 156-Pin Package
- 8-mA Bus Drivers
- Texas Instruments Quality and Reliability

logic symbol†



description

The SN54AS8834 and SN74AS8834 are high speed, three-operand, 64-word register files in a 156-pin ceramic pin grid array.

The register files are designed to support register file expansion for bit-slice systems using the 'AS888 or 'AS8832. Internal parity checks and a 40-bit word width support I/O operations for graphics and 32-bit error detection and correction boards.

The SN54AS8834 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74AS8834 is characterized for operation from 0°C to 70°C.

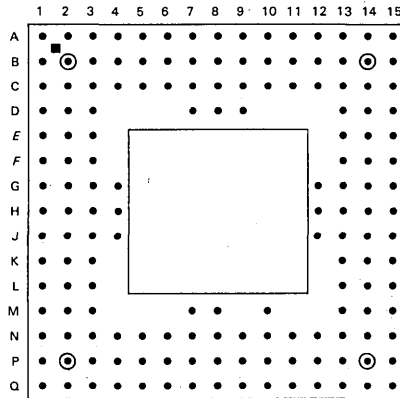


IMPACT-X is a trademark of Texas Instruments

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

SN54AS8834, SN74AS8834
40-BIT REGISTER FILE

SN54AS8834, SN74AS8834
GB PIN-GRID-ARRAY PACKAGE
(TOP VIEW)



2

LSI Devices

PIN		PIN		PIN		PIN		PIN		PIN	
NO.	NAME	NO.	NAME	NO.	NAME	NO.	NAME	NO.	NAME	NO.	NAME
A1	Y29	B12	Y7	D14	Y3	H12	D3	M3	WAR3	P5	D36
A2	NC	B13	Y8	D15	$\overline{OEL2}$	H13	D2	M7	D28	P6	D32
A3	Y27	B14	NC	E1	NC	H14	D5	M8	PL2	P7	D30
A4	Y25	B15	Y0	E2	Y36	H15	D4	M10	D18	P8	PL1
A5	Y23	C1	Y39	E3	GND1	J1	RAB0	M13	WAL3	P9	D26
A6	Y21	C2	NC	E13	GND1	J2	RAA5	M14	WAL2	P10	D22
A7	NC	C3	NC	E14	Y1	J3	RAA3	M15	NC	P11	D16
A8	NC	C4	Y32	E15	TP2	J4	RAA1	N1	NC	P12	D12
A9	Y18	C5	VCC1	F1	$\overline{OER1}$	J12	D11	N2	WAR4	P13	WAR5
A10	Y16	C6	GND1	F2	Y38	J13	GND2	N3	WAR5	P14	D13
A11	Y14	C7	Y22	F3	GND2	J14	D7	N4	$\overline{WER2}$	P15	CLK
A12	Y12	C8	GND1	F13	GND2	J15	D6	N5	D38	Q1	$\overline{WER1}$
A13	NC	C9	Y17	F14	$\overline{OEL1}$	K1	RAA4	N6	D34	Q2	D35
A14	Y10	C10	GND1	F15	AL/ \overline{BR}	K2	GND2	N7	VCC1	Q3	D33
A15	Y2	C11	VCC1	G1	RAB5	K3	GND2	N8	GND1	Q4	D31
B1	Y37	C12	Y6	G2	AR/ \overline{BL}	K13	VCC2	N9	D24	Q5	D29
B2	Y31	C13	NC	G3	VCC2	K14	D9	N10	D20	Q6	PR1
B3	Y33	C14	Y5	G4	$\overline{OEB2}$	K15	D8	N11	D14	Q7	PR2
B4	Y30	C15	NC	G12	\overline{MOE}	L1	RAA2	N12	$\overline{WEL1}$	Q8	NC
B5	Y28	D1	NC	G13	TP1	L2	WAR0	N13	WAL4	Q9	D27
B6	Y26	D2	Y35	G14	D0	L3	VCC2	N14	WAL0	Q10	D25
B7	Y20	D3	Y34	G15	D1	L13	WAL1	N15	NC	Q11	D23
B8	Y19	D7	Y24	H1	RAB3	L14	$\overline{WEL2}$	P1	NC	Q12	D21
B9	Y13	D8	VCC1	H2	RAB4	L15	D10	P2	WAR1	Q13	D19
B10	Y11	D9	Y15	H3	RAB2	M1	RAA0	P3	D37	Q14	D17
B11	Y9	D13	Y4	H4	RAB1	M2	WAR2	P4	D39	Q15	D15

NC—No internal connection

SN54AS8834, SN74AS8834
40-BIT REGISTER FILE

PIN		I/O	DESCRIPTION
NAME	NO.		
AL/BR	F15	I	Output select for Y20-Y39 output data. High selects DA20-DA39; low selects DB0-DB19.
AR/BL	G2	I	Output select for Y0-Y10 output data. High selects DA0-DA19; low selects DA20-DA39.
CLK	P15	I	Clocks data into register file on rising edge.
D0	G14	I	Input data bits 0 through 9
D1	G15		
D2	H13		
D3	H12		
D4	H15		
D5	H14		
D6	J15		
D7	J14		
D8	K15		
D9	K14		
D10	L15	I	Input data bits 10 through 19
D11	J12		
D12	P12		
D13	P14		
D14	N11		
D15	Q15		
D16	P11		
D17	Q14		
D18	M10		
D19	Q13		
D20	N10	I	Input data bits 20 through 29
D21	Q12		
D22	P10		
D23	Q11		
D24	N9		
D25	Q10		
D26	P9		
D27	Q9		
D28	M7		
D29	Q5		
D30	P7	I	Input data bits 30 through 39
D31	Q4		
D32	P6		
D33	Q3		
D34	N6		
D35	Q2		
D36	P5		
D37	P3		
D38	N5		
D39	P4		
GND1	E3		5-volt ground (All ground pins must be used.)
GND1	E13		
GND1	C6		
GND1	C8		
GND1	C10		
GND1	N8		

2

LSI Devices

SN54AS8834, SN74AS8834
40-BIT REGISTER FILE

2

LSI Devices

PIN		I/O	DESCRIPTION
NAME	NO.		
GND2	F3		2-volt ground (All ground pins must be used.)
GND2	F13		
GND2	J13		
GND2	K2		
GND2	D3		
M8	PL2	O	Parity check result. High indicates odd number of high inputs on D30-D39.
MOE	G12	I	Master output enable, active low. Places Y0-Y39 and parity outputs in the high-impedance state when high.
NC	A2		No internal connection
NC	A7		
NC	A8		
NC	A13		
NC	B14		
NC	C2		
NC	C3		
NC	C13		
NC	C15		
NC	D1		
NC	E1		
NC	M15		
NC	N1		
NC	N15		
NC	P1		
NC	Q8		
$\overline{OEL1}$	F14	I	Y20-Y29 output enable, active low
$\overline{OEL2}$	D15		Y30-Y39 output enable, active low
$\overline{OER1}$	F1		Y0-Y9 output enable, active low
$\overline{OER2}$	G4		Y10-Y19 output enable, active low
PL1	P8	O	Parity check result. High indicates odd number of high inputs on D20-D29.
PL2	M8		Parity check result. High indicates odd number of high inputs on D30-D39.
PR1	Q6		Parity check result. High indicates odd number of high inputs on D0-D9.
PR2	Q7		Parity check result. High indicates odd number of high inputs on D10-D19.
RAA0	M1	I	Register file A port read address select (O = LSB)
RAA1	J4		
RAA2	L1		
RAA3	J3		
RAA4	K1		
RAA5	J2		
RAB0	J1	I	Register file A port read address select (O = LSB)
RAB1	H4		
RAB2	H3		
RAB3	H1		
RAB4	H2		
RAB5	G1		
TP1	G13	I	Functional testing input. During normal operation, should be maintained high or open.
TP2	E15		

SN54AS8834, SN74AS8834
40-BIT REGISTER FILE

PIN		I/O	DESCRIPTION
NAME	NO.		
VCC1	C5		5-volt supply for TTL-compatible I/O
VCC1	C11		
VCC1	D8		
VCC1	N7		
VCC2	G3		2-volt supply for internal Schottky transistor logic
VCC2	K13		
VCC2	L3		
WAL0	N14	I	Write address for D20-D39 input data
WAL1	L13		
WAL2	M14		
WAL3	M13		
WAL4	N13		
WAL5	P13		
WAR0	L2	I	Write address for D0-D19 input data
WAR1	P2		
WAR2	M2		
WAR3	M3		
WAR4	N2		
WAR5	N3		
WER1	N12	I	D20-D29 write enable, active low
WER2	L14		D30-D39 write enable, active low
WER1	Q1		D0-D9 write enable, active low
WER2	N4		D10-D19 write enable, active low
Y0	B15	O	Output data bits 0 through 9
Y1	E14		
Y2	A15		
Y3	D14		
Y4	D13		
Y5	C14		
Y6	C12		
Y7	B12		
Y8	B13		
Y9	B11		
Y10	A14	O	Output data bits 10 through 19
Y11	B10		
Y12	A12		
Y13	B9		
Y14	A11		
Y15	D9		
Y16	A10		
Y17	C9		
Y18	A9		
Y19	B8		

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LSI Devices

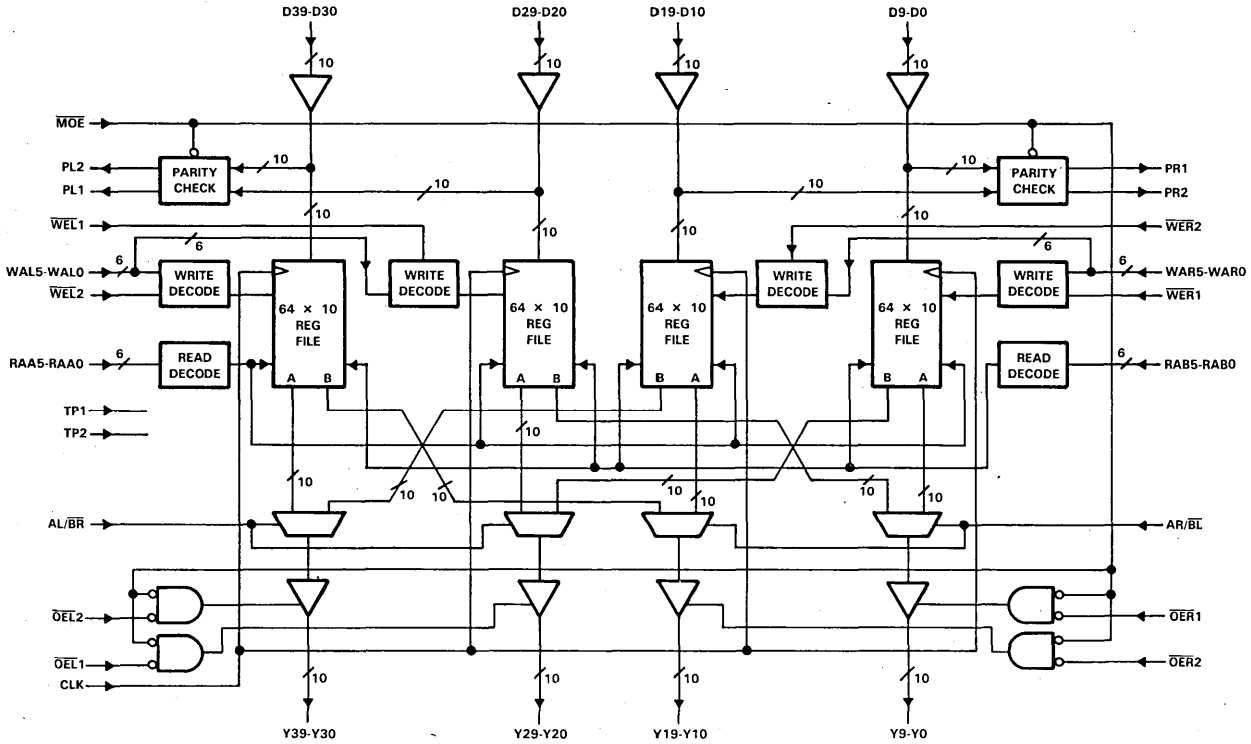


SN54AS8834, SN74AS8834
40-BIT REGISTER FILE

PIN		I/O	DESCRIPTION
NAME	NO.		
Y20	B7	O	Output data bits 20 through 29
Y21	A6		
Y22	C7		
Y23	A5		
Y24	D7		
Y25	A4		
Y26	B6		
Y27	A3		
Y28	B5		
Y29	A1		
Y30	B4	O	Output data bits 30 through 39
Y31	B2		
Y32	C4		
Y33	B3		
Y34	D3		
Y35	D2		
Y36	E2		
Y37	B1		
Y38	F2		
Y39	C1		

2

LSI Devices



ALS8834 REGISTER FILE

SN54AS8834, SN74AS8834
40-BIT REGISTER FILE

SN54AS8834, SN74AS8834 40-BIT REGISTER FILE

data input/output ports

Data is input to the 'AS8834 through four 10-bit data ports: D30-D39, D20-D29, D10-D19 and D0-D9. Data is output from the register file through four 10-bit output ports: Y30-Y39, Y20-Y29, Y10-Y19 and Y0-Y9. The Y ports are enabled by four active low output enables: $\overline{OEL2}$ for Y30-Y39, $\overline{OEL1}$ for Y20-Y29, $\overline{OER2}$ for Y10-Y19, and $\overline{OER1}$ for Y0-Y9.

register file addressing

Data is stored in the register file on the rising edge of the clock. Two write address ports and two read address ports operate independently to implement a 40-bit register file that supports MSH/LSH swap operations. WAL0-WAL5 is the write address for D20-D39 input data; WAR0-WAR5 is the write address for D0-D19 input data. These separate write addresses permit the most significant and the least significant half of a word to be stored at different addresses. Register file writes are enabled by four write enables: $\overline{WEL2}$ for D30-D39, $\overline{WEL1}$ for D20-D29, $\overline{WER2}$ for D10-D19, and $\overline{WER1}$ for D0-D9.

Two read address lines are also provided: RAA0-RAA5 and RAB0-RAB5. These lines control the selection of data to be output on internal data buses DA0-DA39 and DB0-DB39 respectively. Y-output data selection is controlled by $\overline{AL/BR}$ and $\overline{AR/BL}$ as shown in Table 1.

TABLE 1. OUTPUT FUNCTION TABLE

SIGNAL $\overline{AL/BR}$	RESULT Y20-Y39	SIGNAL $\overline{AR/BL}$	RESULT Y0-Y19	RESULT WHEN COMBINED	
				Y20-Y39	Y0-Y19
H	A20-A39	H	A0-A19	A (MSH)	A (LSH)
H	A20-A39	L	B20-B39	A (MSH)	B (MSH)
L	B0-B19	H	A0-A19	B (LSH)	A (LSH)
L	B0-B19	L	B20-B39	B (LSH)	B (MSH)

parity checkers

Two parity checkers are provided for data on the D input ports. A high on output signals PL2, PL1, PR2 or PR1 indicate an odd number of high signals on data inputs D30-D39, D20-D29, D10-D19 and D0-D9 respectively.

master output enable

When high, Master Output Enable, \overline{MOE} , places the four Y output ports and the four parity output ports in the high-impedance state.

SN54AS8834, SN74AS8834 40-BIT REGISTER FILE

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage, V_{CC1}	7 V
Supply voltage, V_{CC2}	3 V
Input voltage	7 V
High-level voltage applied to 3-state outputs	5.5 V
Operating case temperature range: SN54AS8834	-55°C to 125°C
Operating free-air temperature range: SN74AS8834	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

PARAMETER	SN54AS8834			SN74AS8834			UNIT	
	MIN	NOM	MAX	MIN	NOM	MAX		
V_{CC1} I/O supply voltage	4.5	5	5.5	4.5	5	5.5	V	
V_{CC2} STL internal logic supply voltage	1.9	2	2.1	1.9	2	2.1	V	
V_{IH} High-level input voltage	2			2			V	
V_{IL} Low-level input voltage	0.8			0.8			V	
I_{OH} High-level output current	-1			2.6			mA	
I_{OL} Low-level output current	8			8			mA	
T_C Operating case temperature	125						°C	
T_A Operating free-air temperature	-55			0			70	°C

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS8834			SN74AS8834			UNIT
		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
V_{IK}	$V_{CC1} = 4.5$ V, $I_I = -18$ mA	-1.2			-1.2			V
V_{OH}	$V_{CC1} = 4.5$ V, $I_{OH} = -1$ mA	2.4						V
	$V_{CC1} = 4.5$ V, $I_{OH} = -2.6$ mA				2.4			V
V_{OL}	$V_{CC1} = 4.5$ V, $I_{OL} = 8$ mA	0.5			0.5			V
I_{OZH}	$V_{CC1} = 5.5$ V, $V_O = 2.7$ V				20			μA
I_{OZL}	$V_{CC1} = 5.5$ V, $V_O = 0.4$ V				-0.4			mA
I_I	$V_{CC1} = 5.5$ V, $V_I = 7$ V	0.1			0.1			mA
I_{IH}	$V_{CC1} = 5.5$ V, $V_I = 2.7$ V	20			20			μA
I_{IL}	$V_{CC1} = 5.5$ V, $V_I = 0.5$ V	-0.4			-0.4			mA
I_O^{\ddagger}	$V_{CC1} = 5.5$ V, $V_O = 2.25$ V	-30			-112			mA
I_{CC1}	$V_{CC1} = 5.5$ V							mA
I_{CC2}	$V_{CC2} = 2.1$ V							mA

[†] All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

[‡] The output conditions have been chosen to produce a current that closely approximates one-half the true short-circuit current, I_{OS} .

2
LSI Devices

SN54AS8834, SN74AS8834
40-BIT REGISTER FILE

timing requirements

PARAMETER		SN54AS8834		SN74AS8834		UNIT
		MIN	MAX	MIN	MAX	
t _{su}	Setup time	WEL1-WEL2 before CLK†				ns
		WER1-WER2 before CLK†				
		WAL0-WAL5 before CLK†				
		WAR0-WAR5 before CLK†				
		D0-D39 before CLK†				
t _h	Hold time	WEL1-WEL2 after CLK†				ns
		WER1-WER2 after CLK†				
		WAL0-WAL5 after CLK†				
		WAR0-WAR5 after CLK†				
		D0-D39 after CLK†				

switching characteristics over recommended ranges of operating temperature and supply voltage (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54AS8834		SN74AS8834		UNIT
			MIN	MAX	MIN	MAX	
t _{pd}	D30-D39	PL2					ns
	D20-D29	PL1					
	D10-D19	PR2					
	D0-D9	PR1					
	RAA0-RAA5	Y0-Y39					
	RAB0-RAB5	Y0-Y39					
	AL/BR	Y20-Y39					
	AR/BL	Y0-Y19					
	CLK	Y0-Y39†					
t _{en}	MOE	PL2-PL1 or PR2-PR1					ns
	MOE	Y0-Y39					
	OEL2	Y30-Y39					
	OEL1	Y20-Y29					
	OER2	Y10-Y19					
	OER1	Y0-Y9					
t _{dis}	MOE	PL2-PL1 or PR2-PR1					ns
	MOE	Y0-Y39					
	OEL2	Y30-Y39					
	OEL1	Y20-Y29					
	OER2	Y10-Y19					
	OER1	Y0-Y9					

†When read and write address are already selected.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

2 LSI Devices

SN54AS8838, SN74AS8838 32-BIT BARREL SHIFTERS

D2938, NOVEMBER 1985—REVISED MARCH 1986

- High-Speed "Flash" Shift Operations
- Shifts up to 32 Positions in Less than 25 ns
- Performs Logical, Circular, and Arithmetic Shifts
- 3-State Outputs Allow 32-Bit and 16-Bit Bus Interface
- 24-mA Bus Drivers
- 84-Pin Package
- Uses Less than 1.5 W (Max)
- Texas Instruments Quality and Reliability

description

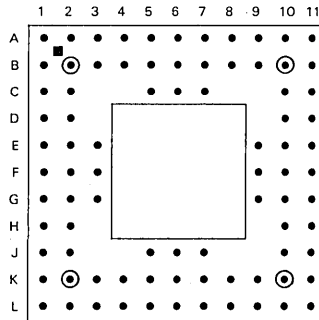
The SN54AS8838 and SN74AS8838 are high-speed 32-bit barrel shifters in an 84-pin ceramic pin-grid array. The devices can shift up to 32 bits in a single instruction cycle of under 25 nanoseconds. Five basic shifts can be programmed: circular left and right, logical left and right, and arithmetic right.

Unlike conventional shift registers, whose shift operations are controlled by the number of input clock pulses applied, the number of positions to be shifted by the 'AS8838 is determined by an input decoder. This form of implementation does not require an input clock, thus, the shift operation is restricted only by internal propagation delays. The delay is the same regardless of the number of positions to be shifted, resulting in a high-speed "flash" shift.

Three-state output controls allow the devices to be interfaced with 32- or 16-bit data buses.

The SN54AS8838 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74AS8838 is characterized for operation from 0°C to 70°C.

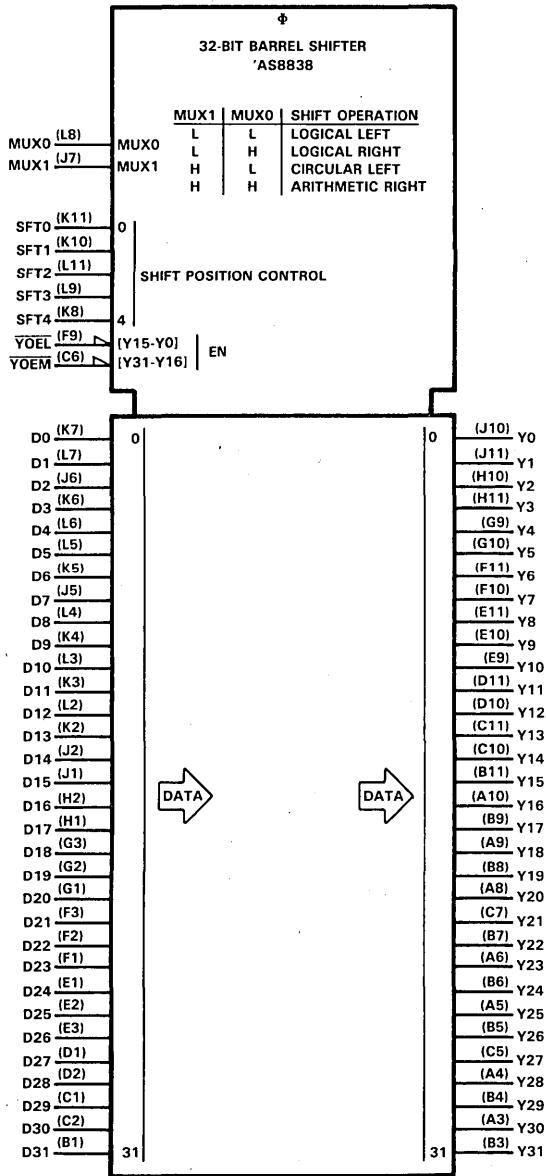
SN54AS8838, SN74AS8838
GB PIN-GRID-ARRAY PACKAGE
(TOP VIEW)



PIN		PIN	
NO.	NAME	NO.	NAME
A1	GND	F9	Y0EL
A2	VCC2	F10	Y7
A3	Y30	F11	Y6
A4	Y28	G1	D20
A5	Y25	G2	D19
A6	Y23	G3	D18
A7	GND	G9	Y4
A8	Y20	G10	Y5
A9	Y18	G11	GND
A10	Y16	H1	D17
A11	GND	H2	D16
B1	D31	H10	Y2
B2	GND	H11	Y3
B3	Y31	J1	D15
B4	Y29	J2	D14
B5	Y26	J5	D7
B6	Y24	J6	D2
B7	Y22	J7	MUX1
B8	Y19	J10	Y0
B9	Y17	J11	Y1
B10	VCC1	K1	VCC1
B11	Y15	K2	D13
C1	D29	K3	D11
C2	D30	K4	D9
C5	Y27	K5	D6
C6	Y0EM	K6	D3
C7	Y21	K7	D0
C10	Y14	K8	SFT4
C11	Y13	K9	GND
D1	D27	K10	SFT1
D2	D28	K11	SFT0
D10	Y12	L1	GND
D11	Y11	L2	D12
E1	D24	L3	D10
E2	D25	L4	D8
E3	D26	L5	D5
E9	Y10	L6	D4
E10	Y9	L7	D1
E11	Y8	L8	MUX0
F1	D23	L9	SFT3
F2	D22	L10	VCC2
F3	D21	L11	SFT2

SN54AS8838, SN74AS8838
32-BIT BARREL SHIFTERS

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

SN54AS8838, SN74AS8838
32-BIT BARREL SHIFTERS

PIN		I/O	DESCRIPTION
NAME	NO.		
D0	K7	I	Input data bits 0 through 31
D1	L7		
D2	J6		
D3	K6		
D4	L6		
D5	L5		
D6	K5		
D7	J5		
D8	L4		
D9	K4		
D10	L3		
D11	K3		
D12	L2		
D13	K2		
D14	J2		
D15	J1		
D16	H2		
D17	H1		
D18	G3		
D19	G2		
D20	G1		
D21	F3		
D22	F2		
D23	F1		
D24	E1		
D25	E2		
D26	E3		
D27	D1		
D28	D2		
D29	C1		
D30	C2		
D31	B1		
GND	A1		Ground (All ground pins must be used.)
GND	A7		
GND	A11		
GND	B2		
GND	G11		
GND	K9		
GND	L1		
MUX0	L8	I	Shift instruction control. Specifies the type of shift operation to be performed. See Table 1 for further information.
MUX1	J7		
SFT0	K11	I	Shift position control. Specifies the number of bit positions to shift. See Table 1 for further information.
SFT1	K10		
SFT2	L11		
SFT3	L9		
SFT4	K8		
VCC1	B10		5-Volt supply for TTL-compatible I/O
VCC1	K1		
VCC2	A2		2-Volt supply for internal Schottky Transistor Logic (STL)
VCC2	L10		

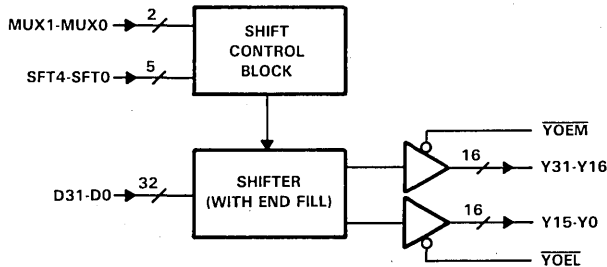
SN54AS8838, SN74AS8838
32-BIT BARREL SHIFTERS

2

LSI Devices

PIN		I/O	DESCRIPTION
NAME	NO.		
Y0	J10	O	Output data bits 0 through 10
Y1	J11		
Y2	H10		
Y3	H11		
Y4	G9		
Y5	G10		
Y6	F11		
Y7	F10		
Y8	E11		
Y9	E10		
Y10	E9		
Y11	D11	O	Output data bits 11 through 31
Y12	D10		
Y13	C11		
Y14	C10		
Y15	B11		
Y16	A10		
Y17	B9		
Y18	A9		
Y19	B8		
Y20	A8		
Y21	C7		
Y22	B7		
Y23	A6		
Y24	B6		
Y25	A5		
Y26	B5		
Y27	C5		
Y28	A4		
Y29	B4		
Y30	A3		
Y31	B3		
YOEL	F9	I	Control input for the Y15-Y0 output port. When YOEL is low, Y15-Y0 is enabled.
YOEM	C6	I	Control input for the Y31-Y16 output port. When YOEM is low, Y31-Y16 is enabled.

functional block diagram



data input/output

Data is input to the 'AS8838 through the D31-D0 data port and output through two 16-bit data ports, Y31-Y16 and Y15-Y0. Two 3-state output controls enable the Y data ports. The most significant half of the shift result is enabled when \overline{YOEM} is low, the least significant half when \overline{YOEL} is low.

shift control block

The shift control block decodes the MUX1-MUX0 instruction inputs and the SFT4-SFT0 shift position controls and transmits the resulting control signals to the shifter. MUX1-MUX0 control shift instruction selection as shown in Table 1. SFT4-SFT0 specify the number of bit positions to be shifted. For right shifts, the two's complement of the number of bit positions must be placed on SFT4-SFT0.

TABLE 1. INSTRUCTION SET

MUX1	MUX0	FUNCTION	OPERATION
L	L	Logical Left Shift	Shift left the number of bit positions defined by SFT4-SFT0. Fill vacated bit positions with zeros.
L	H	Logical Right Shift	Shift right the number of bit positions specified by the two's complement of SFT4-SFT0. Fill vacated bit positions with zeros. (A logical right shift with SFT4-SFT0 = 0 will fill all bits with zeros.)
H	L	Circular Left Shift	Circular left shift the number of bit positions defined by SFT4-SFT0. (A circular right shift can be performed by putting the two's complement of number of bits to be shifted on SFT4-SFT0.)
H	H	Arithmetic Right Shift	Shift right the number of bit positions defined by the two's complement of SFT4-SFT0. Fill vacated bit positions with the D31 input value (sign bit) (An arithmetic right shift with SFT4-SFT0 = 0 will fill all bits with the sign bit.)

2
LSI Devices

SN54AS8838, SN74AS8838 32-BIT BARREL SHIFTERS

shift operation examples

logical shift left (M1 – M0 = LL)

In the shift left mode, SFT4-SFT0 define the number of bit positions to be shifted. The following example shifts a 32-bit word 8 positions to the left and fills the vacated bit positions with zeros.

CONTROL SIGNALS

SHIFT INSTRUCTION M2-M0	NUMBER OF BITS TO SHIFT SFT4-SFT0
00	01000

Assume D31-D0 is hex ABCD0123.

D31-D0

Input Data 1010 1011 1100 1101 0000 0001 0010 0011

Y31-Y0

Result 1100 1101 0000 0001 0010 0011 0000 0000

logical shift right (M1 – M0 = LH)

In the shift right mode, the two's complement of the number of bit positions to be shifted must be placed on SFT4-SFT0. The following example shifts a 32-bit word 8 positions to the right and fills the vacated bit positions with zeros.

CONTROL SIGNALS

SHIFT INSTRUCTION M2-M0	NUMBER OF BITS TO SHIFT SFT4-SFT0
01	11000

Assume D31-D0 is hex ABCD0123.

D31-D0

Input Data 1010 1011 1100 1101 0000 0001 0010 0011

Y31-Y0

Result 0000 0000 1010 1011 1100 1101 0000 0001

2

LSI Devices

circular shift left (M1 – M0 = HL)

In the circular shift left mode, SFT4-SFT0 define the number of bit positions to be shifted. The following example circular shifts a 32-bit word 8 positions to the left.

CONTROL SIGNALS

SHIFT INSTRUCTION M2-M0	NUMBER OF BITS TO SHIFT SFT4-SFT0
10	01000

Assume D31-D0 is hex ABCD0123.

D31-D0

Input Data 1010 1011 1100 1101 0000 0001 0010 0011

Y31-Y0

Result 1100 1101 0000 0001 0010 0011 1010 1011

circular shift right (M1 – M0 = HL)

A circular right shift can be performed by placing the two's complement of the number of bit positions to be shifted on SFT4-SFT0 and using the circular left shift mode (M1 – M0 = HL). The following example circular shifts a 32-bit word 8 positions to the right.

CONTROL SIGNALS

SHIFT INSTRUCTION M2-M0	NUMBER OF BITS TO SHIFT SFT4-SFT0
10	11000

Assume D31-D0 is hex ABCD0123.

D31-D0

Input Data 1010 1011 1100 1101 0000 0001 0010 0011

Y31-Y0

Result 0010 0011 1010 1011 1100 1101 0000 0001

SN54AS8838, SN74AS8838 32-BIT BARREL SHIFTERS

arithmetic shift right (M1 – M0 = HH)

In the arithmetic shift right mode, SFT4-SFT0 define the number of bit positions to be shifted. The following example shifts a 32-bit word 8 positions to the right and fills the vacated bit positions with the sign bit (D31 from the input data).

CONTROL SIGNALS

SHIFT INSTRUCTION M2-M0	NUMBER OF BITS TO SHIFT SFT4-SFT0
11	11000

Assume D31-D0 is hex ABCD0123.

D31-D0

Input Data 1010 1011 1100 1101 0000 0001 0010 0011

Y31-Y0

Result 1111 1111 1010 1011 1100 1101 0000 0001

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage, VCC1	7 V
Supply voltage, VCC2	3 V
Input voltage	7 V
Operating case temperature range: SN54AS8838	-55°C to 125°C
Operating free-air temperature range: SN74AS8838	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

PARAMETER	SN54AS8838			SN74AS8838			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
VCC1 I/O supply voltage	4.5	5	5.5	4.5	5	5.5	V
VCC2 STL internal logic supply voltage	1.9	2	2.1	1.9	2	2.1	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage	0.8			0.8			V
I _{OH} High-level output current	-1			2.6			mA
I _{OL} Low-level output current	12			24			mA
T _A Operating free-air temperature	-55			0			°C
T _C Operating case temperature	125						°C

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS8838			UNIT	
			MIN	TYP [†]	MAX		
V _{IK}	V _{CC1} = 4.5 V,	I _I = -18 mA			-1.2	V	
V _{OH}	V _{CC1} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA		V _{CC} - 2			V	
	V _{CC1} = 4.5 V,	I _{OH} = -1 mA	2.4				
V _{OL}	V _{CC1} = 4.5 V,	I _{OL} = 12 mA	0.4			V	
	V _{CC1} = 4.5 V,	I _{OL} = 24 mA					
I _{OZH}	V _{CC1} = 5.5 V,	V _O = 2.7 V	20			μA	
I _{OZL}	V _{CC1} = 5.5 V,	V _I = 0.4 V	-0.4			mA	
I _I	V _{CC1} = 5.5 V,	V _I = 7 V	0.1			mA	
I _{IH}	V _{CC1} = 5.5 V,	V _I = 2.7 V	20			μA	
I _{IL}	V _{CC1} = 5.5 V,	V _I = 0.4 V	-0.4			mA	
I _O [‡]	V _{CC1} = 5.5 V,	V _O = 2.25 V	-30			-112	mA
I _{CC1}	V _{CC1} = 5.5 V		150			mA	
I _{CC2}	V _{CC2} = 2.1 V		145			mA	

switching characteristics over recommended operating temperature range (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω			UNIT
			SN54AS8838			
			MIN	TYP [†]	MAX	
t _{pd}	MUX1-MUX0	Y31-Y0	22			ns
	SFT4-SFT0	Y31-Y0	22			
	D31-D0	Y31-Y0	22			
t _{en}	YOEL	Y15-Y0	12			ns
	YOEM	Y31-Y16	12			
t _{dis}	YOEL	Y15-Y0	6			ns
	YOEM	Y31-Y16	6			

[†] All typical values are at V_{CC1} = 5 V, T_A = 25°C.

[‡] The output conditions have been chosen to produce a current that closely approximates one-half the true short-circuit current, I_OS.
NOTE 1: For load circuit and voltage waveforms, see pages 1-12 of *The TTL Data Book*, Volume 3, 1984.

SN74AS8838

32-BIT BARREL SHIFTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN74AS8838		UNIT
		MIN	MAX	
V_{IK}	$V_{CC1} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$		-1.2	V
V_{OH}	$V_{CC1} = 4.5 \text{ V to } 5.5 \text{ V}$, $I_{OH} = -0.4 \text{ mA}$	$V_{CC} - 2$		V
	$V_{CC1} = 4.5 \text{ V}$, $I_{OH} = -1 \text{ mA}$			
	$V_{CC1} = 4.5 \text{ V}$, $I_{OH} = -2.6 \text{ mA}$	2.4		
V_{OL}	$V_{CC1} = 4.5 \text{ V}$, $I_{OL} = 12 \text{ mA}$		0.4	V
	$V_{CC1} = 4.5 \text{ V}$, $I_{OL} = 24 \text{ mA}$		0.5	
I_{OZH}	$V_{CC1} = 5.5 \text{ V}$, $V_O = 2.7 \text{ V}$		20	μA
I_{OZL}	$V_{CC1} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$		-0.4	mA
I_I	$V_{CC1} = 5.5 \text{ V}$, $V_I = 7 \text{ V}$		0.1	mA
I_{IH}	$V_{CC1} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$		20	μA
I_{IL}	$V_{CC1} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$		-0.4	mA
I_O^\dagger	$V_{CC1} = 5.5 \text{ V}$, $V_O = 2.25 \text{ V}$	-30	-112	mA
I_{CC1}	$V_{CC1} = 5.5 \text{ V}$		150	mA
I_{CC2}	$V_{CC2} = 2.1 \text{ V}$		145	mA

† The output conditions have been chosen to produce a current that closely approximates one-half the true short-circuit current, I_{OS} .

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V}$, $C_L = 50 \text{ pF}$, $R_1 = 500 \Omega$, $R_2 = 500 \Omega$, $T_A = 25^\circ\text{C}$			$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $R_1 = 500 \Omega$, $R_2 = 500 \Omega$, $T_A = 0^\circ\text{C to } 70^\circ\text{C}$		UNIT
			SN74AS8838			SN74AS8838		
			MIN	TYP	MAX	MIN	MAX	
t_{pd}	MUX1-MUX0	Y31-Y0	22	26		29	ns	
	SFT4-SFT0	Y31-Y0		20	22	25		
	D31-D0	Y31-Y0		22	26	29		
t_{en}	YOEL	Y15-Y0		12	15	17	ns	
	YOEM	Y31-Y16		12	15	17		
t_{dis}	YOEL	Y15-Y0		6	8	10	ns	
	YOEM	Y31-Y16		6	8	10		

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- High-Speed 8-Bit Parallel Output Register
- Serial Shadow Register with Right-Shift Only
- 'ALS29818 Performs Parallel-to-Serial and Serial-to-Parallel Conversion
- Designed Specifically for Use in Applications such as:
 - Write Control Store ('ALS29818)
 - Serial Shadow-Register Diagnostics
- 'ALS29819 Provides Even-Parity Output
- Low Power Dissipation . . . 215 mW Typical
- 'ALS29818 is Functionally Equivalent to AMD AM29818
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

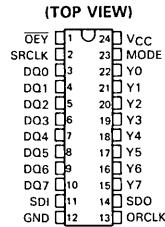
description

The 'ALS29818 and 'ALS29819 are 8-bit output registers with on-chip shadow register for use in applications such as write control store and shadow register diagnostics.

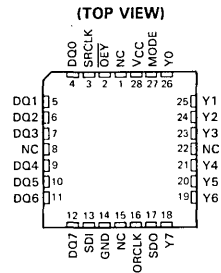
The output registers of the 'ALS29818 and 'ALS29819 are loaded in parallel from either the I/O port (DQ0—DQ7) or the shadow register. The shadow register of the 'ALS29818 is loaded serially from either the I/O port (Y0—Y7) or the output register. The 'ALS29819 shadow register is loaded serially from the I/O port (DQ0—DQ7). In addition, the 'ALS29819 provides a Parity-Even (PE) output, which monitors parity of the output register. Operation of these devices is controlled by the Mode and SDI inputs as shown in the function table.

The SN54ALS29818 and SN54ALS29819 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS29818 and SN74ALS29819 are characterized for operation from 0°C to 70°C.

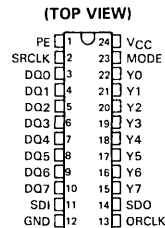
SN54ALS29818 . . . JT PACKAGE
SN74ALS29818 . . . DW OR NT PACKAGE



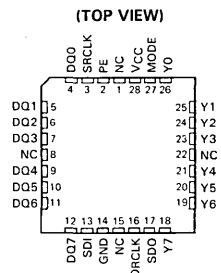
SN54ALS29818 . . . FK PACKAGE
SN74ALS29818 . . . FN PACKAGE



SN54ALS29819 . . . JT PACKAGE
SN74ALS29819 . . . DW OR JT PACKAGE



SN54ALS29819 . . . FK PACKAGE
SN74ALS29819 . . . FN PACKAGE



NC—No internal connection

2
LSI Devices

SN54ALS29818, SN54ALS29819
SN74ALS29818, SN74ALS29819
8-BIT DIAGNOSTICS/PIPELINE REGISTERS

'ALS29818 FUNCTION TABLE

INPUTS					OUTPUT AND I/O			OPERATION OR FUNCTION
MODE	OEY	SDI	SRCLK	ORCLK	SDO	Y0-Y7	DQ0-DQ7	
L	X	X	↑	X	SR7	—	HI-Z	Serial input, shift right, disable DQ0-DQ7
H	H	L	↑	X	SDI	INPUT	HI-Z	Parallel load shadow register from Y0-Y7, disable DQ0-DQ7
H	L	L	↑	No ↑	SDI	OUTPUT	HI-Z	Parallel load shadow register from output register, disable DQ0-DQ7
L	X	X	X	↑	SR7	—	INPUT [†]	Load output register from DQ0-DQ7
L	X	X	↑	↑	SR7	—	INPUT [†]	Load output register from DQ0-DQ7 while shifting shadow register
H	X	X	No ↑	↑	SDI	—	—	Load output register from shadow register
H	X	X	X	X	SDI	—	—	Serial data in to serial data out
H	L	L	↑	↑	SDI	OUTPUT	HI-Z	Exchange data between registers, DQ0-DQ7 disabled
H	X	H	X	X	SDI	—	—	Hold shadow register, transitions on SRCLK do not effect shadow register
H	X	H	↑	X	SDI	—	OUTPUT	Enable DQ0-DQ7 for parallel shadow register output

[†]The DQ0-DQ7 outputs must be disabled before applying data to DQ0-DQ7.

'ALS29819 FUNCTION TABLE

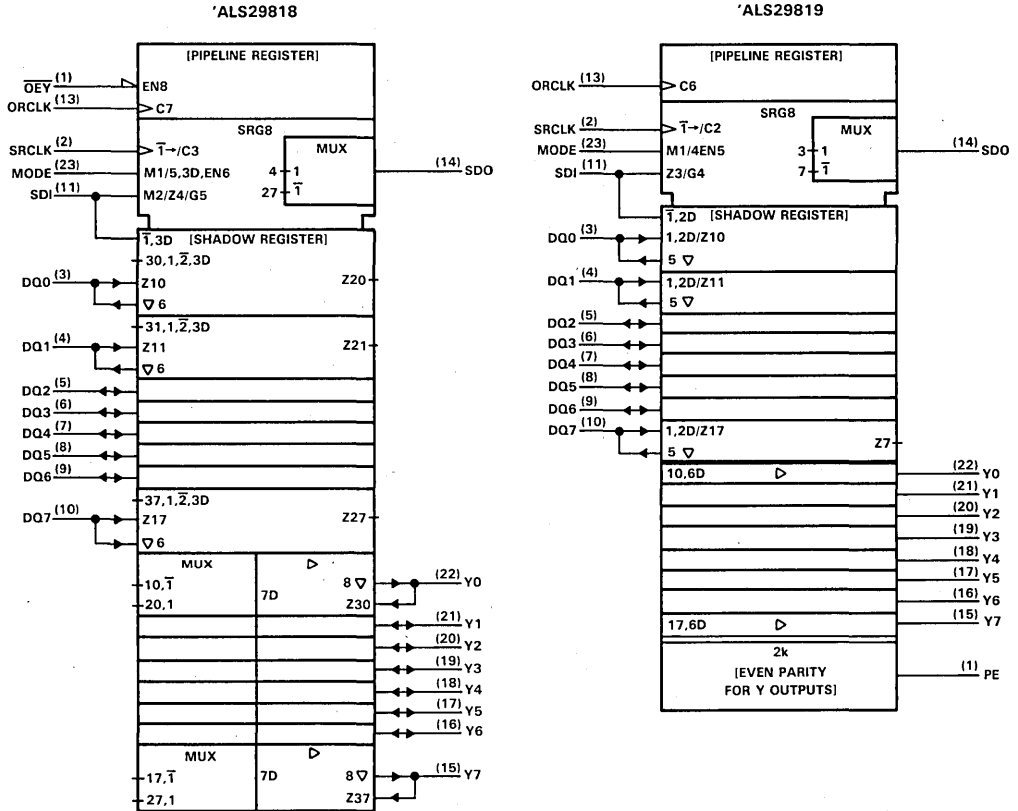
INPUTS				OUTPUT AND I/O			OPERATION OR FUNCTION
MODE	SDI	SRCLK	ORCLK	SDO	Y0-Y7 PE	DQ0-DQ7	
L	X	↑	X	SR7	OUTPUT	HI-Z	Serial input, shift right
H	L	↑	X	SDI (L)	OUTPUT	INPUT	Parallel load shadow register from DQ0-DQ7
H	L	↑	↑	SDI (L)	OUTPUT	INPUT	Parallel load shadow register and output register from DQ0-DQ7
L	X	X	↑	SR7	OUTPUT	INPUT	Load output register from DQ0-DQ7
X	L	X	↑	SR7	OUTPUT	INPUT	Load output register from DQ0-DQ7 while shifting shadow register
L	X	↑	↑	SR7	OUTPUT	INPUT	Load output register from DQ0-DQ7 while shifting shadow register
H	H	No ↑	↑	SDI (H)	OUTPUT	OUTPUT	Load output register from shadow register
H	X	X	X	SDI	OUTPUT	—	Serial data in to serial data out
H	H	X	X	SDI (H)	OUTPUT	OUTPUT HOLD	Hold shadow register, enable DQ0-DQ7, transitions on SRCLK ignored
L	X	X	X	—	OUTPUT	HI-Z	Disable DQ0-DQ7 outputs
X	L	X	X	—	OUTPUT	HI-Z	Disable DQ0-DQ7 outputs

2

LSI Devices

**SN54ALS29818, SN54ALS29819
SN74ALS29818, SN74ALS29819
8-BIT DIAGNOSTICS/PIPELINE REGISTERS**

logic symbols †

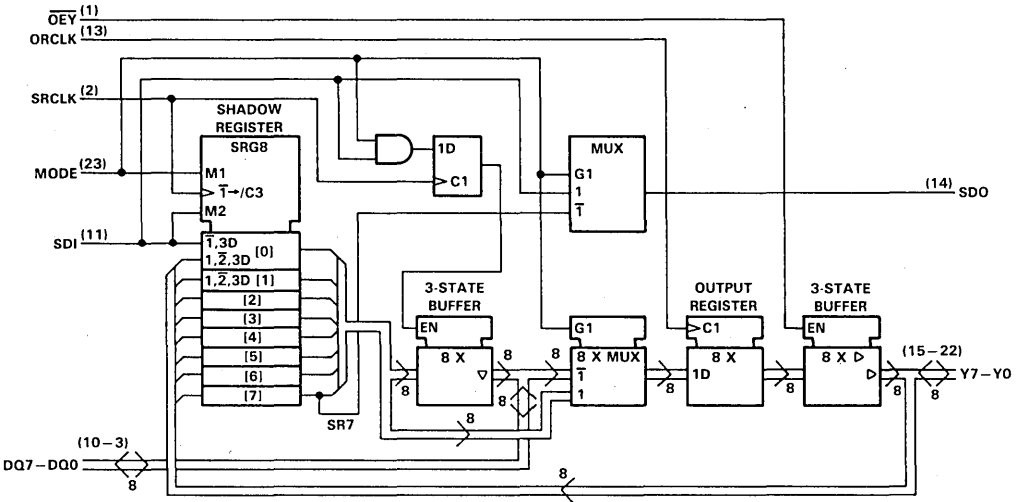


†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

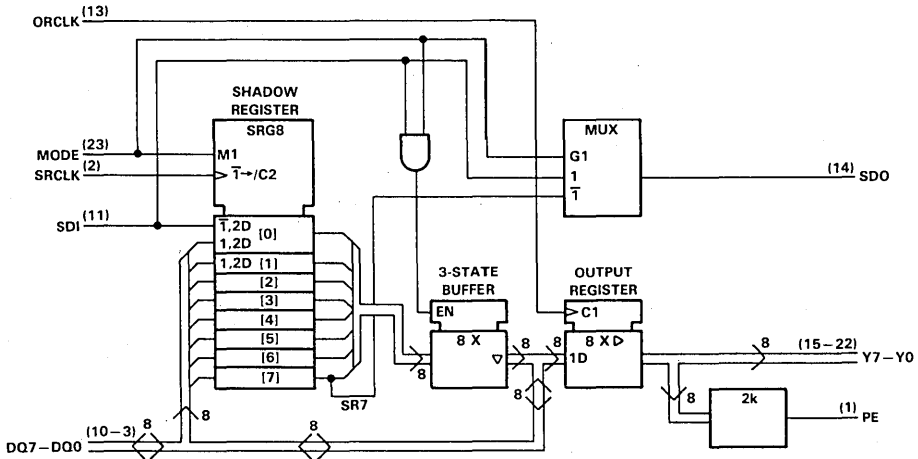
**SN54ALS29818, SN54ALS29819
SN74ALS29818, SN74ALS29819
8-BIT DIAGNOSTICS/PIPELINE REGISTERS**

logic diagrams (positive logic)

'ALS29818



'ALS29819

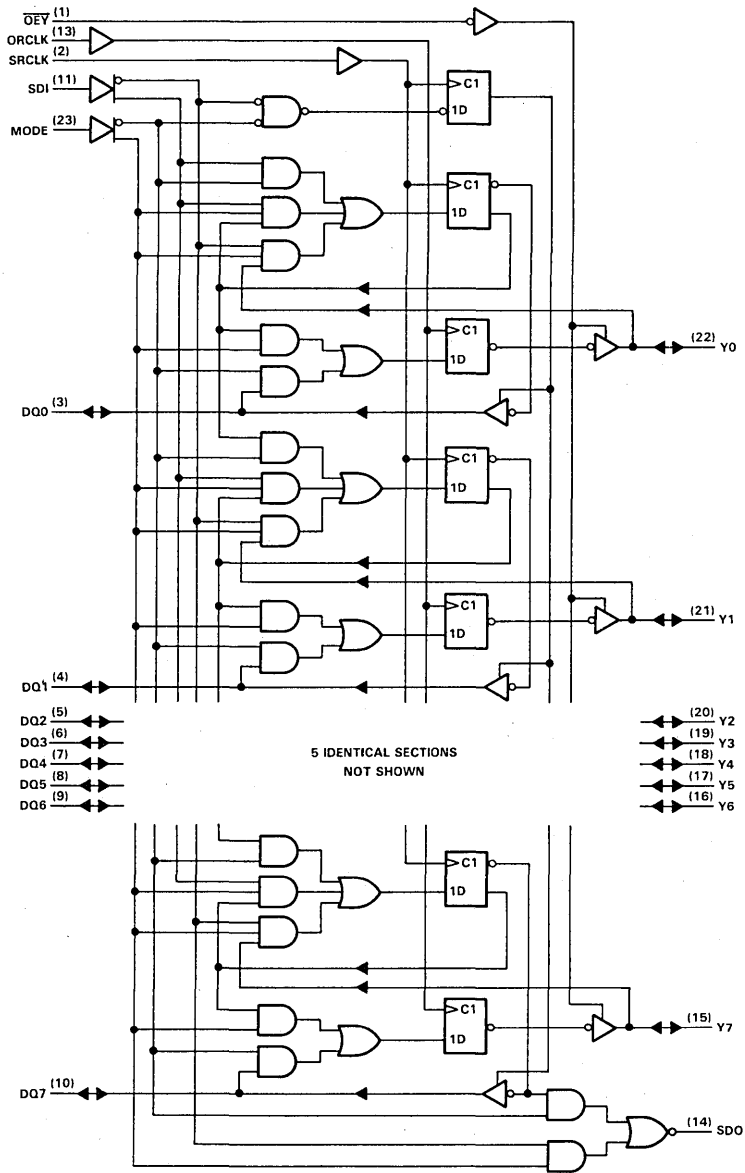


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LSI Devices

SN54ALS29818
 SN74ALS29818
 8-BIT DIAGNOSTICS/PIPELINE REGISTERS

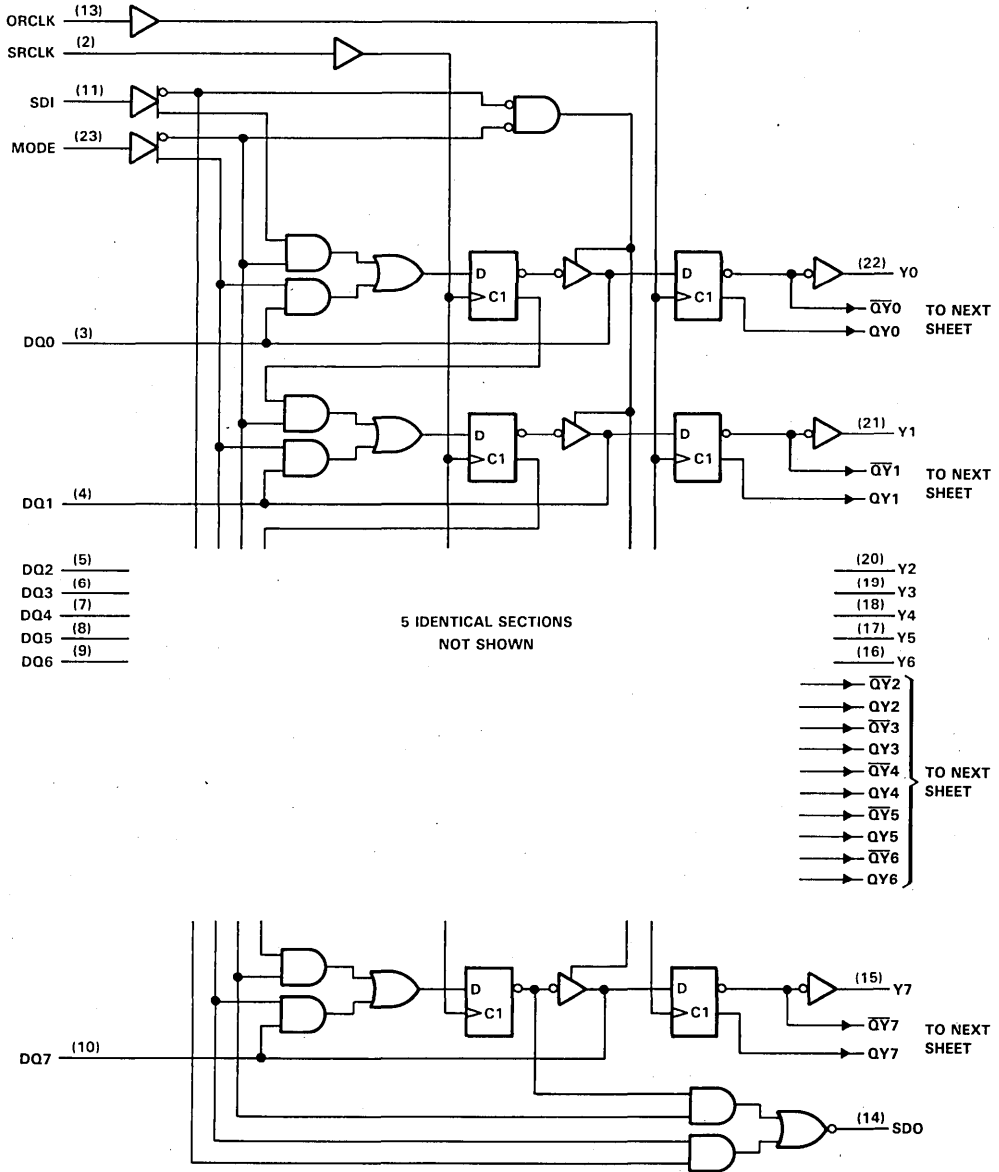
'ALS29818 gate-level logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

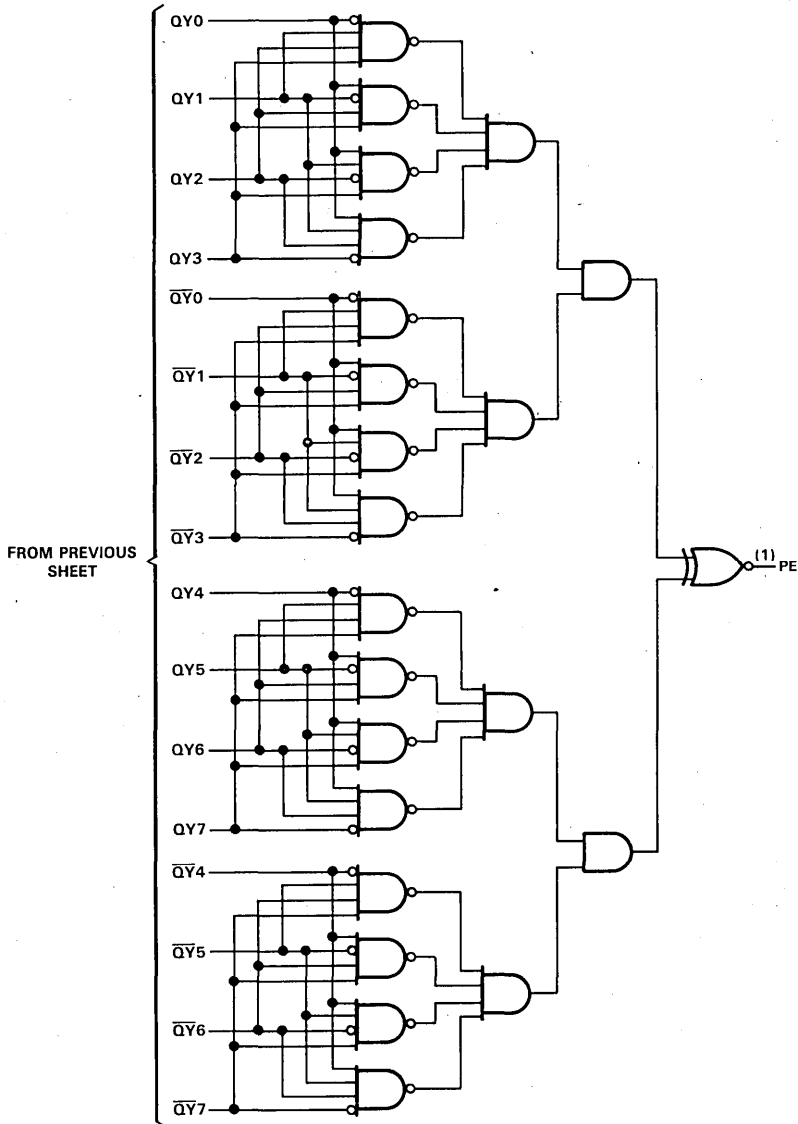
**SN54ALS29819
SN74ALS29819
8-BIT DIAGNOSTICS/PIPELINE REGISTERS**

'ALS29819 gate-level logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

'ALS29819 gate-level logic diagram (positive logic) (continued)



Pin numbers shown are for DW, JT, and NT packages.

2
 LSI Devices

SN54ALS29818, SN54ALS29819
SN74ALS29818, SN74ALS29819
8-BIT DIAGNOSTICS/PIPELINE REGISTERS

absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC}	7 V
Input voltage, any input or I/O port	5.5 V
Operating free-air temperature range: SN54ALS ¹	-55°C to 125°C
SN74ALS ¹	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54ALS29818			SN74ALS29818			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current	Y0-Y7		-3	-3			mA
		All others		-1	-1			
I_{OL}	Low-level output current	Y0-Y7		16	24			mA
		All others		4	8			
f_{clock}	Clock frequency	SRCLK						MHz
		ORCLK						
t_w	Pulse duration	SRCLK high or low						ns
		ORCLK high or low						
t_{su}	Setup time before SRCLK [†]	Y0-Y7						ns
		MODE						
		SDI						
		ORCLK ('ALS29818) [†]						
t_{su}	Setup time before ORCLK [†]	DQ0-DQ7						ns
		MODE						
		SRCLK [‡]						
t_h	Hold time after SRCLK [†]	Y0-Y7						ns
		MODE						
		SDI						
t_h	Hold time after ORCLK [†]	DQ0-DQ7						ns
		MODE						
		SDI ('ALS29819)						
T_A	Operating free-air temperature	-55		125	0		70	°C

[†] This setup time ensures that the shadow register will see stable data from the output register.

[‡] This setup time ensures that the output register will see stable data from the shadow register.

SN54ALS29818, SN54ALS29819
SN74ALS29818, SN74ALS29819
8-BIT DIAGNOSTICS/PIPELINE REGISTERS

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54ALS29818 SN54ALS29819		SN74ALS29818 SN74ALS29819		UNIT		
		MIN	TYP‡	MAX	MIN		TYP‡	MAX
		V_{IK}	$V_{CC} = \text{MIN}, I_I = 18 \text{ mA}$				-1.2	
V_{OH}	All outputs	$V_{CC} = \text{MIN to MAX}, I_{OH} = -0.4 \text{ mA}$		$V_{CC}-2$		$V_{CC}-2$	V	
	Y0-Y7	$V_{CC} = \text{MIN}, I_{OH} = -3 \text{ mA}$		2.4	3.2	2.4 3.2		
	All others	$V_{CC} = \text{MIN}, I_{OH} = -1 \text{ mA}$				2.4 3.2		
V_{OL}	All outputs	$V_{CC} = \text{MIN}, I_{OL} = 4 \text{ mA}$		0.25	0.5	0.25 0.5	V	
		$V_{CC} = \text{MIN}, I_{OL} = 8 \text{ mA}$				0.35 0.5		
	Y0-Y7	$V_{CC} = \text{MIN}, I_{OL} = 16 \text{ mA}$		0.25	0.5	0.25 0.5		
		$V_{CC} = \text{MIN}, I_{OL} = 24 \text{ mA}$				0.35 0.5		
I_I	MODE	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$		0.4		0.4	mA	
	SRCLK			0.3		0.3		
	SDI, OEY			0.2		0.2		
	All others§			0.1		0.1		
I_{IH}	MODE	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$		80		80	μA	
	SRCLK			60		60		
	SDI, OEY			40		40		
	All others§			20		20		
I_{IL}	MODE	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$		-0.4		-0.4	mA	
	SRCLK			-0.3		-0.3		
	SDI, OEY			-0.2		-0.2		
	All others§			-0.1		-0.1		
I_{OS}^\dagger	$V_{CC} = \text{MAX}, V_O = 0$	-75	-250	-75	-250	mA		
I_{CC}	$V_{CC} = \text{MAX}$ (see Note 1)	43		43		mA		

† For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

¶ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

NOTE 1: I_{CC} is measured with all three-state outputs in the high-impedance state.

2

LSI Devices

SN54ALS29818
SN74ALS29818
8-BIT DIAGNOSTICS/PIPELINE REGISTERS

'ALS29818 switching characteristics (see Note 2)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	$V_{CC} = 5 V,$ $C_L = 50 pF,$ $T_A = 25^\circ C$			$V_{CC} = \text{MIN TO MAX,}^\dagger$ $C_L = 50 pF,$ $T_A = \text{MIN TO MAX}^\dagger$				UNIT
					'ALS29818			SN54ALS29818		SN74ALS29818		
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}	SRCLK				37						MHz	
	ORCLK				37							
t _{PLH}	MODE	SDO	R _L = 2 kΩ		8						ns	
t _{PHL}					8							
t _{PLH}	SDI	SDO	R _L = 2 kΩ		8						ns	
t _{PHL}					8							
t _{PLH}	ORCLK	Y0-Y7	R1 = 1 kΩ, R2 = 280 Ω		9						ns	
t _{PHL}					9							
t _{PLH}	SRCLK	SDO	R _L = 2 kΩ		13						ns	
t _{PHL}					13							
t _{PLH}	SRCLK	DQ0-DQ7	R1 = 5 kΩ, R2 = 2 kΩ								ns	
t _{PHL}												
t _{PZH}	SRCLK	DQ0-DQ7	R1 = 5 kΩ, R2 = 2 kΩ		16						ns	
t _{PZL}					19							
t _{PHZ}	SRCLK	DQ0-DQ7	R1 = 5 kΩ, R2 = 2 kΩ		16						ns	
t _{PLZ}					19							
t _{PHZ}	$\overline{OE}V$	Y0-Y7	R1 = 1 kΩ, R2 = 280 Ω		7						ns	
t _{PLZ}					10							
t _{PZH}	$\overline{OE}V$	Y0-Y7	R1 = 1 kΩ, R2 = 280 Ω		6						ns	
t _{PZL}					9							

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN54ALS29819
SN74ALS29819
8-BIT DIAGNOSTICS/PIPELINE REGISTERS

ALS29819 switching characteristics (see Note 2)

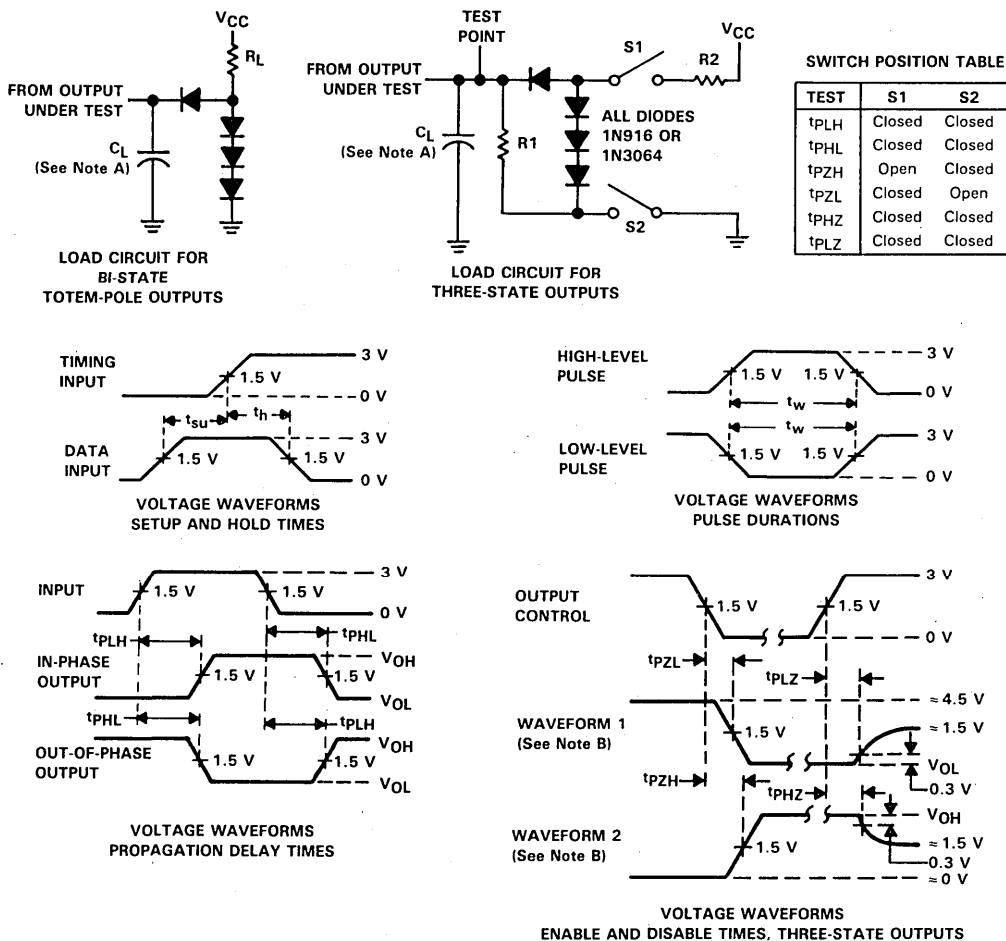
PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	V _{CC} = 5 V, C _L = 50 pF, T _A = 25 °C			V _{CC} = MIN TO MAX, [†] C _L = 50 pF, T _A = MIN TO MAX [†]				UNIT
					ALS29819			SN54ALS29819		SN74ALS29819		
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}	SRCLK				37							MHz
	ORCLK				37							
t _{PLH}	MODE	SDO	R _L = 2 kΩ		8							ns
t _{PHL}					8							
t _{PLH}	SDI	SDO	R _L = 2 kΩ		8							ns
t _{PHL}					8							
t _{PLH}	ORCLK	Y0-Y7	R _L = 2 kΩ		9							ns
t _{PHL}					9							
t _{PLH}	ORCLK	PE	R _L = 2 kΩ		9							ns
t _{PHL}					5							
t _{PLH}	SRCLK	SDO	R _L = 2 kΩ		13							ns
t _{PHL}					13							
t _{PLH}	SRCLK	DQ0-DQ7	R1 = 5 kΩ,		12							ns
t _{PHL}				R2 = 2 kΩ		12						
t _{PZH}	MODE or SDI	DQ0-DQ7	R1 = 5 kΩ,		7							ns
t _{PZL}				R2 = 2 kΩ		9						
t _{PHZ}	MODE or SDI	DQ0-DQ7	R1 = 5 kΩ,		7							ns
t _{PLZ}				R2 = 2 kΩ		9						

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

2
LSI Devices

SN54ALS29818, SN54ALS29819
SN74ALS29818, SN74ALS29819
8-BIT DIAGNOSTICS/PIPELINE REGISTERS

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_o = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

FIGURE 1

2

LSI Devices

**SN54ALS29821, SN54ALS29822
SN74ALS29821, SN74ALS29822
10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS**

D2825, JANUARY 1986

- Functionally Equivalent to AMD's AM29821 and AM29822
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- Outputs Have Undershoot Protection Circuitry
- Power-Up High-Impedance State
- Package Options Include Both Plastic and Ceramic Carriers in Addition to Plastic and Ceramic DIPs
- Buffered Control Inputs to Reduce DC Loading Effects
- Dependable Texas Instruments Quality and Reliability

description

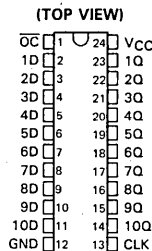
These 10-bit flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock the Q outputs on the 'ALS29821 will be true, and on the 'ALS29822 will be complementary to the data input.

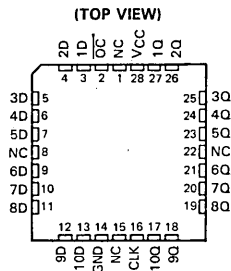
A buffered output-control (\overline{OC}) input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74' family is characterized for operation from 0°C to 70°C .

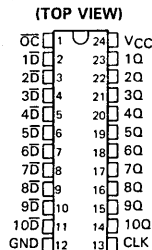
SN54ALS29821 . . . JT PACKAGE
SN74ALS29821 . . . DW OR NT PACKAGE



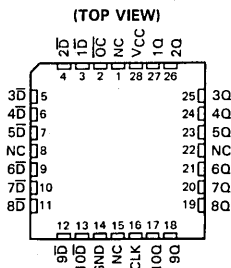
SN54ALS29821 . . . FK PACKAGE
SN74ALS29821 . . . FN PACKAGE



SN54ALS29822 . . . JT PACKAGE
SN74ALS29822 . . . DW OR NT PACKAGE



SN54ALS29822 . . . FK PACKAGE
SN74ALS29822 . . . FN PACKAGE



NC—No internal connection

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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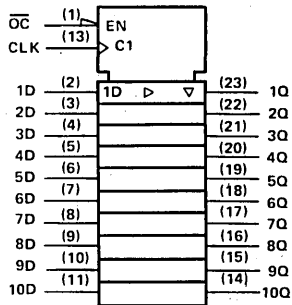
SN54ALS29821, SN74ALS29821

10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

'ALS29821 FUNCTION TABLE (EACH FLIP-FLOP)

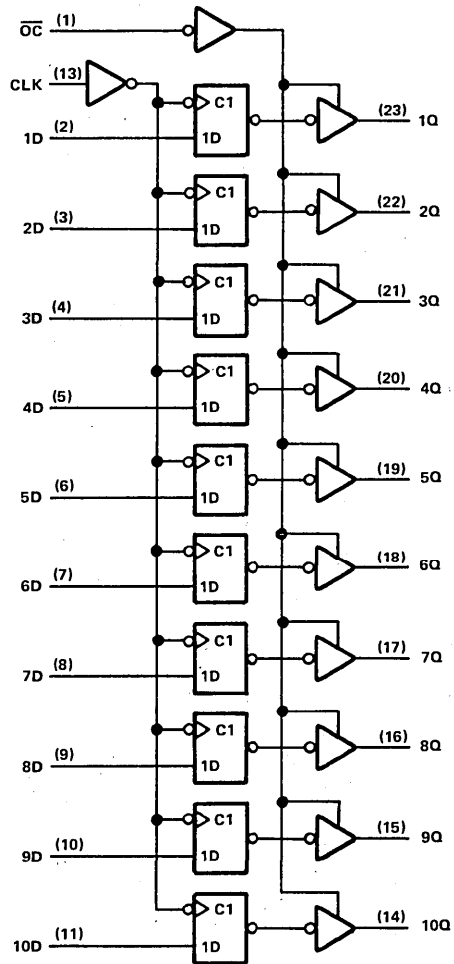
INPUTS			OUTPUT
\overline{OC}	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

'ALS29821 logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

'ALS29821 logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

2

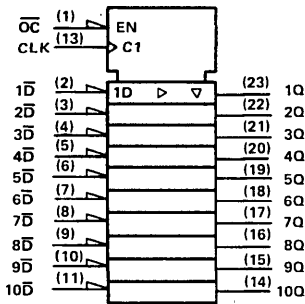
LSI Devices

SN54ALS29822, SN74ALS29822 10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

'ALS29822 FUNCTION TABLE (EACH FLIP-FLOP)

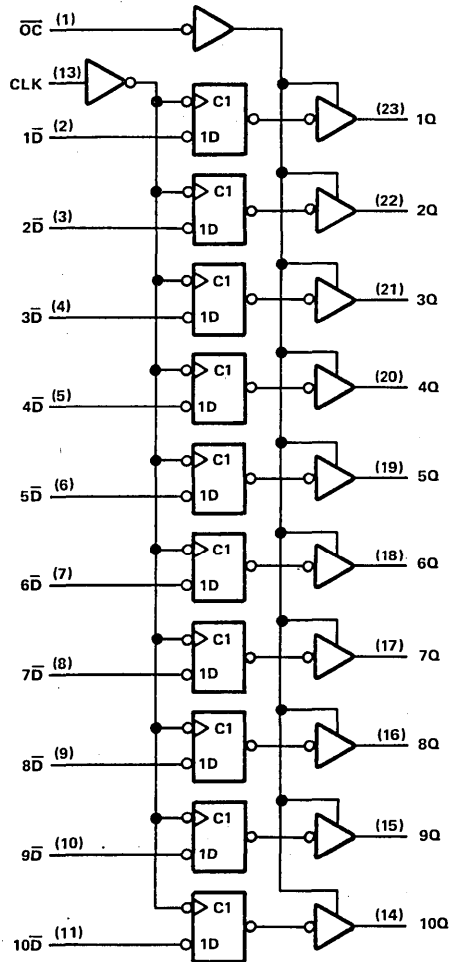
INPUTS			OUTPUT
\overline{OC}	CLK	\overline{D}	Q
L	↑	H	L
L	↑	L	H
L	L	X	Q_0
H	X	X	Z

'ALS29822 logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

'ALS29822 logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

2
 LSI Devices

SN54AS29821, SN54AS29822, SN74AS29821, SN74AS29822

10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	5.5 V
Voltage applied to a disabled 3-state output	5.5 V
Input current	100 mA
Output current	-30 mA to 5 mA
Operating free-air temperature range: SN54ALS29821, SN54ALS29822	-55°C to 125°C
SN74ALS29821, SN74ALS29822	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54ALS29821			SN74ALS29821			UNIT
		SN54ALS29822			SN74ALS29822			
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage	0.8			0.8			V
I_{OH}	High-level output current	-15			-24			mA
I_{OL}	Low-level output current	32			48			mA
t_w	Pulse duration, CLK high or low							ns
t_{su}	Setup time, data before CLK \uparrow							ns
t_h	Hold time, data after CLK \uparrow							ns
T_A	Operating free-air temperature	-55	125		0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS \dagger	SN54ALS29821		SN74ALS29821		UNIT	
		SN54ALS29822		SN74ALS29822			
		MIN	TYP \ddagger MAX	MIN	TYP \ddagger MAX		
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$	-1.2		-1.2		V	
V_{OH}	$V_{CC} = \text{MIN to MAX}, I_{OH} = -0.4 \text{ mA}$	$V_{CC} - 2$		$V_{CC} - 2$		V	
	$V_{CC} = \text{MIN}, I_{OH} = -15 \text{ mA}$	2.4	3.3				
	$V_{CC} = \text{MIN}, I_{OH} = -24 \text{ mA}$			2.4	3.2		
V_{OL}	$V_{CC} = \text{MIN}, I_{OL} = 32 \text{ mA}$	0.25	0.4	0.25	0.4	V	
	$V_{CC} = \text{MIN}, I_{OL} = 48 \text{ mA}$			0.35	0.5		
I_{OZH}	$V_{CC} = \text{MAX}, V_O = 2.4 \text{ V}$	20		20		μA	
I_{OZL}	$V_{CC} = \text{MAX}, V_O = 0.4 \text{ V}$	-20		-20		μA	
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$	0.1		0.1		mA	
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$	20		20		μA	
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$	-0.1		-0.1		mA	
I_{OS}^{\S}	$V_{CC} = \text{MAX}, V_O = 0$	-75	-250	-75	-250	mA	
I_{CC}	'ALS29821	$V_{CC} = \text{MAX}$	Outputs high				mA
			Outputs low				
			Outputs disabled		48	48	
			Outputs high				
			Outputs low				
			Outputs disabled		48	48	
	'ALS29822						

\dagger For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

\ddagger All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

\S Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Additional information on these products can be obtained from the factory as it becomes available.

SN54ALS29821, SN54ALS29822, SN74ALS29821, SN74ALS29822
10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	V _{CC} = 5 V, T _A = 25°C			V _{CC} = MIN TO MAX, [†] T _A = MIN TO MAX [†]				UNIT
				'ALS29821 'ALS29822			SN54ALS29821 SN54ALS29822		SN74ALS29821 SN74ALS29822		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	CLK	Any Q	C _L = 300 pF							ns	
t _{PHL}											
t _{PLH}					6						
t _{PHL}					7						
t _{PZH}	\overline{OC}	Any Q	C _L = 300 pF							ns	
t _{PZL}											
t _{PZH}					12						
t _{PZL}					11						
t _{PHZ}	\overline{OC}	Any Q	C _L = 50 pF							ns	
t _{PLZ}											
t _{PHZ}					5						
t _{PLZ}					6						

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

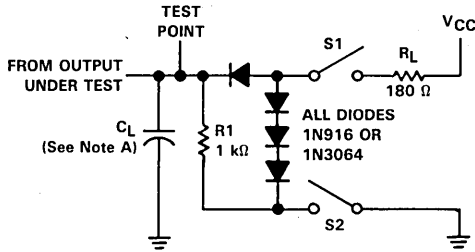
Additional information on these products can be obtained from the factory as it becomes available.



LSI Devices

SN54AS29821, SN54AS29822, SN74AS29821, SN74AS29822
10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

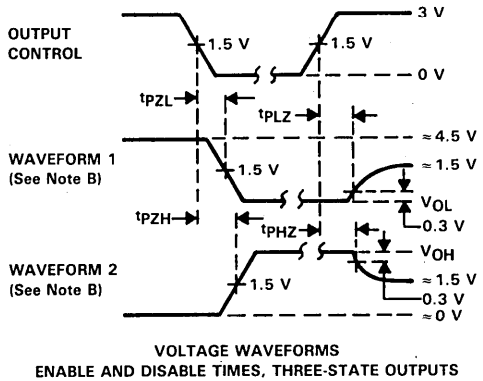
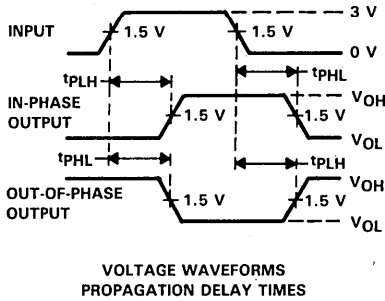
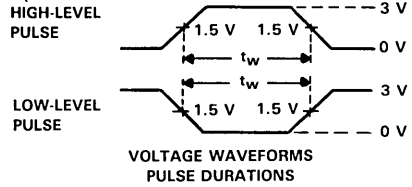
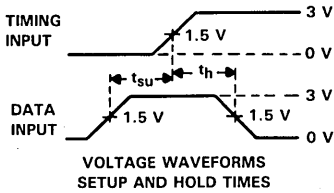
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

SWITCH POSITION TABLE

TEST	S1	S2
t _{PLH}	Closed	Closed
t _{PHL}	Closed	Closed
t _{PZH}	Open	Closed
t _{PZL}	Closed	Open
t _{PHZ}	Closed	Closed
t _{PLZ}	Closed	Closed



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_o = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

FIGURE 1

- Functionally Equivalent to AMD's AM29823 and AM29824
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- Outputs Have Undershoot Protection Circuitry
- Power-Up High-Impedance State
- Buffered Control Inputs to Reduce DC Loading Effects
- Package Options Include both Plastic and Ceramic Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

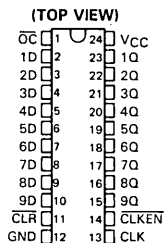
description

These 9-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing and working registers.

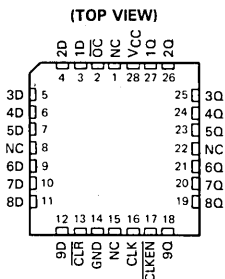
With the clock enable ($\overline{\text{CLKEN}}$) low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{\text{CLKEN}}$ high will disable the clock buffer, thus latching the outputs. The 'ALS29823 has noninverting D inputs and the 'ALS29824 has inverting D inputs. Taking the $\overline{\text{CLR}}$ input low causes the nine Q outputs to go low independently of the clock.

A buffered output-control input ($\overline{\text{OC}}$) can be used to place the nine outputs in either normal logic state (high or low level) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

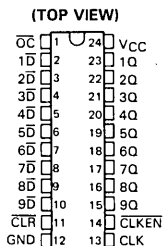
SN54ALS29823 . . . JT PACKAGE
SN74ALS29823 . . . DW OR NT PACKAGE



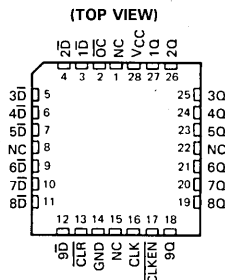
SN54ALS29823 . . . FK PACKAGE
SN74ALS29823 . . . FN PACKAGE



SN54ALS29824 . . . JT PACKAGE
SN74ALS29824 . . . DW OR NT PACKAGE



SN54ALS29824 . . . FK PACKAGE
SN74ALS29824 . . . FN PACKAGE



SN54ALS29823, SN54ALS29824, SN74ALS29823, SN74ALS29824

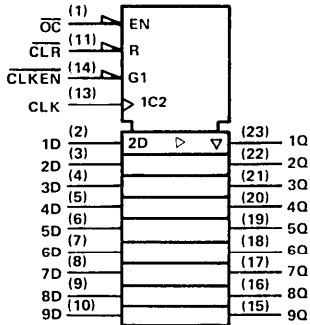
9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

The SN54AS' family is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74AS' family is characterized for operation from 0°C to 70°C.

'ALS29823 FUNCTION TABLE

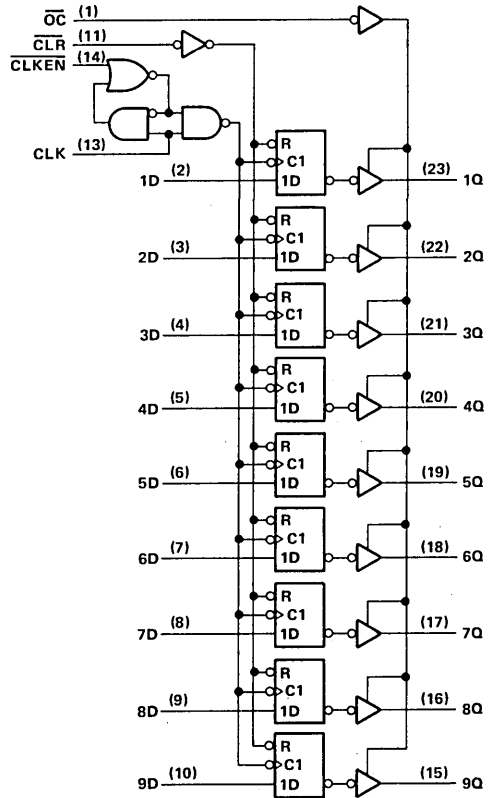
INPUTS					OUTPUT
\overline{OC}	CLR	CLKEN	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q ₀
H	X	X	X	X	Z

'ALS29823 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

'ALS29823 logic diagram (positive logic)



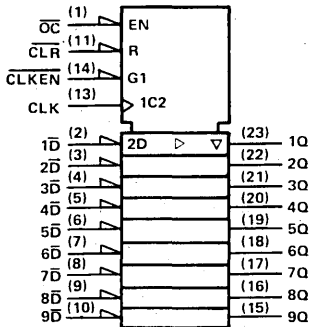
Pin numbers shown are for DW, JT, and NT packages.

SN54ALS29824, SN74ALS29824 9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

'ALS29824 FUNCTION TABLE

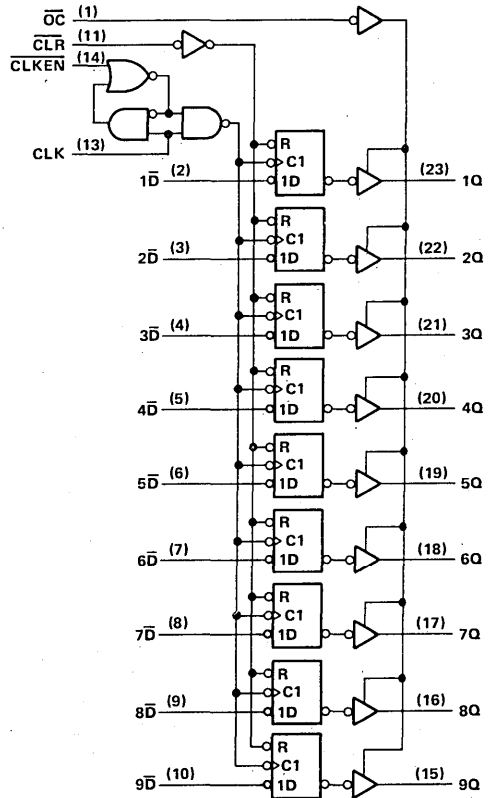
INPUTS					OUTPUT
\overline{OC}	\overline{CLR}	CLKEN	CLK	\overline{D}	Q
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	Q_0
H	X	X	X	X	Z

'ALS29824 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'ALS29824 logic diagram (positive logic)



2
LSI Devices

Pin numbers shown are for DW, JT, and NT packages.

SN54ALS29823, SN54ALS29824, SN74ALS29823, SN74ALS29824
9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	5.5 V
Voltage applied to a disabled 3-state output	5.5 V
Input current	100 mA
Output current	-30 mA to 5 mA
Operating free-air temperature range: SN54ALS29823, SN54ALS29824	-55 °C to 125 °C
SN74ALS29823, SN74ALS29824	0 °C to 70 °C
Storage temperature range	-65 °C to 150 °C

recommended operating conditions

		SN54ALS29823			SN74ALS29823			UNIT
		SN54ALS29824			SN74ALS29824			
		MIN	NOM	MAX	MIN	NOM	MAX	
VCC	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			-15			-24	mA
I _{OL}	Low-level output current			32			48	mA
t _w	Pulse duration	CLR low						ns
		CLK high or low						
t _{su}	Setup time before CLK†	CLR inactive						ns
		Data						
		CLKEN high or low						
t _h	Hold time, CLKEN or data after CLK†							ns
T _A	Operating free-air temperature	-55		125	0		70	°C

2 LSI Devices

SN54ALS29823, SN54ALS29824, SN74ALS29823, SN74ALS29824 9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54ALS29823		SN74ALS29823		UNIT		
			SN54ALS29824		SN74ALS29824				
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN	I _I = -18 mA			-1.2			-1.2	V
V _{OH}	V _{CC} = MIN to MAX,	I _{OH} = -0.4 mA	V _{CC} -2		V _{CC} -2				V
	V _{CC} = MIN,	I _{OH} = -15 mA	2.4	3.3					
	V _{CC} = MIN,	I _{OH} = -24 mA			2.4	3.2			
V _{OL}	V _{CC} = MIN,	I _{OL} = 32 mA	0.25	0.4	0.25	0.4		V	
	V _{CC} = MIN,	I _{OL} = 48 mA			0.35	0.5			
I _{OZH}	V _{CC} = MAX,	V _O = 2.4 V		20		20		μA	
I _{OZL}	V _{CC} = MAX,	V _O = 0.4 V		-20		-20		μA	
I _I	V _{CC} = MAX,	V _I = 5.5 V		0.1		0.1		mA	
I _{IH}	V _{CC} = MAX,	V _I = 2.7 V		20		20		μA	
I _{IL}	V _{CC} = MAX,	V _I = 0.4 V		-0.1		-0.1		mA	
I _{OS} §	V _{CC} = MAX,	V _O = 0	-75		-250	-75		-250	mA
I _{CC}	'ALS29823	V _{CC} = MAX	Outputs high						mA
			Outputs low						
	Outputs disabled		48		48				
	Outputs high								
	Outputs low								
	Outputs disabled		48		48				
'ALS29824	Outputs high								
	Outputs low								

† For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Additional Information on these products can be obtained from the factory as it becomes available.

2

LSI Devices

SN54ALS29823, SN54ALS29824, SN74ALS29823, SN74ALS29824

9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	V _{CC} = 5 V, T _A = 25°C		V _{CC} = MIN TO MAX, [†] T _A = MIN TO MAX [†]				UNIT
				'ALS29823		SN54ALS29823		SN74ALS29823		
				'ALS29824		SN54ALS29824		SN74ALS29824		
MIN	TYP	MAX	MIN	MAX	MIN	MAX				
t _{PLH}	CLK	Any Q	C _L = 300 pF						ns	
t _{PHL}										
t _{PLH}					5.5					
t _{PHL}					6.5					
t _{PHL}	CLR	Any Q	C _L = 50 pF		13				ns	
t _{PZH}	OC	Any Q	C _L = 300 pF						ns	
t _{PZL}										
t _{PZH}					12					
t _{PZL}			C _L = 50 pF		11					
t _{PHZ}	OC	Any Q	C _L = 50 pF						ns	
t _{PLZ}										
t _{PHZ}					5					
t _{PLZ}					5.5					

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

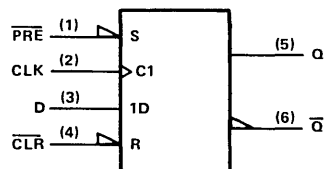
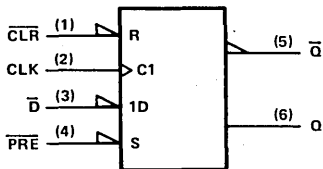
Additional information on these products can be obtained from the factory as it becomes available.

D flip-flop signal conventions

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called \bar{Q} . An input that causes a Q output to go high or a \bar{Q} output to go low is called Preset; an input that causes a Q output to go high or a \bar{Q} output to go low is called Clear. Bars are used over these pin names (PRE and CLR) if they are active-low.

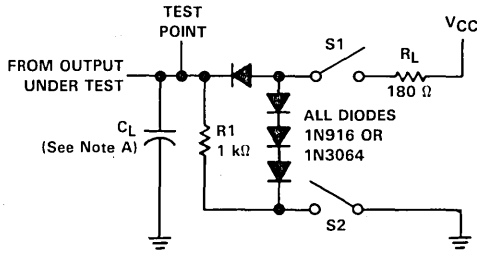
The devices on this data sheet are second-source designs and the pin-name convention used by the original manufacturer has been retained. That makes it necessary to designate the inputs and outputs of the inverting circuit D and \bar{Q} . In some applications it may be advantageous to redesignate the inputs and outputs as D and Q. In that case, outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.

Notice that Q and \bar{Q} exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators ($\bar{\square}$) on PRE and CLR remain since these inputs are still active-low, but that the presence or absence of the polarity changes at D, Q, and \bar{Q} . Of course pin 5 (\bar{Q}) is still in phase with the data input D, but now both are considered active high.



SN54ALS29823, SN54ALS29824, SN74ALS29823, SN74ALS29824 9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

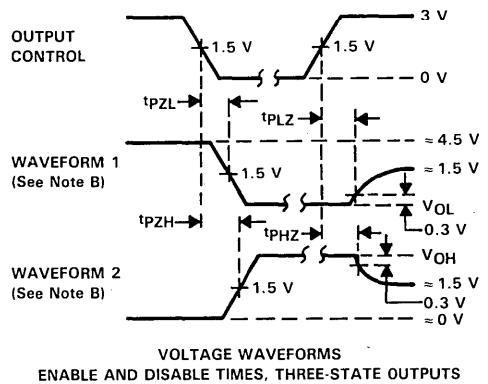
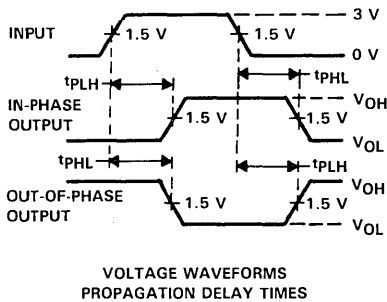
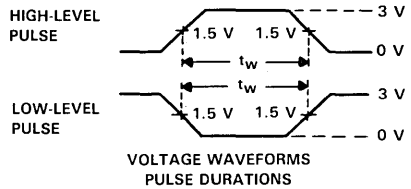
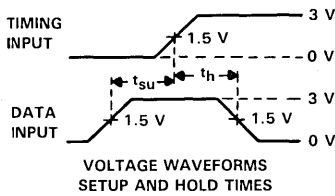
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

SWITCH POSITION TABLE

TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_o = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

FIGURE 1



LSI Devices

**SN54ALS29825, SN54ALS29826
SN74ALS29825, SN74ALS29826
8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS**

D2829, JANUARY 1986

- Functionally Equivalent to AMD's AM29825 and AM29826
- Improved IOH Specifications
- Multiple Output Enables Allow Multiuser Control of the Interface
- Outputs Have Undershoot Protection Circuitry
- Power-Up High-Impedance State
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Buffered Control Inputs to Reduce DC Loading Effect
- Dependable Texas Instruments Quality and Reliability

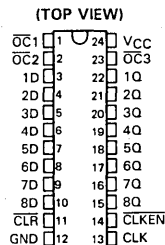
description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing multiuser registers, I/O ports, bidirectional bus drivers, and working registers.

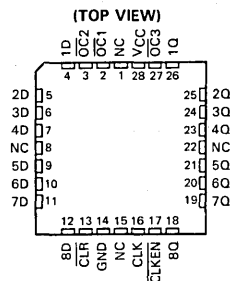
With the clock enable ($\overline{\text{CLKEN}}$) low, the eight D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{\text{CLKEN}}$ high will disable the clock buffer, thus latching the outputs. The 'ALS29825 has non-inverting D inputs and the 'ALS29826 has inverting $\overline{\text{D}}$ inputs. Taking the $\overline{\text{CLR}}$ input low causes the eight Q outputs to go low independently of the clock.

Multiuser buffered output-control inputs ($\overline{\text{OC1}}$, $\overline{\text{OC2}}$, and $\overline{\text{OC3}}$) can be used to place the eight outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

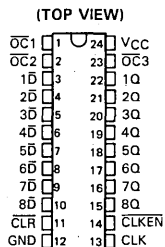
SN54ALS29825 . . . JT PACKAGE
SN74ALS29825 . . . DW OR NT PACKAGE



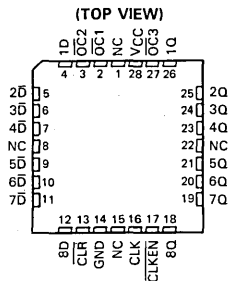
SN54ALS29825 . . . FK PACKAGE
SN74ALS29825 . . . FN PACKAGE



SN54ALS29826 . . . JT PACKAGE
SN74ALS29826 . . . DW OR NT PACKAGE



SN54ALS29826 . . . FK PACKAGE
SN74ALS29826 . . . FN PACKAGE



NC—No internal connection

SN54ALS29825, SN54ALS29826 SN74ALS29825, SN74ALS29826 8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C .
The SN74' family is characterized for operation from 0°C to 70°C .

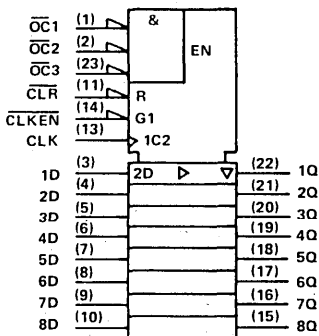
'ALS29825 FUNCTION TABLE

INPUTS					OUTPUT
$\overline{\text{OC}}^*$	CLR	CLKEN	CLK	D	Q
L	L	X	X	X	L
L	H	L	\uparrow	H	H
L	H	L	\uparrow	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

$\overline{\text{OC}}^* = \text{H}$ if any of $\overline{\text{OC}}1$, $\overline{\text{OC}}2$, or $\overline{\text{OC}}3$ is high.

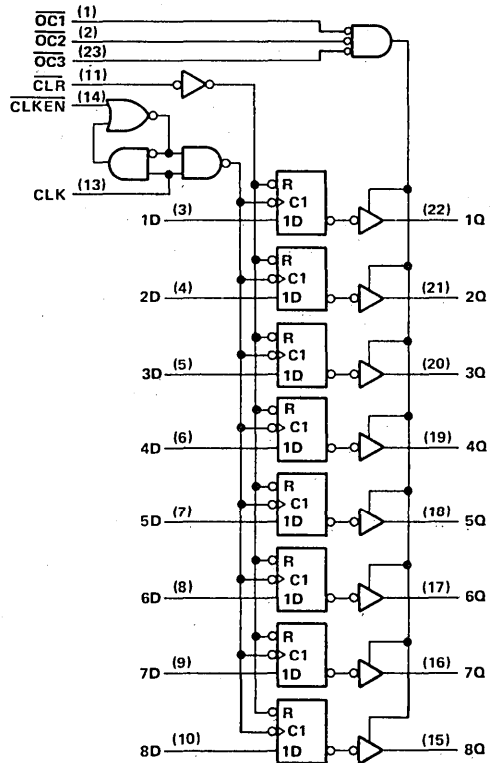
$\overline{\text{OC}}^* = \text{L}$ if all of $\overline{\text{OC}}1$, $\overline{\text{OC}}2$, and $\overline{\text{OC}}3$ are low.

'ALS29825 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12
Pin numbers shown are for DW, JT, and NT packages.

'ALS29825 logic diagram (positive logic)



Pin numbers are for DW, JT, and NT packages.

**SN54ALS29825, SN54ALS29826
SN74ALS29825, SN74ALS29826**
8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

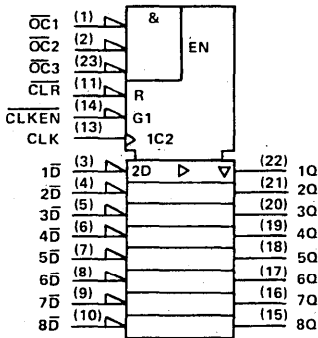
***ALS29826 FUNCTION TABLE**

INPUTS					OUTPUT
\overline{OC}^*	CLR	CLKEN	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	Q_0
H	X	X	X	X	Z

$\overline{OC}^* = H$ if any of $\overline{OC}1$, $\overline{OC}2$, or $\overline{OC}3$ is high.

$\overline{OC}^* = L$ if all of $\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$ are low.

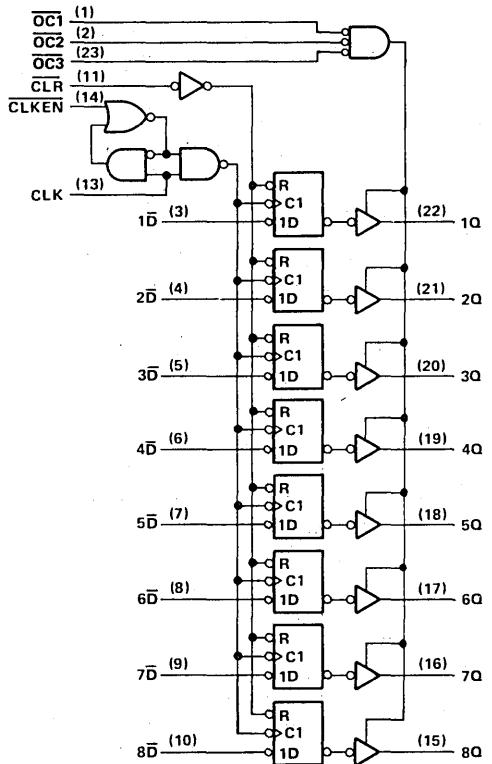
***ALS29826 logic symbol†**



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers are for DW, JT, and NT packages.

***ALS29826 logic diagram (positive logic)**



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Input current	100 mA
Output current	-30 mA to 5 mA
Operating free-air temperature range:	
SN54ALS29825, SN54ALS29826	-55°C to 125°C
SN74ALS29825, SN74ALS29826	0°C to 70°C
Storage temperature range	-65 to 150°C

2
LSI Devices

SN54ALS29825, SN54ALS29826
SN74ALS29825, SN74ALS29826
8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

recommended operating conditions

		SN54ALS29825			SN74ALS29825			UNIT
		SN54ALS29826			SN74ALS29826			
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage				0.8			V
I _{OH}	High-level output current				-15			mA
I _{OL}	Low-level output current				32			mA
t _w	Pulse duration	CLR low						ns
		CLK high						
		CLK low						
t _{su}	Setup time before CLK†	CLR inactive						ns
		Data						
		CLKEN high or low						
t _h	Hold time, data after CLK†	Data						ns
		CLKEN						
T _A	Operating free-air temperature	-55		125		0 70		°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

LSI Devices

PARAMETER		TEST CONDITIONS†		SN54ALS29825		SN74ALS29825		UNIT
				MIN	TYP‡	MAX	MIN	
V _{IK}		V _{CC} = MIN.	I _I = -18 mA	-1.2		-1.2		V
V _{OH}		V _{CC} = MIN to MAX,	I _{OH} = -0.4 mA	V _{CC} - 2		V _{CC} - 2		V
		V _{CC} = MIN,	I _{OH} = -15 mA	2.4	3.3			
		V _{CC} = MIN,	I _{OH} = -24 mA			2.4	3.2	
V _{OL}		V _{CC} = MIN,	I _{OL} = 32 mA	0.25	0.4	0.25	0.4	V
		V _{CC} = MIN,	I _{OL} = 48 mA			0.35	0.5	
I _{OZH}		V _{CC} = MAX,	V _O = 2.4 V	20		20		μA
I _{OZL}		V _{CC} = MAX,	V _O = 0.4 V	-20		-20		μA
I _I		V _{CC} = MAX,	V _I = 5.5 V	0.1		0.1		mA
I _{IH}		V _{CC} = MAX,	V _I = 2.7 V	20		20		μA
I _{IL}		V _{CC} = MAX,	V _I = 0.4 V	-0.1		-0.1		mA
I _{OS} §		V _{CC} = MAX,	V _O = 0	-75	-250	-75	-250	mA
I _{CC}	'ALS29825	V _{CC} = MAX	Outputs high					mA
			Outputs low					
	Outputs disabled		48		48			
	Outputs high							
	Outputs low							
	'ALS29826		Outputs disabled	48		48		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Additional information on these products can be obtained from the factory as it becomes available.

SN54ALS29825, SN54ALS29826
SN74ALS29825, SN74ALS29826
8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	V _{CC} = 5 V, T _A = 25°C		V _{CC} = MIN TO MAX, [†] T _A = MIN TO MAX [†]				UNIT
				'ALS29825 'ALS29826		SN54ALS29825 SN54ALS29826		SN74ALS29825 SN74ALS29826		
				MIN	TYP	MAX	MIN	MAX	MIN	
t _{PLH}	CLK	Any Q	C _L = 300 pF							ns
t _{PHL}										
t _{PLH}					6					
t _{PHL}					7					
t _{PHL}	CLR	Any Q	C _L = 50 pF		13					ns
t _{PZH}	\overline{OC}	Any Q	C _L = 300 pF							ns
t _{PZL}										
t _{PZH}					12					
t _{PZL}					11					
t _{PHZ}	\overline{OC}	Any Q	C _L = 50 pF							ns
t _{PLZ}										
t _{PHZ}					5					
t _{PLZ}					6					

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

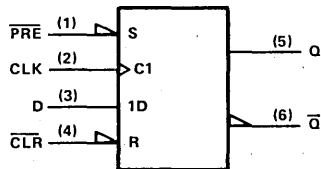
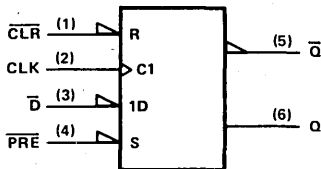
Additional information on these products can be obtained from the factory as it becomes available.

D flip-flop signal conventions

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called \overline{Q} . An input that causes a Q output to go high or a \overline{Q} output to go low is called Preset; an input that causes a \overline{Q} output to go high or a Q output to go low is called Clear. Bars are used over these pin names (\overline{PRE} and \overline{CLR}) if they are active-low.

The devices on this data sheet are second-source designs and the pin-name convention used by the original manufacturer has been retained. That makes it necessary to designate the inputs and outputs of the inverting circuit \overline{D} and Q. In some applications it may be advantageous to redesignate the inputs and outputs as D and \overline{Q} . In that case, outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.

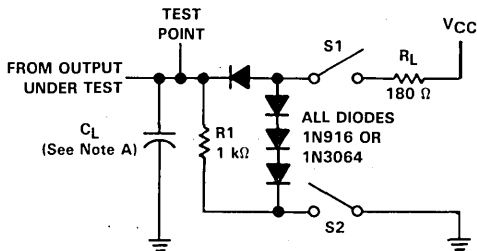
Notice that Q and \overline{Q} exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (∇) on \overline{PRE} and \overline{CLR} remain since these inputs are still active-low, but that the presence or absence of the polarity changes at \overline{D} , Q, and \overline{Q} . Of course pins 5 (Q) is still in phase with the data input D, but now both are considered active high.



2
LSI Devices

SN54ALS29825, SN54ALS29826
SN74ALS29825, SN74ALS29826
8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

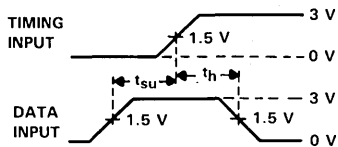
PARAMETER MEASUREMENT INFORMATION



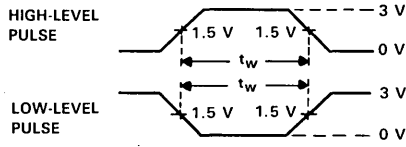
SWITCH POSITION TABLE

TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

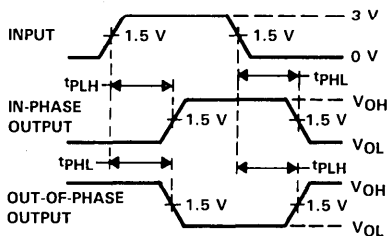
LOAD CIRCUIT



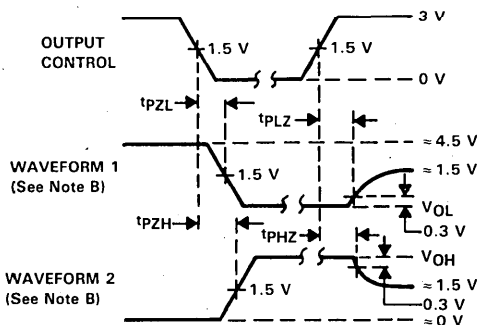
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATIONS**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS**

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

FIGURE 1

- Functionally Equivalent to AM29827 and AM29828
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Data Flow-Thru Pinout (All Inputs on Opposite Side from Outputs)
- Power-Up High-Impedance State
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

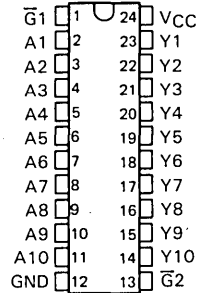
These 10-bit buffers and bus drivers provide high-performance bus interface for wide data paths or busses carrying parity.

The three-state control gate is a 2-input NOR such that if either $\overline{G1}$ or $\overline{G2}$ is high, all ten outputs are in the high-impedance state.

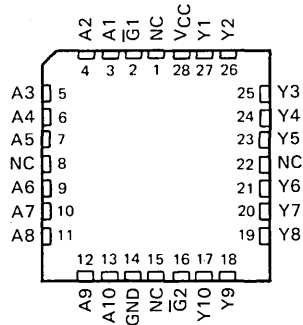
The 'ALS29827 provides true data and the 'ALS29828 provides inverted data at the outputs.

The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74' family is characterized for operation from 0°C to 70°C .

SN54ALS' . . . JT PACKAGE
SN74ALS' . . . DW OR NT PACKAGE
(TOP VIEW)



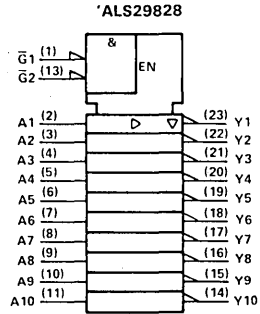
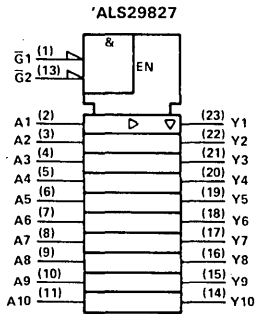
SN54ALS' . . . FK PACKAGE
SN74ALS' . . . FN PACKAGE
(TOP VIEW)



LSI Devices

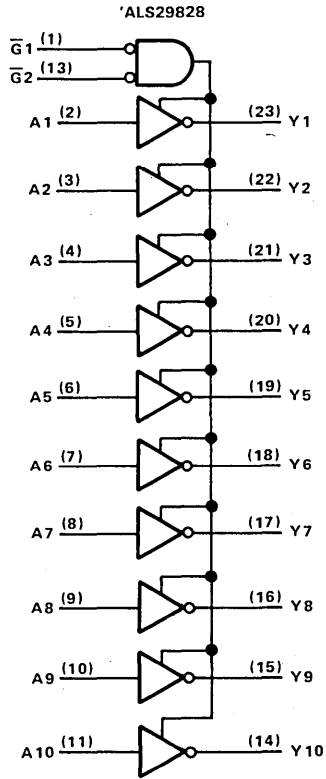
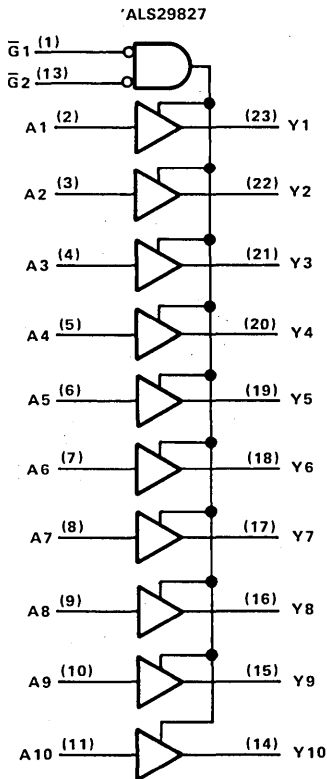
**SN54ALS29827, SN54ALS29828
SN74ALS29827, SN74ALS29828
10-BIT BUFFERS AND BUS DRIVERS WITH 3-STATE OUTPUTS**

logic symbols †



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



Pin numbers shown are DW, JT, and NT packages.

2

LSI Devices

SN54ALS29827, SN54ALS29828 SN74ALS29827, SN74ALS29828

10-BIT BUFFERS AND BUS DRIVERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	5.5 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range: SN54ALS29827, SN54ALS29828	-55°C to 125°C
SN74ALS29827, SN74ALS29828	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54ALS29827 SN54ALS29828			SN74ALS29827 SN74ALS29828			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage				0.8			V
I_{OH}	High-level output current				-15			-24 mA
I_{OL}	Low-level output current				32			48 mA
T_A	Operating free-air temperature	-55			125			0 70 °C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54ALS29827 SN54ALS29828			SN74ALS29827 SN74ALS29828			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$	-1.2			-1.2			V
V_{OH}	$V_{CC} = \text{MIN to MAX}, I_{OH} = -0.4 \text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = \text{MIN}, I_{OH} = -15 \text{ mA}$	2						
	$V_{CC} = \text{MIN}, I_{OH} = -24 \text{ mA}$				2			
V_{OL}	$V_{CC} = \text{MIN}, I_{OL} = 32 \text{ mA}$	0.25 0.4			0.25 0.4			V
	$V_{CC} = \text{MIN}, I_{OL} = 48 \text{ mA}$				0.35 0.5			
I_{OZH}	$V_{CC} = \text{MAX}, V_O = 2.4 \text{ V}$	20			20			μA
I_{OZL}	$V_{CC} = \text{MAX}, V_O = 0.4 \text{ V}$	-20			-20			μA
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$	0.1			0.1			mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$	20			20			μA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$	-0.1			-0.1			mA
I_{OS}^{\S}	$V_{CC} = \text{MAX}, V_O = 0$	-75 -250			-75 -250			mA
I_{CC}	'ALS29827	$V_{CC} = \text{MAX}$	Outputs high	16		16		mA
			Outputs low	20		20		
			Outputs disabled	19		19		
	'ALS29828	$V_{CC} = \text{MAX}$	Outputs high	12		12		mA
			Outputs low	16		16		
			Outputs disabled	14		14		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Additional information on these products can be obtained from the factory as it becomes available.

2

LSI Devices



SN54ALS29827, SN54ALS29828
SN74ALS29827, SN74ALS29828
10-BIT BUFFERS AND BUS DRIVERS WITH 3-STATE OUTPUTS

switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	V _{CC} = 5 V, T _A = 25°C			V _{CC} = MIN TO MAX, [†] T _A = MIN TO MAX [†]				UNIT
				'ALS29827 'ALS29828			SN54ALS29827 SN54ALS29828		SN74ALS29827 SN74ALS29828		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	C _L = 300 pF	8						ns	
t _{PHL}				11							
t _{PLH}			C _L = 50 pF	5							
t _{PHL}				5							
t _{PZH}	\bar{G}	Y	C _L = 300 pF	11					ns		
t _{PZL}				18							
t _{PZH}			C _L = 50 pF	7							
t _{PZL}				10							
t _{PHZ}	\bar{G}	Y	C _L = 50 pF	11					ns		
t _{PLZ}				5							
t _{PHZ}			C _L = 5 pF	4							
t _{PLZ}				4							

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

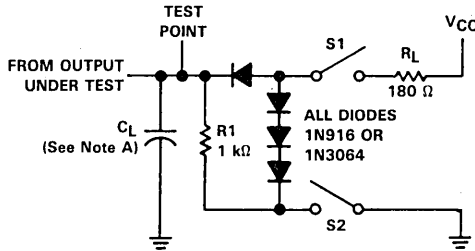
Additional information on these products can be obtained from the factory as it becomes available.

2

LSI Devices

SN54ALS29827, SN54ALS29828
SN74ALS29827, SN74ALS29828
10-BIT BUFFERS AND BUS DRIVERS WITH 3-STATE OUTPUTS

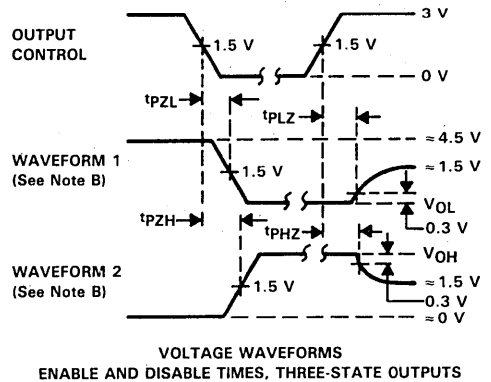
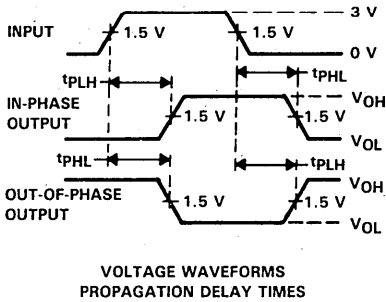
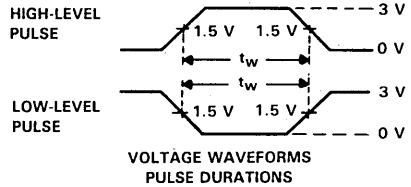
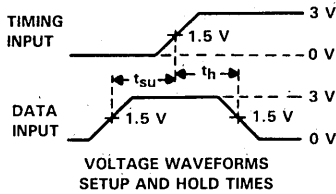
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

SWITCH POSITION TABLE

TEST	S1	S2
t _{PLH}	Closed	Closed
t _{PHL}	Closed	Closed
t _{PZH}	Open	Closed
t _{PZL}	Closed	Open
t _{PHZ}	Closed	Closed
t _{PLZ}	Closed	Closed



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_0 = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

FIGURE 1

- Functionally Equivalent to AM29861 and AM29862
- Choice of True or Inverting Logic
- Power-Up High-Impedance State
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 10-bit bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}BA$ and $\overline{G}AB$).

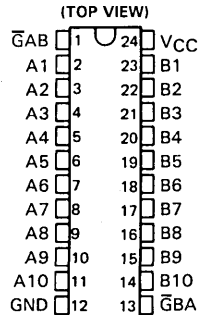
The enable inputs can be used to disable the device so that the buses are effectively isolated.

The SN54' family is characterized for operation over the full military temperature range of $-55^{\circ}C$ to $125^{\circ}C$. The SN74' family is characterized for operation from $0^{\circ}C$ to $70^{\circ}C$.

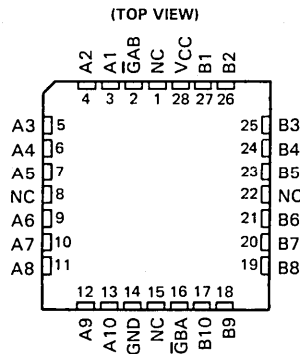
FUNCTION TABLE

INPUTS		OPERATION	
$\overline{G}AB$	$\overline{G}BA$	ALS29861	ALS29862
L	H	A to B	\overline{A} to B
H	L	B to A	\overline{B} to A
H	H	Isolation	Isolation
L	L	Latch A and B ($\overline{A} = B$)	Latch A and B ($\overline{A} = \overline{B}$)

SN54ALS' ... JT PACKAGE
SN74ALS' ... DW OR NT PACKAGE



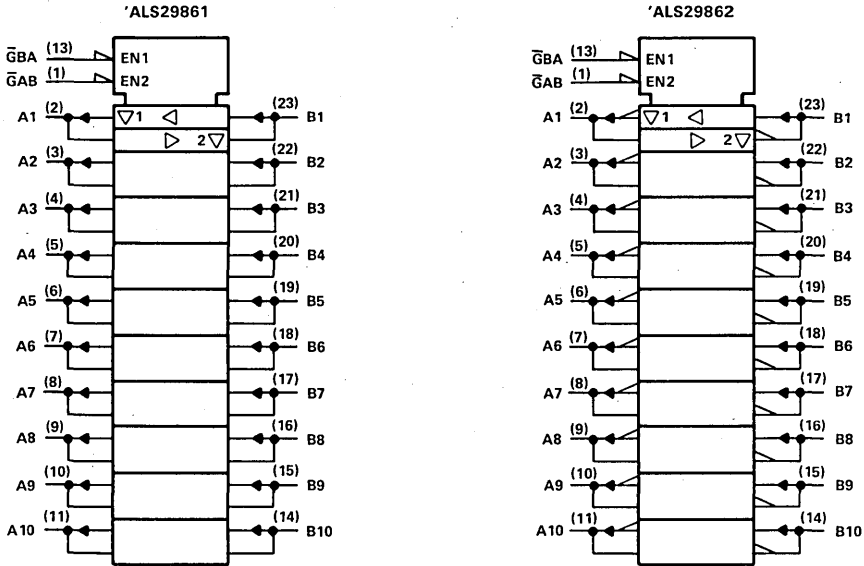
SN54ALS' ... FK PACKAGE
SN74ALS' ... FN PACKAGE



NC—No internal connection

**SN54ALS29861, SN54ALS29862
SN74ALS29861, SN74ALS29862
10-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS**

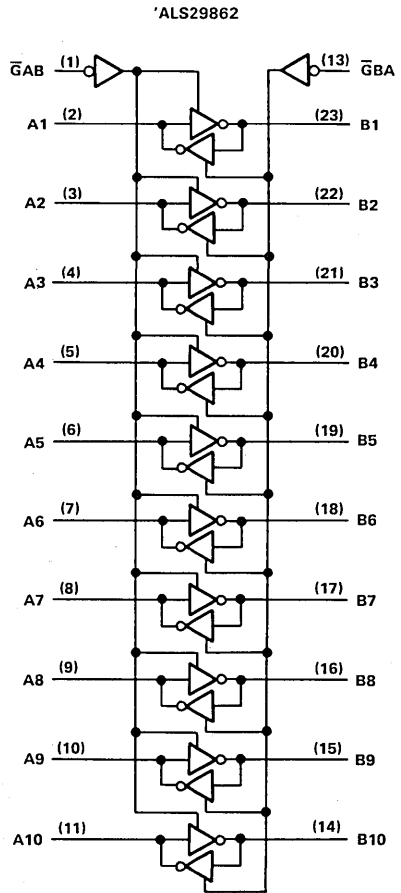
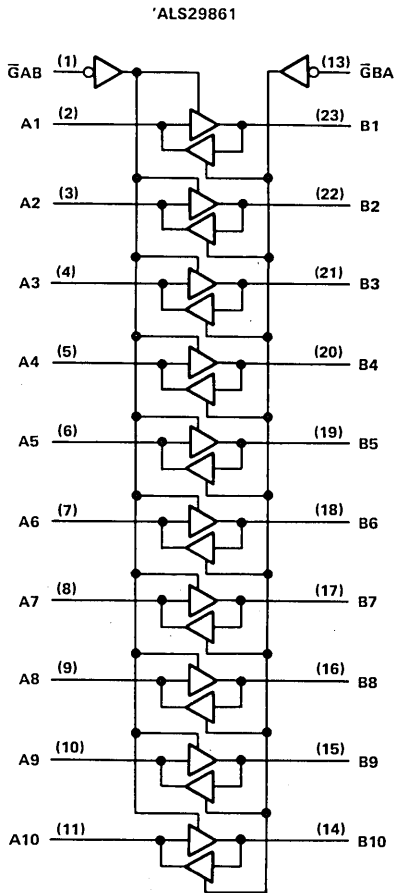
logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.

**SN54ALS29861, SN54ALS29862
SN74ALS29861, SN74ALS29862
10-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS**

logic diagrams



Pin numbers shown are for DW, JT, and NT packages.

SN54ALS29861, SN54ALS29862
SN74ALS29861, SN74ALS29862
10-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage: All inputs and I/O ports	5.5 V
Operating free-air temperature range: SN54ALS29861, SN54ALS29862	-55°C to 125°C
SN74ALS29861, SN74ALS29862	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

	SN54ALS29861			SN74ALS29861			UNIT
	SN54ALS29862			SN74ALS29862			
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			-15			-24	mA
I_{OL} Low-level output current			32			48	mA
T_A Operating free-air temperature	-55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

LSI Devices

PARAMETER	TEST CONDITIONS [†]		SN54ALS29861		SN74ALS29861		UNIT
			SN54ALS29862		SN74ALS29862		
			MIN	TYP [‡]	MAX	MIN	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$		-1.2		-1.2		V
V_{OH}	$V_{CC} = \text{MIN to MAX}, I_{OH} = -0.4 \text{ mA}$		$V_{CC} - 2$		$V_{CC} - 2$		V
	$V_{CC} = \text{MIN}, I_{OH} = -15 \text{ mA}$		2				
	$V_{CC} = \text{MIN}, I_{OH} = -24 \text{ mA}$				2		
V_{OL}	$V_{CC} = \text{MIN}, I_{OL} = 32 \text{ mA}$		0.25	0.4	0.25	0.4	V
	$V_{CC} = \text{MIN}, I_{OL} = 48 \text{ mA}$				0.35	0.5	
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$						mA
I_{IH}	Control inputs	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$	20		20		μA
	A or B ports [§]		20		20		
I_{IL}	Control inputs	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$	-0.1		-0.1		mA
	A or B ports [§]		-0.1		-0.1		
I_{OS} [¶]	$V_{CC} = \text{MAX}, V_O = 0$		-75	-250	-75	-250	mA
I_{CC}	'ALS29861	$V_{CC} = \text{MAX}$	Outputs high		28		mA
			Outputs low		38		
	Outputs disabled		36				
	'ALS29862		Outputs high		22		
			Outputs low		30		
	Outputs disabled		28		28		

[†] For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

[§] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[¶] Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

**SN54ALS29861, SN54ALS29862
SN74ALS29861, SN74ALS29862
10-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS**

***ALS29861 switching characteristics**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	V _{CC} = 5 V, T _A = 25°C			V _{CC} = MIN TO MAX, [†] T _A = MIN TO MAX [†]				UNIT
				*ALS29861			SN54ALS29861		SN74ALS29861		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	C _L = 300 pF	8						ns	
t _{PHL}				11							
t _{PLH}			5								
t _{PHL}			5								
t _{PZH}	A or B	A or B	C _L = 300 pF	11						ns	
t _{PZL}				17							
t _{PZH}			7								
t _{PZL}			10								
t _{PHZ}	A or B	A or B	C _L = 50 pF	11						ns	
t _{PLZ}				5							
t _{PHZ}			4								
t _{PLZ}			4								

***ALS29862 switching characteristics**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	V _{CC} = 5 V, T _A = 25°C			V _{CC} = MIN TO MAX, [†] T _A = MIN TO MAX [†]				UNIT
				*ALS29862			SN54ALS29862		SN74ALS29862		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	C _L = 300 pF	7						ns	
t _{PHL}				11							
t _{PLH}			4								
t _{PHL}			5								
t _{PZH}	A or B	A or B	C _L = 300 pF	11						ns	
t _{PZL}				17							
t _{PZH}			7								
t _{PZL}			10								
t _{PHZ}	A or B	A or B	C _L = 50 pF	11						ns	
t _{PLZ}				5							
t _{PHZ}			4								
t _{PLZ}			4								

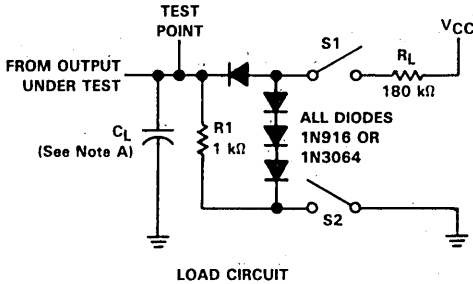
[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

Additional information on these products can be obtained from the factory as it becomes available.

2
LSI Devices

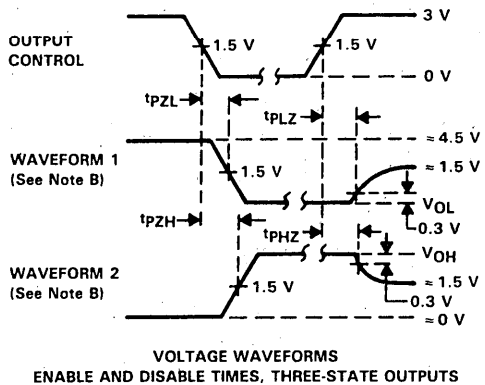
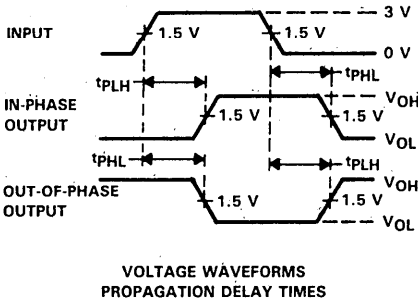
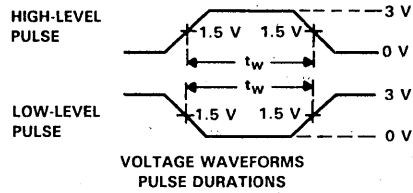
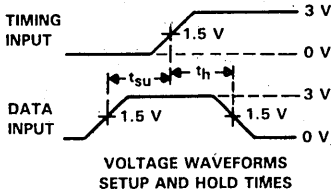
**SN54ALS29861, SN54ALS29862
SN74ALS29861, SN74ALS29862
10-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS**

PARAMETER MEASUREMENT INFORMATION



SWITCH POSITION TABLE

TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

FIGURE 1

- Functionally Equivalent to AM29863 and AM29864
- Choice of True or Inverting Logic
- Power-Up High-Impedance State
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

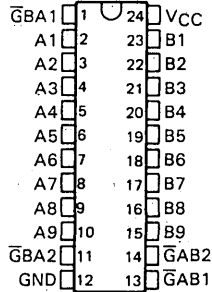
description

These 9-bit bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

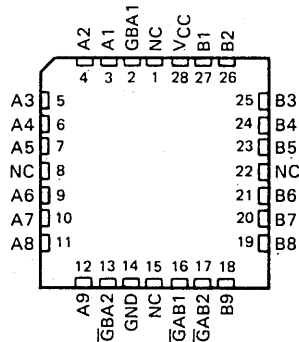
These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}BA1$, $\overline{G}BA2$, $\overline{G}AB1$, and $\overline{G}AB2$).

The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74' family is characterized for operation from 0°C to 70°C .

SN54ALS'... JT PACKAGE
SN74ALS'... DW OR NT PACKAGE
(TOP VIEW)



SN54ALS'... FK PACKAGE
SN74ALS'... FN PACKAGE
(TOP VIEW)



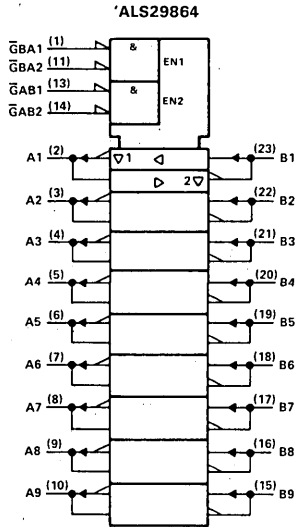
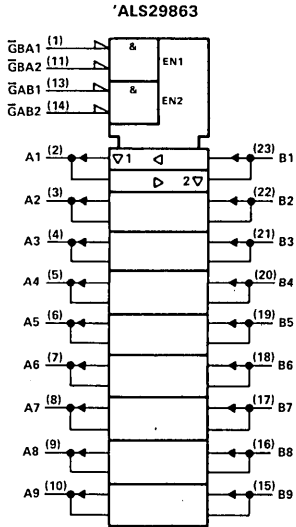
NC—No internal connection

FUNCTION TABLE

ENABLE INPUTS				OPERATION	
$\overline{G}AB1$	$\overline{G}AB2$	$\overline{G}BA1$	$\overline{G}BA2$	'ALS29863	'ALS29864
L	L	L	L	Latch A and B	Latch A and B
L	L	H	X	A to B	A to \overline{B}
L	L	X	H	B to A	B to \overline{A}
H	X	L	L	Isolation	Isolation
X	H	L	L		
H	X	X	H		
X	H	X	H		
X	H	H	X		

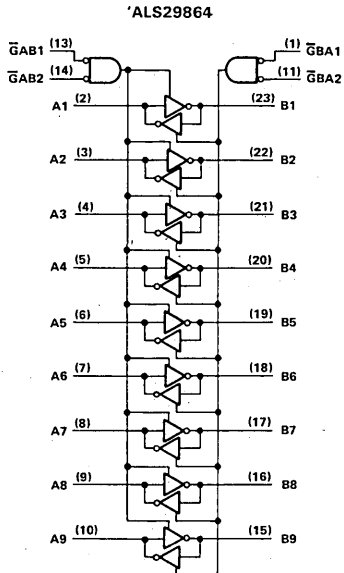
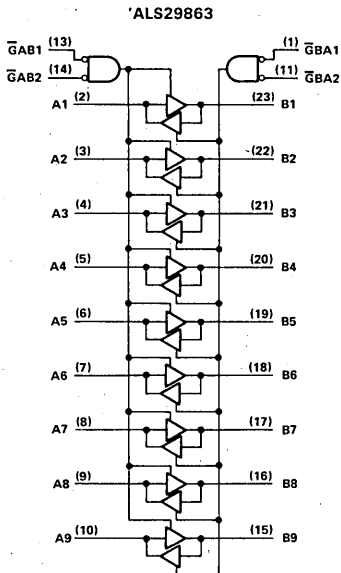
SN54ALS29863, SN54ALS29864
SN74ALS29863, SN74ALS29864
9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

logic symbols †



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams



Pin numbers shown are for DW, JT, and NT packages.

2

LSI Devices

SN54ALS29863, SN54ALS29864
SN74ALS29863, SN74ALS29864
9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage: All inputs and I/O ports	5.5 V
Operating free-air temperature range: SN54ALS29863, SN54ALS29864	-55°C to 125°C
SN74ALS29863, SN74ALS29864	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

	SN54ALS29863 SN54ALS29864			SN74ALS29863 SN74ALS29864			UNIT	
	MIN	NOM	MAX	MIN	NOM	MAX		
V_{CC} Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
V_{IH} High-level input voltage	2			2			V	
V_{IL} Low-level input voltage	0.8			0.8			V	
I_{OH} High-level output current	-15			-24			mA	
I_{OL} Low-level output current	32			48			mA	
T_A Operating free-air temperature	-55			0			70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54ALS29863 SN54ALS29864		SN74ALS29863 SN74ALS29864		UNIT
		MIN	TYP [‡]	MAX	MIN	
V_{IK}	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$	-1.2		-1.2		V
V_{OH}	$V_{CC} = \text{MIN to MAX}$, $I_{OH} = -0.4 \text{ mA}$	$V_{CC}-2$		$V_{CC}-2$		V
	$V_{CC} = \text{MIN}$, $I_{OH} = -15 \text{ mA}$	2		2		
V_{OL}	$V_{CC} = \text{MIN}$, $I_{OH} = -24 \text{ mA}$	2		2		V
	$V_{CC} = \text{MIN}$, $I_{OH} = -32 \text{ mA}$	0.25	0.4	0.25	0.4	
I_I	$V_{CC} = \text{MIN}$, $I_{OL} = 48 \text{ mA}$			0.35	0.5	mA
	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$					
I_{IH}	Control inputs	20		20		μA
	A or B ports [§]	20		20		
I_{IL}	Control inputs	-0.1		-0.1		mA
	A or B ports [§]	-0.1		-0.1		
I_{OS} [¶]	$V_{CC} = \text{MAX}$, $V_O = 0$	-75	-250	-75	-250	mA
I_{CC}	'ALS29863	$V_{CC} = \text{MAX}$	Outputs high	26	26	mA
			Outputs low	35	35	
			Outputs disabled	34	34	
			Outputs high	20	20	
			Outputs low	27	27	
'ALS29864	$V_{CC} = \text{MAX}$	Outputs high	26	26	mA	
		Outputs low	27	27		
		Outputs disabled	26	26		

[†] For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

[§] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[¶] Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

2
LSI Devices

**SN54ALS29863, SN54ALS29864
SN74ALS29863, SN74ALS29864
9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS**

†ALS29863 switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	$V_{CC} = 5 V,$ $T_A = 25^{\circ}C$			$V_{CC} = \text{MIN TO MAX,}^{\dagger}$ $T_A = \text{MIN TO MAX}^{\dagger}$			UNIT	
				†ALS29863			SN54ALS29863		SN74ALS29863		
				MIN	TYP	MAX	MIN	MAX	MIN		MAX
t_{PLH}	A or B	B or A	$C_L = 300 \text{ pF}$	8					ns		
t_{PHL}				11							
t_{PLH}			5								
t_{PHL}			5								
t_{PZH}	$\overline{G}AB$ or $\overline{G}BA$	A or B	$C_L = 300 \text{ pF}$	11					ns		
t_{PZL}				17							
t_{PZH}			7								
t_{PZL}			10								
t_{PHZ}	$\overline{G}AB$ or $\overline{G}BA$	A or B	$C_L = 50 \text{ pF}$	11					ns		
t_{PLZ}				5							
t_{PHZ}			4								
t_{PLZ}			4								

†ALS29864 switching characteristics

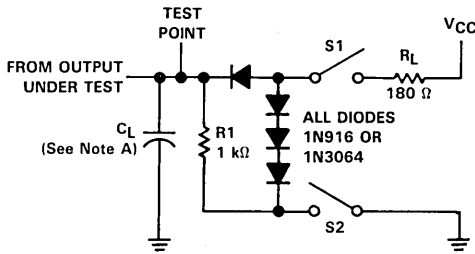
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	$V_{CC} = 5 V,$ $T_A = 25^{\circ}C$			$V_{CC} = \text{MIN TO MAX,}^{\dagger}$ $T_A = \text{MIN TO MAX}^{\dagger}$			UNIT	
				†ALS29864			SN54ALS29864		SN74ALS29864		
				MIN	TYP	MAX	MIN	MAX	MIN		MAX
t_{PLH}	A or B	B or A	$C_L = 300 \text{ pF}$	7					ns		
t_{PHL}				11							
t_{PLH}			4								
t_{PHL}			5								
t_{PZH}	$\overline{G}AB$ or $\overline{G}BA$	A or B	$C_L = 300 \text{ pF}$	11					ns		
t_{PZL}				17							
t_{PZH}			7								
t_{PZL}			10								
t_{PHZ}	$\overline{G}AB$ or $\overline{G}BA$	A or B	$C_L = 50 \text{ pF}$	11					ns		
t_{PLZ}				5							
t_{PHZ}			4								
t_{PLZ}			4								

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

Additional information on these products can be obtained from the factory as it becomes available.

**SN54ALS29863, SN54ALS29864
SN74ALS29863, SN74ALS29864
9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS**

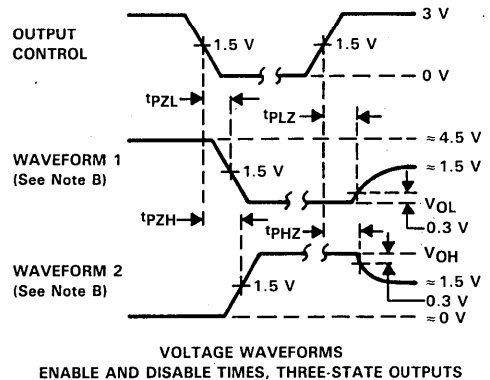
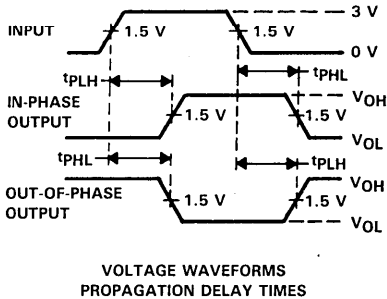
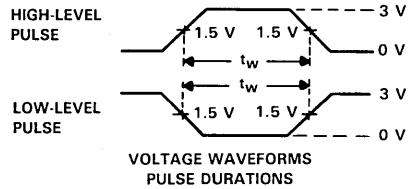
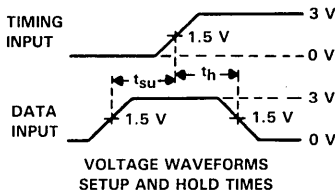
PARAMETER MEASUREMENT INFORMATION



SWITCH POSITION TABLE

TEST	S1	S2
t _{PLH}	Closed	Closed
t _{PHL}	Closed	Closed
t _{PZH}	Open	Closed
t _{PZL}	Closed	Open
t _{PHZ}	Closed	Closed
t _{PLZ}	Closed	Closed

LOAD CIRCUIT



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_o = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

FIGURE 1

2
LSI Devices

2

LSI Devices

THCT1010-160M, THCT1010-140E, THCT1010-100 16-BIT BY 16-BIT MULTIPLIERS/ACCUMULATORS

independently controlled by CLK X and CLK Y, and the product registers are D-type positive-edge-triggered flip-flops. Separate three-state output enables are provided for each output product register. These, in combination with the independent input clocks, allow operation on a microprocessor bus.

The THCT1010 has a round control (RND) that rounds the product to the 19 most significant bits. The preload control (PREL) is used in conjunction with the output enables to initialize the contents of the output registers. The THCT1010 will perform multiplication and addition, multiplication and subtraction, or straight multiplication depending upon the states of the accumulate control (ACC) and subtractor control (SUB). The TC control provides the capability of formatting the input data to be either two's complement or unsigned magnitude.

The THCT1010-160M is characterized for operation over the full military temperature range of -55°C to 125°C . The THCT1010-140E is characterized for operation from -40°C to 85°C . The THCT1010-100 is characterized for operation from 0°C to 70°C .

2

LSI Devices

THCT1010-160M, THCT1010-140E, THCT1010-100 16-BIT BY 16-BIT MULTIPLIERS/ACCUMULATORS

NO.	PIN NAME	DESCRIPTION
56-64, 1-7	X15 thru X0	X data inputs, X15 is the most-significant bit. The data is loaded into the X register on the rising edge of CLKX.
8-15, 17-24	Y0/PRO thru Y15/PR15	I/O ports for least significant product (LSP) bits of output product register, input ports for Y data. Y0/PRO is the least significant bit. The mode is controlled by the PREL and OEMS pins.
25-43	PR16 thru PR34	I/O ports for output product register bits. PR16 through PR31 are the most-significant product (MSP) bits. PR32 through PR34 are the extended product (XTP) bits. The mode is controlled by PREL, OELS, OEX.
44	CLK PR	Product clock input. On the low-to-high transition, latches the LSP, MSP, and XTP into the output product register.
45	OEMS	Active-low output enable for MSP output product register. When high, causes the PR31 through PR16 outputs to be in the high-impedance state.
46	PREL	Preload control. When high, the output product register's outputs are disabled. When an output enable (OELS, OEMS, OEX) is high, preload data can be entered into the output product register from the PR I/O lines on the rising edge of CLK PR.
47	OEX	Active-low output enable for XTP output product register. When high, causes the PR32 through PR34 outputs to be in the high-impedance state.
48	TC	Two's complement control. When TC is high, the input data is in two's complement format. When TC is low, the input data is in unsigned magnitude format. The TC signal is loaded into the control register on the rising edge of CLK X or CLK Y.
50	CLK Y	Y clock input. On the low-to-high transition, clocks data in from the Y inputs.
51	CLK X	X clock input. On the low-to-high transition, clocks data in from the X inputs.
52	ACC	Accumulator control. When ACC is high and SUB is low, the content of the output product register is added to the next product generated. The sum is then placed in the output product register on the rising edge of CLK PR. When ACC is low, the product is stored directly into the output register on the rising edge of CLK PR. The ACC signal is loaded into the control register at the rising edge of CLK X or CLK Y.
53	SUB	Subtraction control. When SUB and ACC are high, the content of the output product register is subtracted from the next product generated. The result is then placed in the output product register on the rising edge of CLK PR. When SUB is low and ACC is high, the addition operation is performed instead of subtraction. When ACC is low, SUB is a "Don't Care". The SUB signal is loaded into the control register on the rising edge of CLK X or CLK Y.
54	RND	Round control. When high, causes the product of the X and Y inputs to be rounded to the 19 most significant bits by adding a 1 to the MSB of the LSP. The RND signal is loaded into the control register on the rising edge of CLK X or CLK Y.
55	OELS	Active-low output enable for LSP output product register. When high, causes the PRO through PR15 outputs to be in the high-impedance state.

Pin numbers shown are for the JD and N packages.

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LSI Devices

THCT1010-160M, THCT1010-140E, THCT1010-100
16-BIT BY 16-BIT MULTIPLIERS/ACCUMULATORS

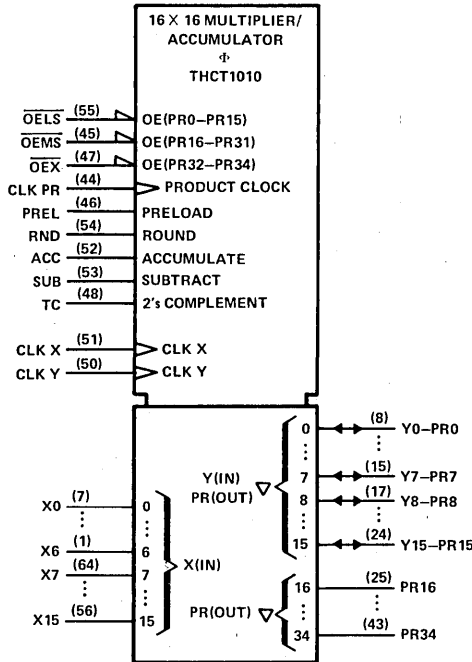
PRELOAD FUNCTION TABLE

PREL	OEX	OEMS	OELS	XTP	MSP	LSP
L	L	L	L	(PR32-PR34)	(PR16-PR31)	(PRO-PR15)
L	L	L	H	(PR32-PR34)	(PR16-PR31)	Z
L	L	H	L	(PR32-PR34)	Z	(PRO-PR15)
L	L	H	H	(PR32-PR34)	Z	Z
L	H	L	L	Z	(PR16-PR31)	(PRO-PR15)
L	H	L	H	Z	(PR16-PR31)	Z
L	H	H	L	Z	Z	(PRO-PR15)
L	H	H	H	Z	Z	Z
H	L	L	L	Z	Z	Z
H	L	L	H	Z	Z	PL
H	L	H	L	Z	PL	Z
H	L	H	H	Z	PL	PL
H	H	L	L	PL	Z	Z
H	H	L	H	PL	Z	PL
H	H	H	L	PL	PL	Z
H	H	H	H	PL	PL	PL

PL = Output buffers at high impedance or output disabled. Preload data supplied externally at output pins will be loaded into the output register on the rising edge of CLK PR.

2

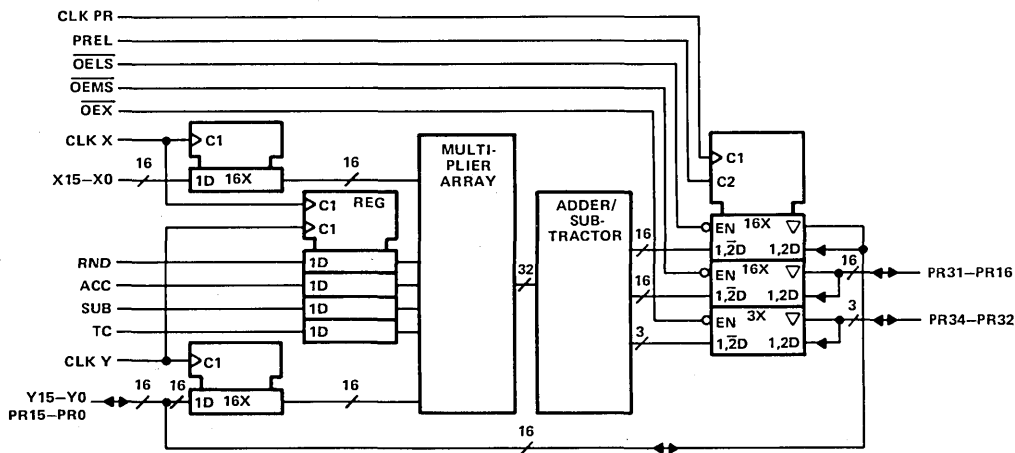
logic symbol



Pin numbers shown are for the JD and N packages.

THCT1010-160M, THCT1010-140E, THCT1010-100 16-BIT BY 16-BIT MULTIPLIERS/ACCUMULATORS

logic diagram (positive logic)



Pin numbers shown are for the JD and N packages.

absolute maximum ratings over operating free-air temperature†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input diode current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output diode current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND pins	± 50 mA
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	300°C
Storage temperature range	-65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			THCT1010-160M			THCT1010-140E			THCT1010-100			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2			2			2			V
V_{IL}	Low-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	0			0			0			V
V_I	Input voltage		0			0			0			V_{CC}
V_O	Output voltage		0			0			0			V_{CC}
t_t	Input transition (rise and fall) times		0			0			0			500 ns
T_A	Operating free-air temperature		-55			-40			0			70 °C

2
LSI Devices

THCT1010-160M, THCT1010-140E, THCT1010-100 16-BIT BY 16-BIT MULTIPLIERS/ACCUMULATORS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			THCT1010-160M		THCT1010-140E THCT1010-100		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL} , I _{OH} = -20 μA	4.5 V	4.4			4.4		4.4	V	
	V _I = V _{IH} or V _{IL} , I _{OH} = -4 mA	4.5 V	3.86			3.7		3.76		
V _{OL}	V _I = V _{IH} or V _{IL} , I _{OL} = 20 μA	4.5 V		0.1		0.1		0.1	V	
	V _I = V _{IH} or V _{IL} , I _{OL} = 4 mA	4.5 V		0.32		0.4		0.37		
I _I	V _I = 0 to V _{CC}	5.5 V		±5	±100		±1000	±1000	nA	
I _{OZ}	V _O = V _{CC} or 0, V _I = V _{IH} or V _{IL}	5.5 V		±0.01	±0.5		±10	±5	μA	
I _{CC} [†]	V _I = V _{CC} or 0, I _O = 0	5.5 V			0.75		2	1	mA	
C _i		4.5 V							pF	
		to 5.5 V		3	10		10	10		

[†]See Figure 4.

2

LSI Devices

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

THCT1010-160M, THCT1010-140E

	V _{CC}	T _A = 25°C		THCT1010-160M		THCT1010-140E		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w Pulse duration, clocks X and Y high or low	4.5 V	20		30		25		ns
	5.5 V	20		30		25		
t _{su} Setup time, X input before CLK X† or Y input before CLK Y†	4.5 V	10		30		25		ns
	5.5 V	10		30		25		
t _h Hold time, X input after CLK X†	4.5 V	6		12		10		ns
	5.5 V	6		12		10		
t _h Hold time, Y input after CLK Y† or preload data after CLK PR†	4.5 V	1		7		5		ns
	5.5 V	1		7		5		

THCT1010-100

	V _{CC}	T _A = 25°C		THCT1010-100		UNIT
		MIN	MAX	MIN	MAX	
t _w Pulse duration, clocks X and Y high or low	4.75 V	20		25		ns
t _{su} Setup time, X input before CLK X† or Y input before CLK Y†	4.75 V	10		20		ns
t _h Hold time	X input after CLK X†	4.75 V	6	10		ns
	Y input after CLK Y† or preload data after CLK PR†	4.75 V	1	5		ns

THCT1010-160M, THCT1010-140E, THCT1010-100

16-BIT BY 16-BIT MULTIPLIERS/ACCUMULATORS

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), $C_L = 50$ pF (see Figure 3)

THCT1010-160M, THCT1010-140E

PARAMETER	V _{CC}	T _A = 25°C			THCT1010-160M		THCT1010-140E		UNIT
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
t _{pd} Propagation delay time	4.5 V	45			65		55		ns
	5.5 V				60		50		
t _{en} Enable time	4.5 V	35			65		45		ns
	5.5 V				60		40		
t _{dis} Disable time	4.5 V	35			60		45		ns
	5.5 V				55		40		
t _{macc} Multiply/accumulate time	4.5 V	100			160		140		ns
	5.5 V				140		120		

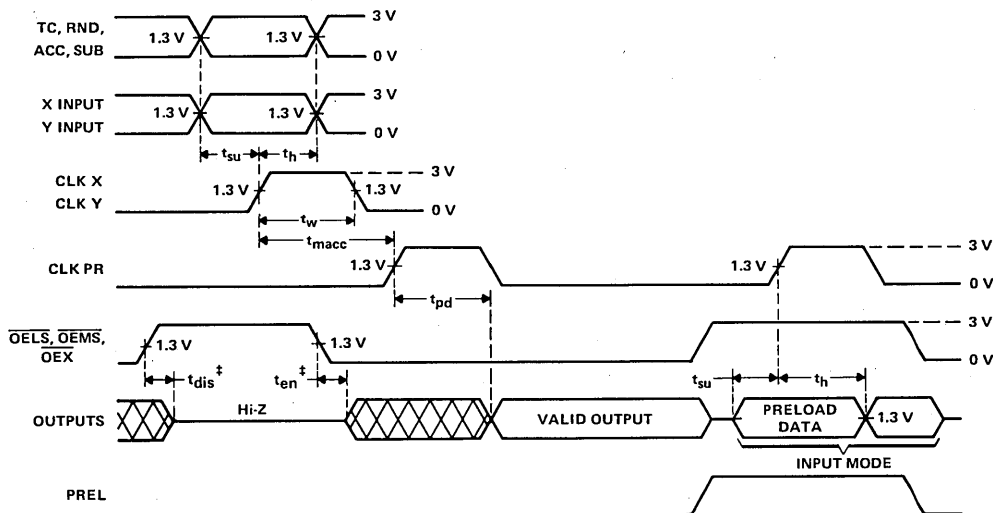
C _{pd} Power dissipation capacitance	No load, T _A = 25°C	750 pF typ
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THCT1010-100

PARAMETER	V _{CC}	T _A = 25°C			THCT1010-100		UNIT
		MIN	TYP†	MAX	MIN	MAX	
t _{pd} Propagation delay time	4.75 V	35			45		ns
t _{en} Enable time	4.75 V	30			40		ns
t _{dis} Disable time	4.75 V	30			40		ns
t _{macc} Multiply/accumulate time	4.75 V	90			100		ns

†Typical values are at V_{CC} = 5 V.

PARAMETER MEASUREMENT INFORMATION



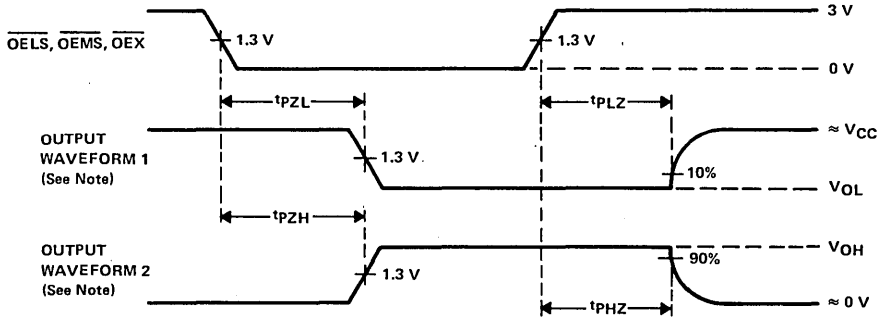
†The measurement points for enable and disable times are as shown in Figure 2.

FIGURE 1. VOLTAGE WAVEFORMS

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LSI Devices

THCT1010-160M, THCT1010-140E, THCT1010-100
16-BIT BY 16-BIT MULTIPLIERS/ACCUMULATORS

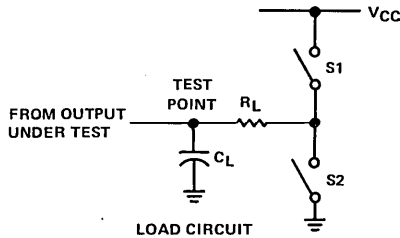
PARAMETER MEASUREMENT INFORMATION



NOTE: Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 2. DETAILED VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES

2
LSI Devices



PARAMETER	RL	CL†	S1	S2
ten	tPZH	1 kΩ	OPEN	CLOSED
	tPZL	50 pF	CLOSED	OPEN
tdis	tPHZ	1 kΩ	OPEN	CLOSED
	tPLZ	50 pF	CLOSED	OPEN
t _{pd} or t _t	—	50 pF	OPEN	OPEN

†CL includes probe and test fixture capacitance

FIGURE 3. LOAD CIRCUITS

TYPICAL CHARACTERISTICS

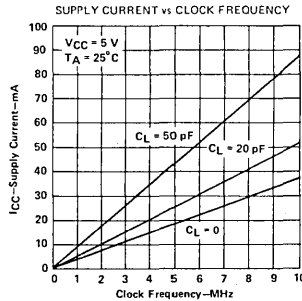


FIGURE 4

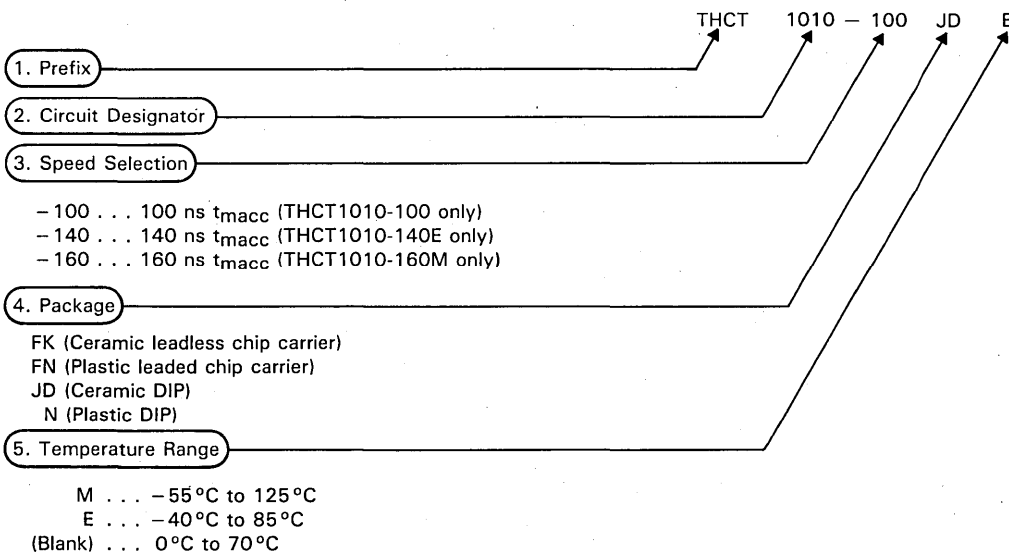
THCT1010-160M, THCT1010-140E, THCT1010-100 16-BIT BY 16-BIT MULTIPLIERS/ACCUMULATORS

THERMAL INFORMATION

THERMAL RESISTANCE

PACKAGE	PINS	JUNCTION-TO-CASE THERMAL RESISTANCE, $R_{\theta JC}$ (°C/W)	JUNCTION-TO-FREE-AIR THERMAL RESISTANCE, $R_{\theta JA}$ (°C/W)
FK	68	8	36
FN	68		
JD	64	9	32
N	64		

ORDERING INSTRUCTIONS



2
LSI Devices

2

LSI Devices

- Inputs are TTL- and CMOS-Voltage Compatible
- Interfaces Mechanical Devices to Data Bus
- Identifies and Measures Forward or Backward Rotation or Direction
- Measures Pulse Duration and Frequency
- Cascadable 16-Bit Up/Down Counter
- 8-Bit Parallel 3-State Bus with Each Output Capable of Driving up to 15 LSTTL Loads
- Dependable Texas Instruments Quality and Reliability

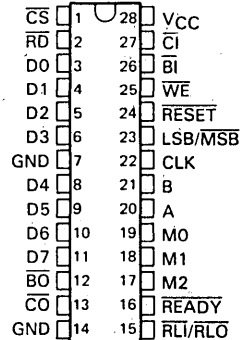
description

The THCT2000 direction discriminator can determine the direction and displacement of a mechanical device based on input signals from two transducers in quadrature. It can also measure a pulse duration using a known clock rate, or a frequency over a known time interval. It includes a 16-bit counter, which can be used separately. Several of these devices may be cascaded to provide accuracy greater than 16-bits.

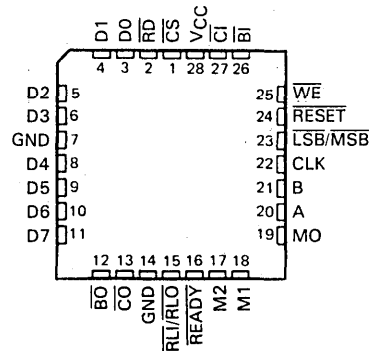
The device may be used in many diverse applications, and is specifically designed for use in many types of microprocessor-based systems. Some of the possibilities include motor controls, robotics, tracker balls (mice), lathe or tooling machines, automobiles, and conveyer belts or other transport mechanisms.

The THCT2000M is characterized for operation over the full military temperature range of -55°C to 125°C. The THCT2000E is characterized for operation from -40°C to 85°C.

THCT2000M . . . JD PACKAGE
THCT2000E . . . JD OR N PACKAGE
(TOP VIEW)

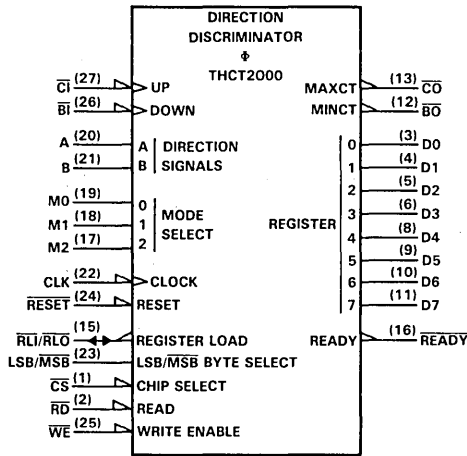


THCT2000M . . . FK PACKAGE
THCT2000E . . . FN PACKAGE
(TOP VIEW)



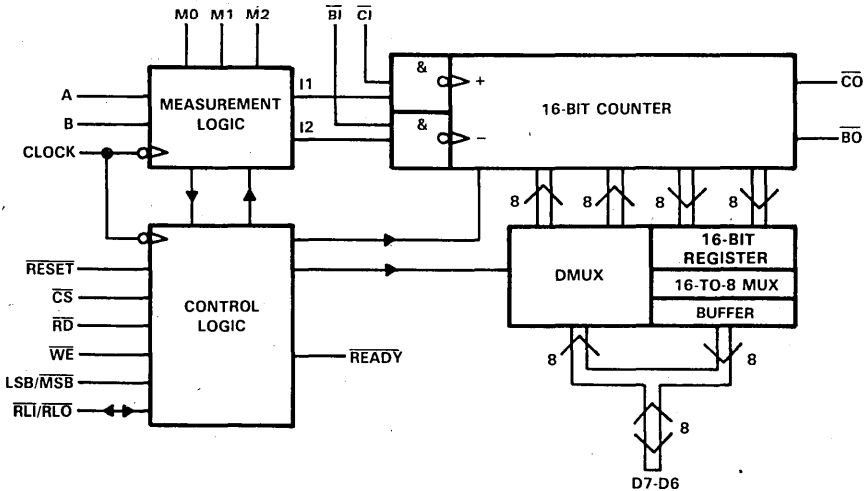
THCT2000M, THCT2000E DIRECTION DISCRIMINATORS

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

functional block diagram



2

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THCT2000M, THCT2000E DIRECTION DISCRIMINATORS

NAME	PIN NUMBER	DESCRIPTION
A, B	20, 21	Signal measurement inputs.
\overline{BI}	26	Cascade input for counting down. In mode 0, \overline{BI} is used as the clock input for counting down. Triggering occurs on the high-to-low transition.
\overline{BO}	12	Counter output underflow signal. Active (low) for a duration equal to the low level of the input clock.
\overline{CI}	27	Cascade input for counting up. In mode 0, \overline{CI} is used as the clock input for counting up. Triggering occurs on the high-to-low transition.
CLK	22	Clock input. Used for internal synchronization and control timing.
\overline{CO}	13	Counter output overflow signal. Active (low) for a duration equal to the low level of the input clock.
\overline{CS}	1	Chip select input. This active-low input is used to enable read and write functions. For additional details, see read and write timing diagrams.
D0-D7	3, 4, 5, 6, 8, 9, 10, 11	Counter load inputs/register output data lines.
GND	7, 14	Pins 7 and 14 are both internally connected to the ground rail of the integrated circuit but both should be connected to the system ground for proper operation.
LSB/MSB	23	Byte select input. During read operations, a high level selects the least significant byte, while a low level selects the most significant byte. For write operations, this input directs the data on the bus into the least significant or most significant byte position of the counter. See write timing diagrams for additional details.
M0, M1, M2	19, 18, 17	Mode select inputs.
\overline{RD}	2	Read input. When active (low) in conjunction with \overline{CS} low, the data stored in the output register will be present on the data bus as selected by the LSB/MSB input. See read timing diagrams for additional details.
READY	16	Ready output. When active (low), this output indicates to the processor that it may complete the read or write operation. \overline{READY} is synchronous with the negative-going edge of CLK. This output requires a pullup resistor (1 k Ω nominal).
RESET	24	Counter and control logic reset. When active (low), the counter is asynchronously reset to zero while the control logic is asynchronously initialized to the proper state as determined by the mode control inputs. The output register is not affected by RESET.
RLI/RLO	15	Register load input/register load output (open drain). This pin can be used as an input to directly load the output register, or it can be used as an output to detect whenever the output register has been loaded. When used as an output, a pullup resistor (1 k Ω nominal) is required. See read timing diagrams for additional details.
VCC	28	Power supply voltage.
\overline{WE}	25	Write enable input. When active (low) in conjunction with \overline{CS} low, the data present on D0-D7 will be asynchronously loaded into the counter as selected by LSB/MSB. See write timing diagrams for additional details.

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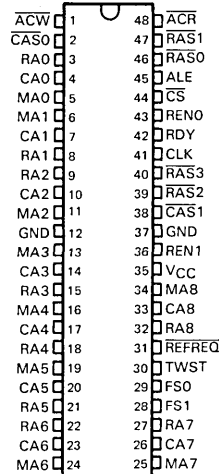
LSI Devices

THCT4502 DYNAMIC RAM CONTROLLER

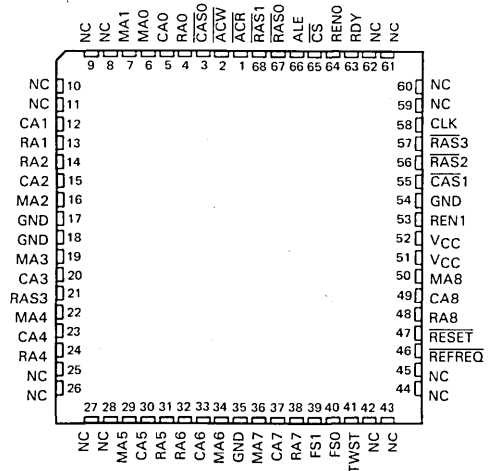
D2905, OCTOBER 1985

- Inputs are TTL- and CMOS-Voltage Compatible
- Controls Operation of 64K and 256K Dynamic RAMs
- Creates Static RAM Appearance
- One Package Contains Address Multiplexer, Refresh Control, and Timing Control
- Directly Addresses and Drives Up to 2 Megabytes of Memory Without External Drivers
- Operates from Microprocessor Clock
 - No Crystals, Delay Lines, or RC Networks
 - Eliminates Arbitration Delays
- Refresh May Be Internally or Externally Initiated
- Versatile
 - Strap-Selected Refresh Rate
 - Synchronous, Predictable Refresh
 - Selection of Distributed, Transparent, and Cycle-Steal Refresh Modes
 - Interfaces Easily to Popular Microprocessors
 - Asynchronous RESET Function Provided in FK and FN Packages
- High-Performance Si-Gate CMOS Technology
- Strap-Selected Wait State Generation for Microprocessor/Memory Speed Matching
- Ability to Synchronize or Interleave Controller with the Microprocessor System (Including Multiple Controllers)
- 3-State Outputs Allow Multiport Memory Configuration
- Performance Range:
 - 125 ns ALE low to $\overline{\text{CAS}}$ low
- Compatible with TMS4500A/B and with VTI VL4500A and VL4502
- Available in Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

THCT4502 . . . JD OR N PACKAGE
(TOP VIEW)



THCT4502 . . . FK OR FN PACKAGE
(TOP VIEW)



NC—No internal connection

2

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PRODUCTION DATA documents contain information current as of publication date. Products conform to these specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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THCT4502 DYNAMIC RAM CONTROLLER

description

The THCT4502 is a monolithic DRAM system controller providing address multiplexing, timing, control and refresh/access arbitration functions to simplify the interface of dynamic RAMs to microprocessor systems.

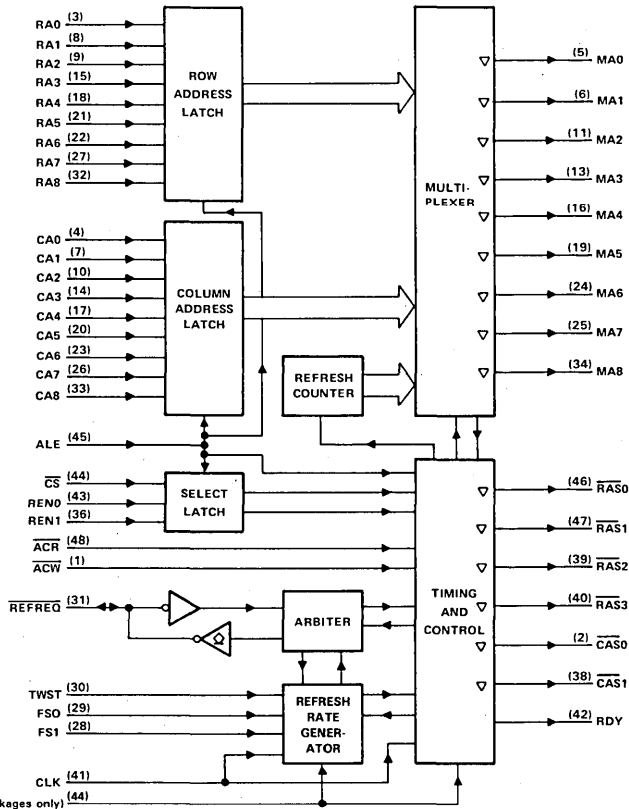
The controller contains an 18-bit multiplexer that generates the address lines for the memory device from the 18 system address bits and provides the strobe signals required by the memory to decode the address. A 9-bit refresh counter generates up to 512 row addresses required to refresh.

A refresh timer is provided to generate the necessary timing to refresh the dynamic memories and ensure data retention.

The THCT4502 also contains refresh/access arbitration circuitry to resolve conflicts between access requests and memory-refresh cycles.

The THCT4502 is characterized for operation from 0°C to 70°C.

functional block diagram



Pin numbers shown are for JD and N packages.

pin descriptions

RA0-RA8	Input	Row Address — These address inputs are used to generate the row address for the multiplexer.
CA0-CA8	Input	Column Address — These address inputs are used to generate the column address for the multiplexer.
MA0-MA8	Output	Memory Address — These three-state outputs are designed to drive the addresses of the dynamic RAM array.
ALE	Input	Address Latch Enable — This input is used to latch the 18 address inputs, \overline{CS} , \overline{RNO} , and $\overline{REN1}$. This also initiates an access cycle if \overline{CS} is low. The rising edge (low level to high level) of ALE returns all \overline{RAS} outputs to the high level.
\overline{CS}	Input	Chip Select — A low on this input enables an access cycle. The trailing edge of ALE latches the chip select input.
RNO, REN1	Inputs	\overline{RAS} Enable 0 and 1 — These inputs are used to select one of four banks of RAM when \overline{CS} is low. When $\overline{REN1}$ is low, the lower banks are enabled via $\overline{CAS0}$, $\overline{RAS0}$, and $\overline{RAS1}$. When $\overline{REN1}$ is high, the higher banks are enabled via $\overline{CAS1}$, $\overline{RAS2}$ and $\overline{RAS3}$. RNO selects $\overline{RAS0}$ and $\overline{RAS2}$ when low, or $\overline{RAS1}$ and $\overline{RAS3}$ when high. (see Table 2).
\overline{ACR} , \overline{ACW}	Input	Access Control, Read; Access Control, Write — A low on either of these inputs causes the column address to appear on MA0-MA8 and a low-going pulse from \overline{CAS} . The rising edge of \overline{ACR} or \overline{ACW} terminates the cycle by forcing \overline{RAS} and \overline{CAS} high. When \overline{ACR} and \overline{ACW} are both low, MA0-MA8, $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, $\overline{RAS3}$, $\overline{CAS0}$ and $\overline{CAS1}$ go into a high-impedance (floating) state.
CLK	Input	System Clock — This input provides the master timing to generate refresh cycle timings and refresh rate. Refresh rate is determined by the TWST, FS1, and FSO inputs.
\overline{REFREQ}	Input	Refresh Request — This input should be driven by an open-collector or open-drain output. On input, a low-going edge initiates a refresh cycle and will cause the internal refresh timer to be reset on the next falling edge of the CLK. As an output, a low-going edge signals an internal refresh request and that the refresh timer will be reset on the next low-going edge of CLK. \overline{REFREQ} will remain low until the refresh cycle is in progress and the current refresh address is present on MA0-MA8. (Note: \overline{REFREQ} contains an internal active pullup with a nominal resistance of 10 k Ω , which is disabled when \overline{REFREQ} is low).
$\overline{RAS0}$, $\overline{RAS1}$ $\overline{RAS2}$, $\overline{RAS3}$	Output	Row Address Strobe — These three-state outputs are used to latch the row address into the bank of DRAMs selected by RNO and REN1. On refresh, all \overline{RAS} signals are active.
$\overline{CAS0}$, $\overline{CAS1}$	Output	Column Address Strobe — These three-state outputs are used to latch the column address into the DRAM array.
RDY	Output	Ready — This totem-pole output synchronizes memories that are too slow to guarantee microprocessor access time requirements. This output is also used to inhibit access cycles during refresh when in cycle-steal mode.

2
LSI Devices

THCT4502 DYNAMIC RAM CONTROLLER

pin descriptions (continued)

TWST	Input	Timing/Wait Strap — A high on this input indicates a wait state should be added to each memory cycle. In addition it is used in conjunction with FSO and FS1 to determine refresh rate and timing or initialize the controller.
FS0, FS1	Inputs	Frequency Select 0; Frequency Select 1 — These are strap inputs to select Mode and Frequency of operation as shown in Table 1.
$\overline{\text{RESET}}^\dagger$	Input	$\overline{\text{RESET}}$ — Active-low input to initialize the controller asynchronously. Refresh Address is set to IFF16, internal refresh requests, synchronizer, and frequency divider are cleared. (Note: $\overline{\text{RESET}}$ contains an internal pullup resistor with a nominal resistance of 100 k Ω , which allows this pin to be left open.)

[†]This function is available only in the FK and FN packages.

TABLE 1. STRAP CONFIGURATION

STRAP INPUT MODES			WAIT STATES FOR MEMORY ACCESS	REFRESH RATE	MINIMUM CLOCK FREQUENCY (MHz)	REFRESH FREQUENCY (kHz)	CLOCK CYCLES FOR EACH REFRESH
TWST	FS1	FS0					
L	L	L [†]	0	EXTERNAL	—	REFREQ	4
L	L	H	0	EXTERNAL	—	REFREQ	3
L	H	L	0	CLK \div 61	3.904	64-95 [‡]	3
L	H	H	0	CLK \div 91	5.824	64-88 [§]	4
H	L	L	1	CLK \div 61	3.904	64-95 [‡]	3
H	L	H	1	CLK \div 91	5.824	64-75 [‡]	4
H	H	L	1	CLK \div 106	6.784	64-73 [‡]	4
H	H	H	1	CLK \div 121	7.744	64-83 [¶]	4

[†]This strap configuration resets the Refresh Timer Circuitry.

[‡]Upper figure in refresh frequency is the frequency that is produced if the minimum clock frequency of the next select state is used.

[§]Refresh frequency if clock frequency is 8 MHz.

[¶]Refresh frequency if clock frequency is 10 MHz.

TABLE 2. OUTPUT STROBE SELECTION

CONTROL INPUT		SELECTED OUTPUT					
REN1	RENO	RAS0	RAS1	RAS2	RAS3	CAS0	CAS1
L	L	X				X	
L	H		X			X	
H	L			X			X
H	H				X		X

NOTE: Changing the logic value of REN1 after a low-to-high transition of ALE and before $\overline{\text{ACX}}$ rises causes the other $\overline{\text{CAS}}$ to fall. Both $\overline{\text{CAS}}$ signals remain low until $\overline{\text{ACX}}$ rises.

functional description

The THCT4502 consists of six basic blocks: address and select latches, refresh rate generator, refresh counter, the multiplexer, the arbiter, and the timing and control block.

address and select latches

The address and select latches allow the DRAM controller to be used in systems that multiplex address and data on the same lines without external latches. The row address latches are transparent, meaning that while ALE is high, the output at MA0-MA8 follows the inputs RAO-RA8.

refresh rate generator

The refresh rate generator is a counter that indicates to the arbiter that it is time for a refresh cycle. The counter divides the clock frequency according to the configuration straps as shown in Table 1. The counter is reset when a refresh cycle is requested or when TWST, FS1, and FS0 are low. The configuration straps allow the matching of memories to the system access time. Upon power-up it is necessary to provide a reset signal by driving all three straps to the controller (or RESET for devices in the FK and FN packages only) low. A systems power-on reset (RESET) can be used to do this by connecting it to those straps that are desired high during operation. During this reset period, at least four clock cycles should occur.

refresh counter

The refresh counter contains the address of the row to be refreshed. The counter is decremented after each refresh cycle. A low-to-high transition on TWST sets the refresh counter to 1FF₁₆ (511₁₀).

multiplexer

The multiplexer provides the DRAM array with row, column, and refresh addresses at the proper times. Its inputs are the address latches and the refresh counter. The outputs provide up to 18 multiplexed addresses on nine lines.

arbiter

The arbiter provides two operational cycles: access and refresh. The arbiter resolves conflicts between cycle requests and cycles in execution, and schedules the inhibited cycle when used in cycle-steal mode.

timing and control block

The timing and control block executes the operational cycle at the request of the arbiter. It provides the DRAM array with RAS and CAS signals. It provides the CPU with a RDY signal. It controls the multiplexer during all cycles. It resets the refresh rate generator and decrements the refresh counter during refresh cycles.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC} (See Note 1)	-1.5 V to 7 V
Input diode current, I _{IK} (V _I < 0, V _I > V _{CC})	±20 mA
Output diode current, I _{OK} (V _O < 0, V _O > V _{CC})	±20 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±35 mA
Continuous current through V _{CC} or GND pins	±70 mA
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: FK or JD package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: FN or N package	260°C

[†] Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to network ground.

2
LSI Devices

THCT4502

DYNAMIC RAM CONTROLLER

recommended operating conditions

	MIN	NOM	MAX	UNIT
V _{CC} Supply voltage	4.5	5	5.5	V
V _{IH} High-level input voltage	2		V _{CC} +0.5	V
V _{IL} Low-level input voltage	-0.5 [†]		0.8	V
V _O Output voltage	-0.5		V _{CC} +0.5	V
t _t Input transition (rise and fall) time	0		500	ns
T _A Operating free-air temperature	0		70	°C

[†] The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	T _A = 25°C			UNIT
				MIN	TYP	MAX	
V _{OH} High-level output voltage	MA0-MA8, RAS0-RAS3, CAS0-CAS1	I _{OH} = -20 μA	4.5 V	4.4		4.4	V
		I _{OH} = -6 mA	4.5 V	3.86		3.76	
	RDY	I _{OH} = -20 μA	4.5 V	4.4		4.4	
		I _{OH} = -4 mA	4.5 V	3.86		3.76	
	REFREQ	I _{OH} = -20 μA	4.5 V	4		3.8	
V _{OL} Low-level output voltage	RDY, REFREQ	I _{OL} = 20 μA	4.5 V		0.1	0.1	V
		I _{OL} = 4 mA	4.5 V		0.32	0.37	
	MA0-MA8, RAS0-RAS3, CAS0, CAS1	I _{OL} = 20 μA	4.5 V		0.1	0.1	
		I _{OL} = 6 mA	4.5 V		0.32	0.37	
I _{IH} High-level input current except REFREQ	V _I = 5.5 V	5.5 V		0.1	1	μA	
I _{IL} Low-level input current	REFREQ	V _I = 0	5.5 V		-5	-50	μA
	RESET				-100	-250	
	All others				-0.1	-1	
I _{OZ} [‡] Off-state output current (3-state outputs only)	V _O = 0 to 5.5 V	5.5 V		±5	±50	μA	
I _{CC} Supply current	V _I = V _{CC} or 0, I _O = 0	5.5 V		5	15	mA	
ΔI _{CC} [§] Supply current change	One input at 0.5 V or 2.4 V, Other inputs at 0 V or V _{CC}	5.5 V		1.4	2.4	3	mA
C _i Input capacitance	V _I = 0, f = 1 MHz	5.5 V		5	10	10	pF

[‡] This parameter, I_{OZ}, the high impedance-state output current, applies only for three-state outputs and transceiver I/O pins.

[§] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

THCT4502 DYNAMIC RAM CONTROLLER

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		THCT4502-125		UNIT
		MIN	MAX	
$t_{c(C)}$	CLK cycle time	100		ns
$t_{w(CH)}$	CLK high pulse duration	45		ns
$t_{w(CL)}$	CLK low pulse duration	45		ns
t_{AEL-CL}	Time delay, ALE low to CLK starting low (see Note 1)	25		ns
t_{CL-AEL}	Time delay, CLK low to ALE starting low (see Note 1)	15		ns
t_{CL-AEH}	Time delay, CLK low to ALE	15		ns
$t_{w(AEH)}$	Pulse width ALE high	45		ns
t_{AV-AEL}	Time delay, address REN1, CS valid to ALE low	10		ns
t_{AEL-AX}	Time delay, ALE low to address not valid	15		ns
$t_{AEL-ACL}$	Time delay, ALE low to \overline{ACX} low (see Notes 3, 4, 5, and 6)	$t_{h(RA)} + 30$		ns
t_{ACH-CL}	Time delay, \overline{ACX} high to CLK low (see Notes 3 and 7)	30		ns
t_{ACL-CH}	Time delay, \overline{ACX} low to CLK starting high (to remove RDY)	30		ns
t_{RQL-CL}	Time delay, REFREQ low to CLK starting low (see Note 8)	35		ns
$t_{w(RQL)}$	Pulse width REFREQ low	30		ns
$t_{w(ACL)}$	\overline{ACX} low width (see Note 9)	120		ns
t_{reset}	Power-up reset	$4t_{cCLK}$		ns

- NOTES:
1. Coincidence of the trailing edge of CLK and the trailing edge of ALE should be avoided as the refresh/access occurs on the trailing CLK edge.
 2. If ALE rises before \overline{ACX} and a refresh request is present, the falling edge of CLK after t_{CL-AEH} will output the refresh address to MA0-MA7 and initiate a refresh cycle.
 3. These specifications relate to system timing and do not directly reflect device performance.
 4. On the access grant cycle following refresh, the occurrence of \overline{CAS} low depends on the relative occurrence of ALE low to \overline{ACX} low. If \overline{ACX} occurs prior to or coincident with ALE, then \overline{CAS} is timed from the CLK high transition that causes \overline{RAS} low. If \overline{ACX} occurs 20 ns or more after ALE, then \overline{CAS} is timed from the CLK low transition following the CLK high transition causing \overline{RAS} low.
 5. For maximum speed access (internal delays on both access and access grant cycles), \overline{ACX} should occur prior to or coincident with ALE.
 6. $t_{h(RA)}$ is the dynamic memory row address hold time. \overline{ACX} should follow ALE by $t_{AEL-CEL}$ in systems where the required $t_{h(RA)}$ is greater than $t_{REL-MAX}$ minimum.
 7. The minimum of 20 ns is specified to ensure arbitration will occur on falling CLK edge, t_{ACH-CL} also affects precharge time such that the minimum t_{ACH-CL} should be equal or greater than: $t_{w(RH)} - t_{w(CL)} + 30$ ns (for a cycle where \overline{ACX} high occurs prior to ALE high) where $t_{w(RH)}$ is the DRAM \overline{RAS} precharge time.
 8. This parameter is necessary only if refresh arbitration is to occur on this low-going CLK edge (in systems where refresh is synchronized to external events).
 9. The specification $t_{w(ACL)}$ is designed to allow a \overline{CAS} pulse. This assures normal operation of the device in testing and system operation.

2
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THCT4502 DYNAMIC RAM CONTROLLER

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 1)

PARAMETER	TEST CONDITIONS	THCT4502-125		UNIT
		MIN	MAX	
$t_{AEL-REL}$ Time delay, ALE low to \overline{RAS} starting low	$C_L = 180$ pF		45	ns
$t_{RAV-MAV}$ Time delay, row address valid to memory address valid	$C_L = 360$ pF		50	ns
$t_{AEH-MAV}$ Time delay, ALE high to valid memory address	$C_L = 360$ pF		90	ns
$t_{AEL-RYL}$ Time delay, ALE to RDY starting low (TWST = 1 or refresh in progress)	$C_L = 40$ pF		40	ns
$t_{AEL-CEL}$ Time delay, ALE low to \overline{CAS} starting low (see Note 10)	$C_L = 360$ pF	50	125	ns
$t_{AEH-REH}$ Time delay, ALE high to \overline{RAS} starting high	$C_L = 180$ pF		50	ns
$t_{ACL-MAX}$ Row address valid after \overline{ACX}	$C_L = 360$ pF	15		ns
$t_{MAV-CEL}$ Time delay, memory address valid to \overline{CAS} starting low	$C_L = 360$ pF	0		ns
$t_{ACL-CEL}$ Time delay, \overline{ACX} low to \overline{CAS} starting low (see Note 10)	$C_L = 360$ pF	40	100	ns
$t_{ACH-REH}$ Time delay, \overline{ACX} to \overline{RAS} starting high	$C_L = 180$ pF		55	ns
$t_{ACH-CEH}$ Time delay, \overline{ACX} high to \overline{CAS} starting high	$C_L = 360$ pF	5	45	ns
$t_{ACH-MAX}$ Column address valid after \overline{ACX} high	$C_L = 360$ pF	10		ns
t_{CH-RYH} Time delay, CLK high to RDY starting high (after \overline{ACX} low) (see Note 11)	$C_L = 40$ pF		60	ns
$t_{RFL-RFL}$ Time delay, \overline{REFREQ} external till supported by \overline{REFREQ} internal	$C_L = 40$ pF		35	ns
t_{CH-RFL} Time delay, CLK high till \overline{REFREQ} internal starting low	$C_L = 40$ pF		50	ns
t_{CL-MAV} Time delay, CLK low till refresh address valid	$C_L = 360$ pF		100	ns
t_{CH-RRL} Time delay, CLK high till refresh \overline{RAS} starting low	$C_L = 180$ pF	10	60	ns
$t_{MAV-RRL}$ Time delay, refresh address valid till refresh \overline{RAS} low	$C_L = 180$ pF	5		ns
t_{CL-RFH} Time delay, CLK low to \overline{REFREQ} starting high (3 cycle refresh)	$C_L = 40$ pF		70	ns
t_{CH-RFH} Time delay, CLK high to \overline{REFREQ} starting high (4 cycle refresh)	$C_L = 40$ pF		70	ns
t_{CH-RRH} Time delay, CLK high to refresh \overline{RAS} starting high	$C_L = 160$ pF	5	60	ns
t_{CH-MAX} Refresh address valid after CLK high	$C_L = 360$ pF	10		ns

NOTES: 10. The falling edge of \overline{CAS} occurs when both ALE low to \overline{CAS} low time delay ($t_{AEL-CEL}$) and \overline{ACX} low to \overline{CAS} low time delay ($t_{ACL-CEL}$) have elapsed, i.e., if \overline{ACX} goes low prior to ($t_{AEL-CEL} - t_{ACL-CEL}$) after the falling edge of ALE, the falling edge of \overline{CAS} is measured from the falling edge of ALE ($t_{AEL-CEL}$). Otherwise, the access time increases and the falling edge of \overline{CAS} is measured from the falling edge of \overline{ACX} ($t_{ACL-CEL}$).

11. RDY returns high on the rising edge of CLK. If TWST = 0, then on an access grant cycle RDY goes high on the same edge that causes access \overline{RAS} low. If TWST = 1, then RDY goes to the high level on the first rising CLK edge after \overline{ACX} goes low on access cycles and on the next rising edge after the edge that causes access \overline{RAS} low on access grant cycles (assuming \overline{ACX} low).

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LSI Devices

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 1) (continued)

PARAMETER	TEST CONDITIONS	THCT4502-125		UNIT
		MIN	MAX	
t _{CH-REL} Time delay, CLK high till access $\overline{\text{RAS}}$ starting low	C _L = 180 pF		60	ns
t _{CL-CEL} Time delay, CLK low to access $\overline{\text{CAS}}$ starting low (see Note 12)	C _L = 360 pF		100	ns
t _{CL-MAX} Row address valid after CLK low	C _L = 360 pF	25		ns
t _{REL-MAX} Row address valid after RAS low	C _L = 360 pF	25		ns
t _{AEH-MAX} Column address valid after ALE high	C _L = 360 pF	10		ns
t _{dis} Output disable time (3-state outputs)	C _L = 360 pF		125	ns
t _{en} Output enable time (3-state outputs)	C _L = 360 pF		75	ns
t _{CAV-CEL} Time delay, column address valid to $\overline{\text{CAS}}$ starting low after refresh (see Note 12)	C _L = 360 pF	0		ns
t _{CH-CEL} Time delay, CLK high to access $\overline{\text{CAS}}$ starting low (see Note 13)	C _L = 360 pF		180	ns
t _{t(CEL)} $\overline{\text{CAS}}$ fall time	C _L = 360 pF		20	ns
t _{t(CEH)} $\overline{\text{CAS}}$ rise time	C _L = 360 pF		50	ns
t _{t(REL)} $\overline{\text{RAS}}$ fall time	C _L = 180 pF		30	ns
t _{t(REH)} $\overline{\text{RAS}}$ rise time	C _L = 180 pF		40	ns
t _{t(MAV)} Address transition time	C _L = 180 pF		40	ns
t _{t(RYL)} RDY fall time	C _L = 40 pF		20	ns
t _{t(RYH)} RDY rise time	C _L = 40 pF		50	ns

NOTES: 12. The occurrence of $\overline{\text{CAS}}$ low is guaranteed not to occur until the column address is valid on MAX.

13. On the access grant cycle following refresh, the occurrence of $\overline{\text{CAS}}$ low depends on the relative occurrence of ALE low to ACX low. If ACX occurs prior to or coincident with ALE then $\overline{\text{CAS}}$ is timed from the CLK high transition that causes $\overline{\text{RAS}}$ low. If ACX occurs 20 ns or more after ALE then $\overline{\text{CAS}}$ is timed from the CLK low transition following the CLK high transition causing $\overline{\text{RAS}}$ low. (See Refresh Cycle Timing Diagram)

PARAMETER MEASUREMENT INFORMATION

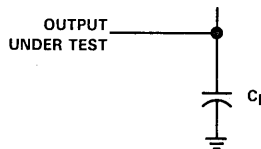
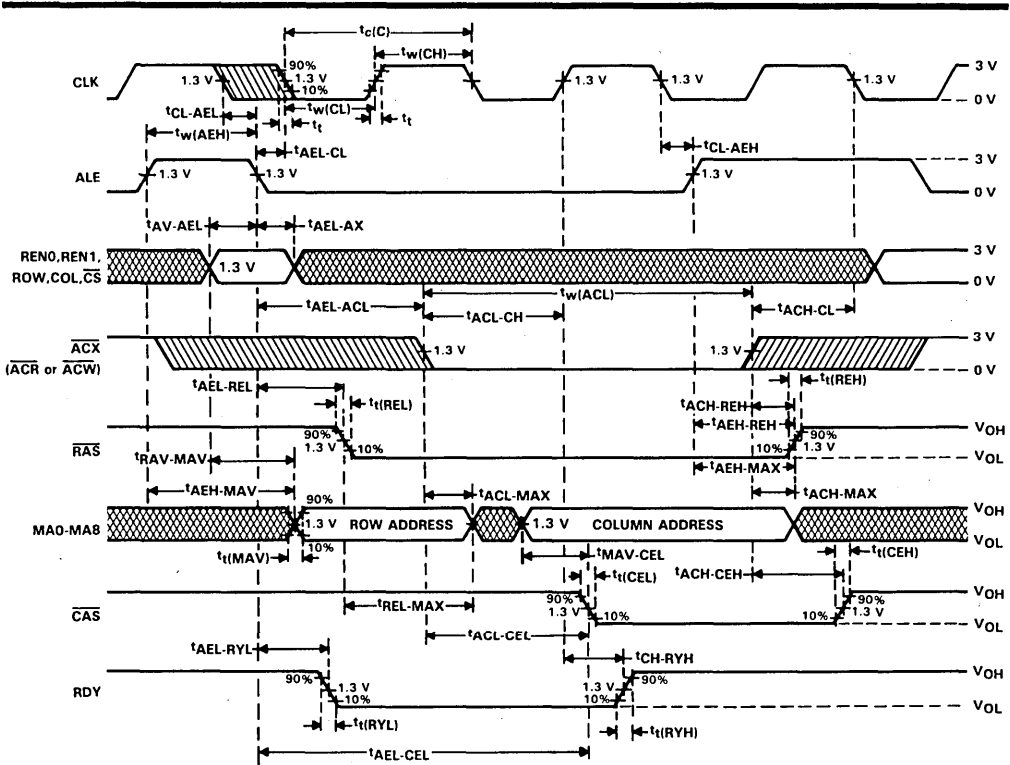


FIGURE 1. LOAD CIRCUIT

THCT4502 DYNAMIC RAM CONTROLLER



NOTE 14: All transition times (t_t) are measured between 10% and 90% points.

FIGURE 2. ACCESS CYCLE TIMING

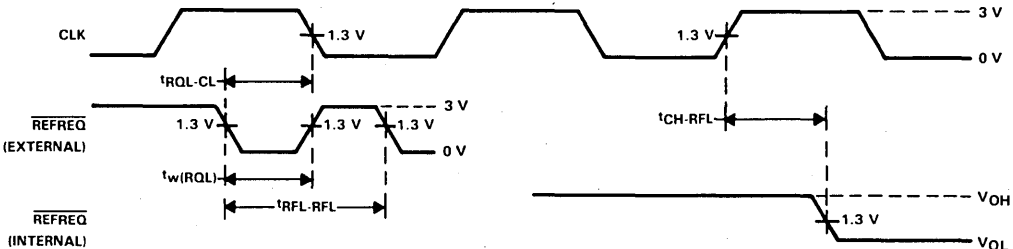
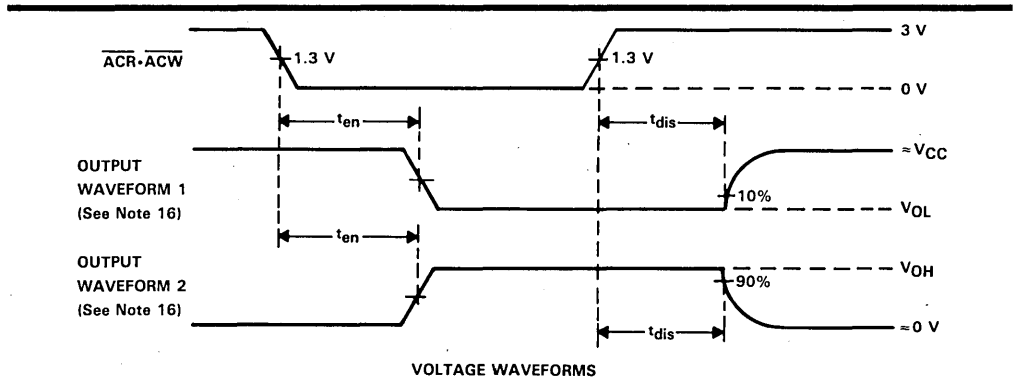


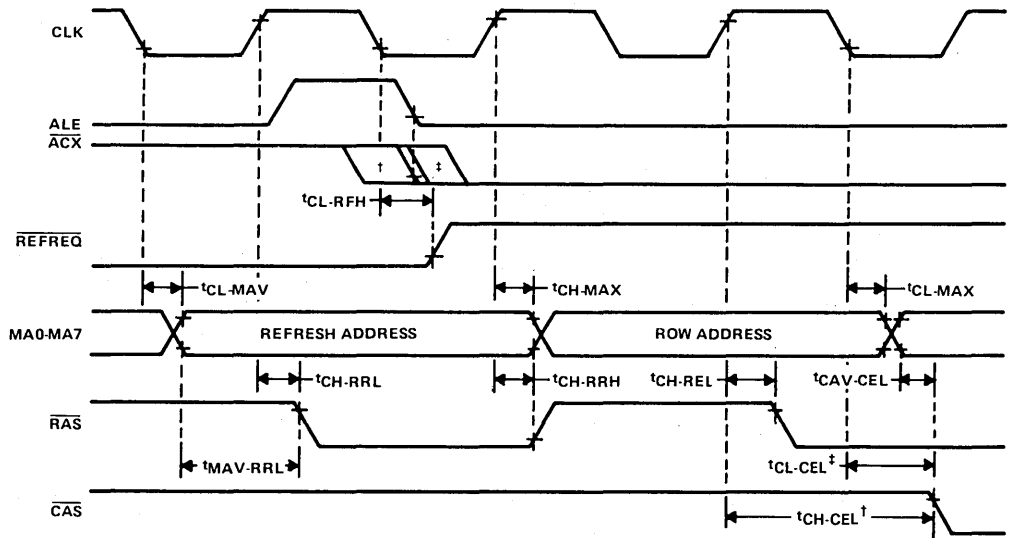
FIGURE 3. REFRESH REQUEST TIMING

NOTE 15: All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_{out} = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.



NOTE 16: Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the access controls. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the access controls.

FIGURE 4. ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS



† On access grant cycle following refresh, $\overline{\text{CAS}}$ low and address multiplexing are timed from CLK high transition ($t_{\text{CH-CEL}}$) if $\overline{\text{ACX}}$ low occurs prior to or coincident with the falling edge of ALE.

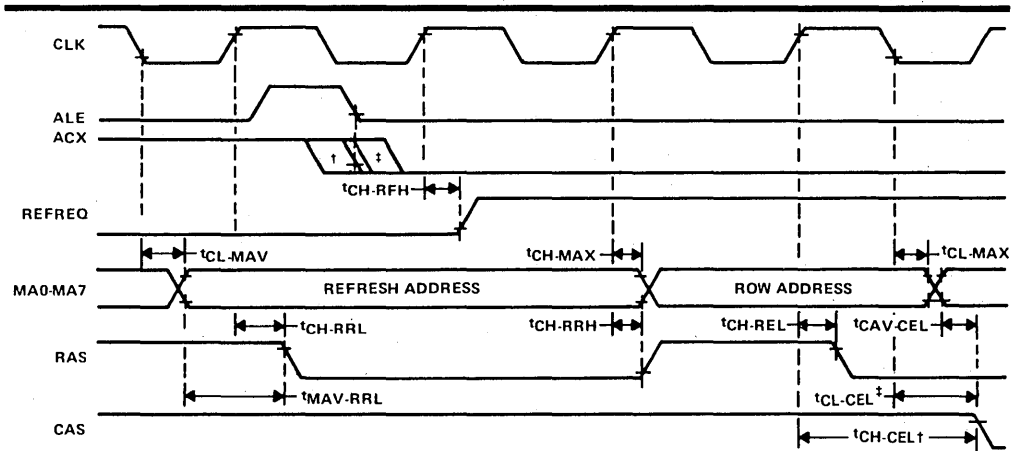
‡ On access grant cycle following refresh, $\overline{\text{CAS}}$ low and address multiplexing are timed from CLK low transition ($t_{\text{CL-CEL}}$) if $\overline{\text{ACX}}$ low occurs 20 ns or more after the falling edge of ALE.

NOTE 15: All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_{\text{out}} = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.

FIGURE 5. REFRESH CYCLE TIMING (THREE CYCLE)

2
LSI Devices

THCT4502
DYNAMIC RAM CONTROLLER



† On access grant cycle following refresh, \overline{CAS} low and address multiplexing are timed from CLK high transition (t_{CH-CEL}) if \overline{ACX} low occurs prior to or coincident with the falling edge of ALE.

‡ On access grant cycle following refresh, \overline{CAS} low and address multiplexing are timed from CLK low transition (t_{CL-CEL}) if \overline{ACX} low occurs 20 ns or more after the falling edge of ALE.

NOTE 15: All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_{out} = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.

FIGURE 6. REFRESH CYCLE TIMING (FOUR CYCLE)

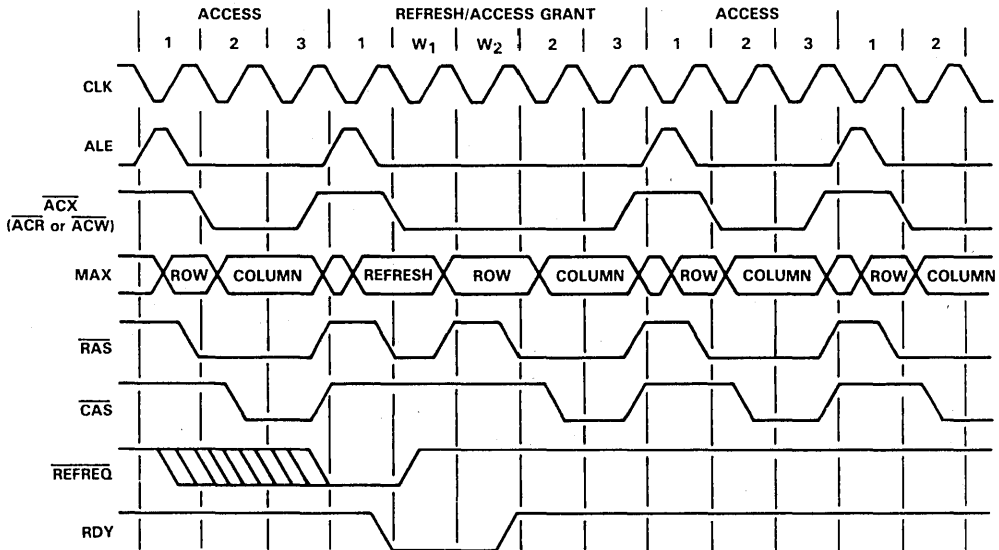


FIGURE 7. TYPICAL ACCESS/REFRESH/ACCESS CYCLE (THREE-CYCLE, TWST IS LOW)

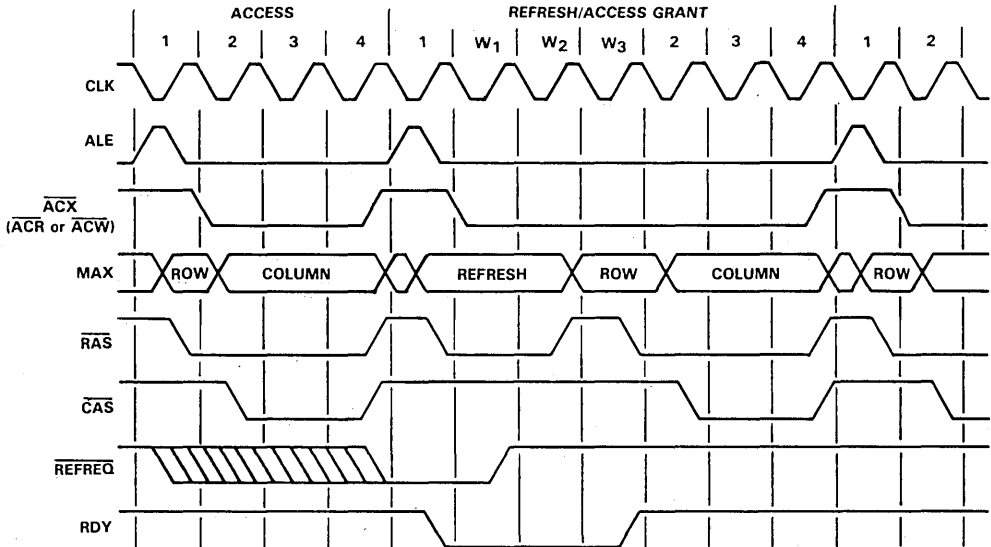


FIGURE 8. TYPICAL ACCESS/REFRESH/ACCESS CYCLE (FOUR-CYCLE; TWST IS LOW)

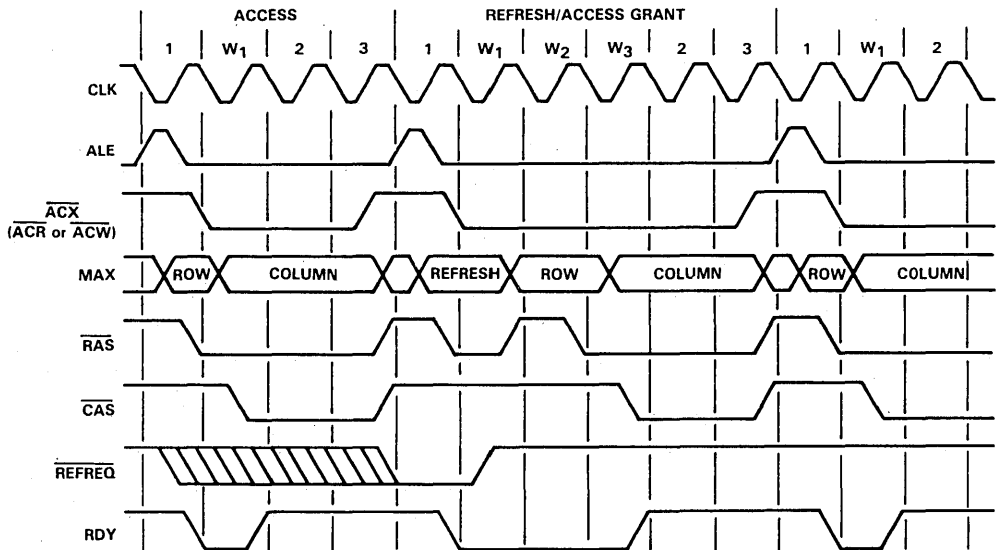


FIGURE 9. TYPICAL ACCESS/REFRESH/ACCESS CYCLE (THREE-CYCLE; TWST IS HIGH)

**THCT4502
DYNAMIC RAM CONTROLLER**

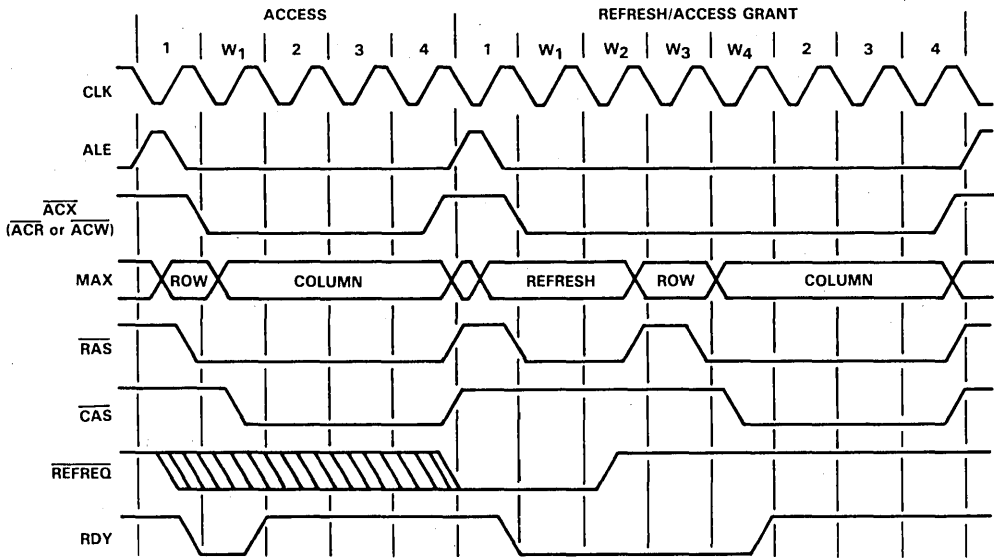
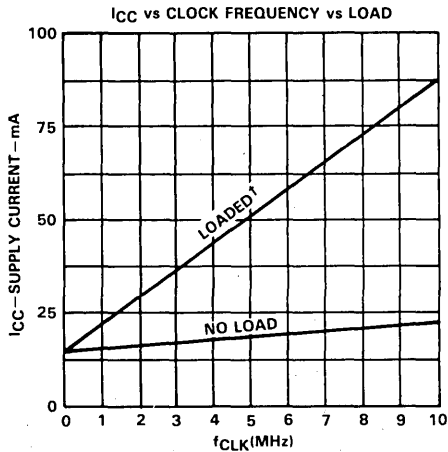


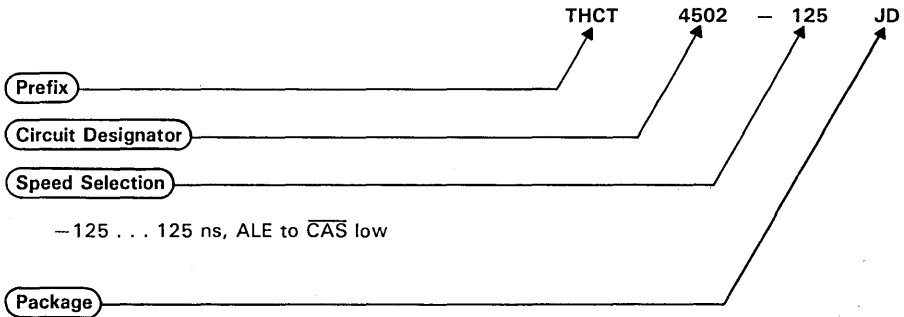
FIGURE 10. TYPICAL ACCESS/REFRESH/ACCESS CYCLE (FOUR-CYCLE, TWST IS HIGH)



[†] Load is 360 pF for $\overline{\text{CAS}}$ and MA outputs, 180 pF for all $\overline{\text{RAS}}$ outputs.

FIGURE 11.

ORDERING INSTRUCTIONS



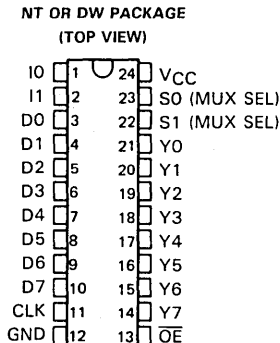
- 125 . . . 125 ns, ALE to $\overline{\text{CAS}}$ low

N, JD (Dual in-line packages)
FK, FN (Chip carrier packages)

2

LSI Devices

- Four 8-Bit Registers
- Dual 2-Level or Single 4-Level Pipeline Registers
- Any One of Four Registers Selectable for Output
- High-Speed Low-Power CMOS Logic
- Fully TTL Compatible
- Dependable Texas Instruments Quality and Reliability



description

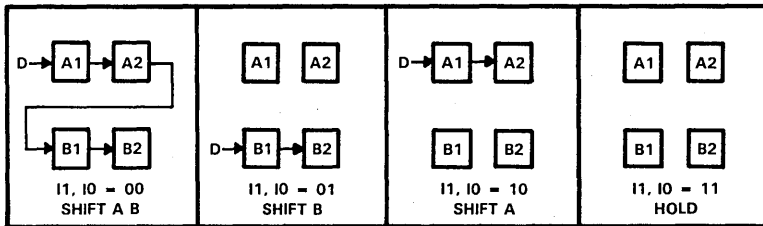
The THCT29520 and THCT29521 are high-speed CMOS multilevel pipeline registers. They are interchangeable with the Advanced Micro Device bipolar AM29520 and AM29521 but dissipate a fraction of the power.

The THCT29520 and THCT29521 contain four 8-bit positive-edge-triggered registers. The registers can operate as one set of 4-level pipeline registers or two sets of 2-level pipeline registers. The output can be selected from any one of the four registers.

The THCT29520 and THCT29521 differ in the way data is transferred in the dual 2-level register modes (I = 01 or 10). For the THCT29520, new data is written into the first-level register while the old data in the first-level register is shifted into the second-level register. For the THCT29521, new data is written over the old data in the first-level register. The data in the second-level register remains unchanged.

The THCT29520 and THCT29521 are characterized for operation from 0°C to 70°C. The THCT29520E and THCT29521E are characterized for operation from -40°C to 85°C.

THCT29520 MODES

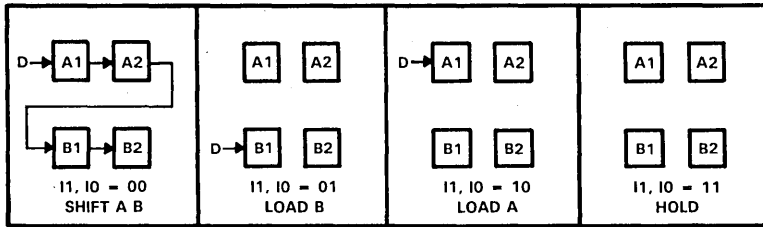


I1	IO	OPERATION	A1	A2	B1	B2
L	L	SHIFT A B	D	A ₁₀	A ₂₀	B ₁₀
L	H	SHIFT B	A ₁₀	A ₂₀	D	B ₁₀
H	L	SHIFT A	D	A ₁₀	B ₁₀	B ₂₀
H	H	HOLD	A ₁₀	A ₂₀	B ₁₀	B ₂₀

2
LSI Devices

THCT29520, THCT29521 MULTILEVEL PIPELINE REGISTERS

THCT29521 MODES



I1	I0	OPERATION	A1	A2	B1	B2
L	L	SHIFT A B	D	A1 ₀	A2 ₀	B1 ₀
L	H	LOAD B	A1 ₀	A2 ₀	D	B2 ₀
H	L	LOAD A	D	A2 ₀	B1 ₀	B2 ₀
H	H	HOLD	A1 ₀	A2 ₀	B1 ₀	B2 ₀

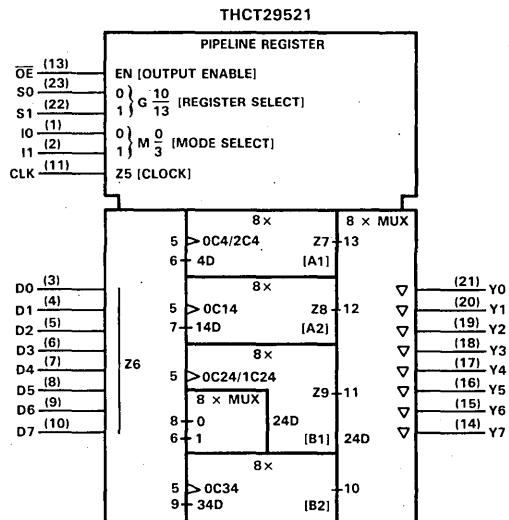
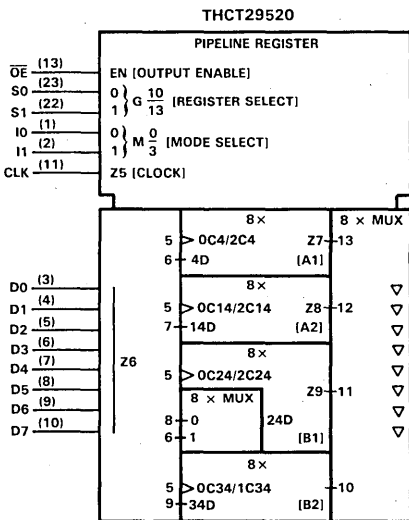
OUTPUT FUNCTION TABLE

INPUTS			OUTPUT
OE	S1	S0	Y
L	L	L	B2
L	L	H	B1
L	H	L	A2
L	H	H	A1
H	X	X	Z

2

LSI Devices

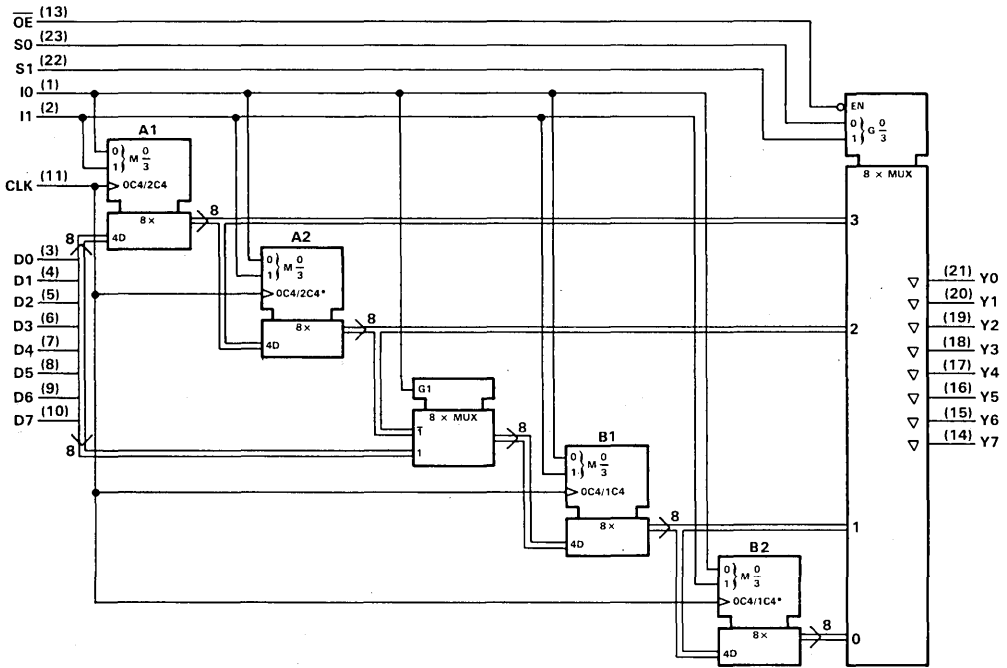
logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

THCT29520, THCT29521 MULTILEVEL PIPELINE REGISTERS

logic diagram (positive logic)



2
LSI Devices

* The label "OC4/2C4" means that the clock in register A2 affects the eight data inputs of that register, collectively labeled "4D", only in modes 0 and 2 (I1, IO = L L and H L, respectively). This logic diagram applies specifically for the THCT29520. For the THCT29521, the labels marked with the asterisks in registers A2 and B2 would both be reduced to "OC4" indicating that these clocks have effect only in mode 0 in that device. Otherwise this diagram applies to both devices.

absolute maximum rating over operating free-air temperature range (see Note 1)

Supply voltage, VCC	-0.5 V to 7 V
Input diode current, I _{IK} (V _I < 0 or V _I > V _{CC})	± 20 mA
Output diode current, I _{OK} (V _O < 0 or V _O > V _{CC})	± 20 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	± 35 mA
Continuous current through V _{CC} or GND	± 70 mA
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	300°C
Storage temperature range	-65°C to 150°C

NOTE 1: Stress beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THCT29520, THCT29521 MULTILEVEL PIPELINE REGISTERS

recommended operating conditions

	THCT29520E THCT29521E			THCT29520 THCT29521			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage	0	0.8		0	0.8		V
V _I Input voltage	0	V _{CC}		0	V _{CC}		V
V _O Output voltage	0	V _{CC}		0	V _{CC}		V
t _t Input transition (rise and fall) time	0	500		0	500		ns
T _A Operating free-air temperature	-40		85	-0		70	°C

electrical characteristics over recommended operating temperature range, V_I = V_{IH} or V_{IL} (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			THCT29520E THCT29521E		THCT29520 THCT29521		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -20 μA	4.5 V	4.4	4.499		4.4		4.4	V	
	I _{OH} = -8 mA	4.5 V	3.9	4.3		3.8		3.8		
V _{OL}	I _{OL} = 20 μA	4.5 V	0.001 0.1		0.1		0.1		V	
	I _{OL} = 8 mA	4.5 V	0.17 0.26		0.33		0.33			
I _I	V _I = 0 to V _{CC}	5.5 V	±0.1 +100		±1000		±1000		nA	
I _{OZ}	V _I = 0 or V _{CC}	5.5 V	±0.01 ±0.5		±5		±5		μA	
I _{CC}	V _I < 0.5 V or > 2.4 V, I _O = 0	4.5 V	8		80		80		μA	
C _i		4.5 V to 5.5 V	3 10		10		10		pF	

timing requirements over recommended operating free-air temperature range

PARAMETER	V _{CC}	T _A = 25°C			THCT29520E THCT29521E		THCT29520 THCT29521		UNIT
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _w Pulse duration, CLK high or low	4.5 V	6			12		12		ns
	5.5 V	5			10		10		
t _{su} Setup time before CLK†	4.5 V	10			15		15		ns
	5.5 V	8			13		13		
t _h Hold time after CLK†	4.5 V	0			0		0		ns
	5.5 V	0			0		0		

THCT29520, THCT29521 MULTILEVEL PIPELINE REGISTERS

switching characteristics over recommended free-air temperature range, $C_L = 50$ pF (unless otherwise noted) See Note 2

PARAMETER	FROM	TO	V _{CC}	T _A = 25°C			THCT29520E THCT29521E		THCT29520 THCT29521		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	CLK ↑	Y	4.5 V	18			27		26		ns
			5.5 V	16			25		24		
t _{pd}	S0, S1	Y	4.5 V	17			27		26		ns
			5.5 V	15			25		24		
t _{en}	\overline{OE} ↓	Y	4.5 V	10			16		15		ns
			5.5 V	7			15		14		
t _{dis}	\overline{OE} ↑	Y	4.5 V	14			20		20		ns
			5.5 V	13			20		20		
t _t		Y	4.5 V	7			12		12		ns
			5.5 V	7			12		12		

C _{pd}	Power dissipation capacitance [†]	No load, T _A = 25°C	110 pF typ
-----------------	--	--------------------------------	------------

[†]No load dynamic power dissipation, $P_d = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$

NOTE 2: For load circuit and voltage waveforms, see page 1-14 of the *High-Speed CMOS Logic Data Book*, 1984.



LSI Devices

2

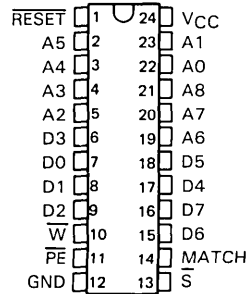
LSI Devices

TMS2150 CACHE ADDRESS COMPARATOR

D2911, MARCH 1982—REVISED SEPTEMBER 1985

- Fast Address to Match Valid Delay — Three Speed Ranges: 35 ns, 45 ns, 55 ns
- 512 × 9 Internal RAM
- 300-Mil 24-Pin Ceramic Side-Brazed or Plastic Dual-In-Line or Small Outline Packages
- Max Power Dissipation: 660 mW
- On-Chip Parity Generation and Checking
- Parity Error Output/Force Parity Error Input
- On-Chip Address/Data Comparator
- Asynchronous, Single-Cycle Reset
- Easily Expandable
- Fully Static
- Reliable SMOS (Scaled NMOS) Technology
- TTL- and CMOS-Compatible Inputs and Outputs

DW, JD, OR NT PACKAGE
(TOP VIEW)



2
LSI Devices

description

This 8-bit-slice cache address comparator consists of a high-speed 512 × 9 static RAM array, parity generator, parity checker, and 9-bit high-speed comparator. It is fabricated using N-channel silicon gate technology for high speed and simple interface with MOS and bipolar TTL circuits. The cache address comparator is easily cascadable for wider tag addresses or deeper tag memories. Significant reductions in cache memory component count, board area, and power dissipation can be achieved with this device.

When \bar{S} is low and \bar{W} is high, the cache address comparator compares the contents of the memory location addressed by A0-A8 with the data on D0-D7 plus generated parity. An equality is indicated by a high level on the MATCH output. A low-level output from \bar{PE} signifies a parity error in the internal RAM data. \bar{PE} is an N-channel open-drain output for easy OR-tying. During a write cycle (\bar{S} and \bar{W} low), data on D0-D7 plus generated even parity are written in the 9-bit memory location addressed by A0-A8. Also during write, a parity error may be forced by holding \bar{PE} low.

A \bar{RESET} input is provided for initialization. When \bar{RESET} goes low, all 512 × 9 RAM locations are cleared and the MATCH output is forced high.

The cache address comparator operates from a single +5 V supply and is offered in a 24-pin 300-mil ceramic side brazed or plastic dual-in-line packages. The device is fully TTL compatible and is characterized for operation from 0°C to 70°C.

MATCH OUTPUT DESCRIPTION

MATCH = V_{OH} if: [A0-A8] = D0-D7 + parity,
or: $\bar{RESET} = V_{IL}$,
or: $\bar{S} = V_{IH}$,
or: $\bar{W} = V_{IL}$

MATCH = V_{OL} if: [A0-A8] ≠ D0-D7 + parity,
with $\bar{RESET} = V_{IH}$,
 $\bar{S} = V_{IL}$, and $\bar{W} = V_{IH}$

FUNCTION TABLE

OUTPUT		FUNCTION DESCRIPTION
MATCH	\bar{PE}	
L	L	Parity Error
L	H	Not Equal
H	L	Undefined Error
H	H	Equal

Where S = V_{IL} , W = V_{IH} , RESET = V_{IH}

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

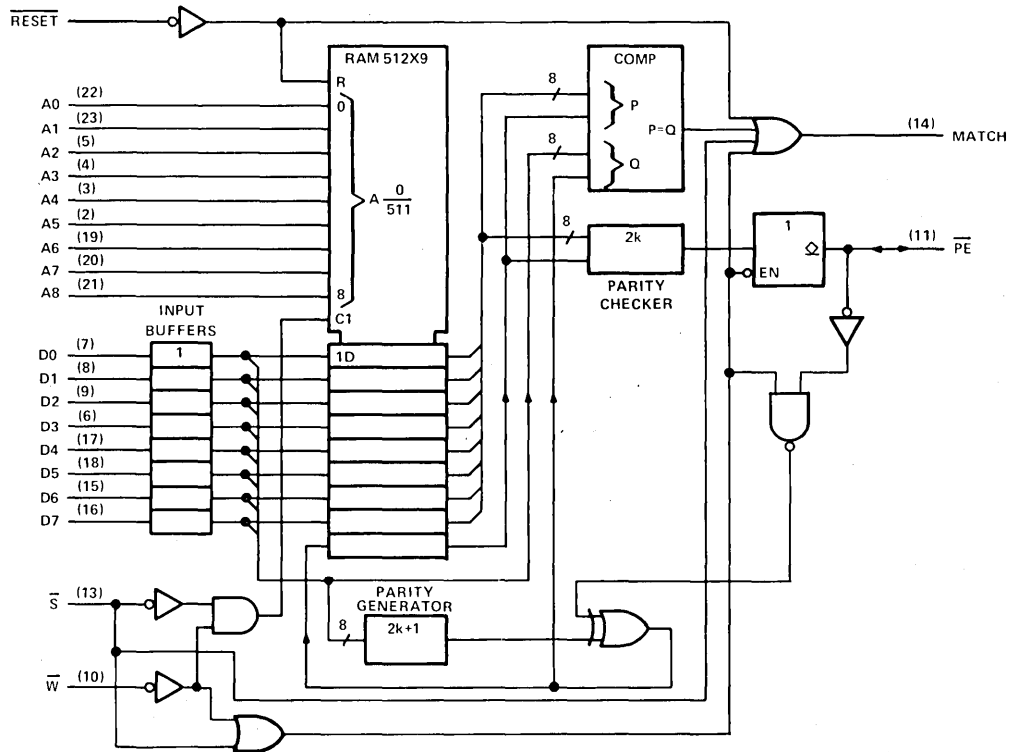


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TMS2150 CACHE ADDRESS COMPARATOR

functional block diagram (positive logic)



This diagram has been changed to correct errors in previous versions. No functional change has been made in the chip.

PIN FUNCTIONAL DESCRIPTION

PIN		DESCRIPTION
NAME	NO.	
RESET	1	RESET input. Asynchronously clears entire RAM array and forces MATCH high when RESET is at V_{IL} and \overline{W} is at V_{IH} .
A0	22	Address inputs. Address 1 of 512-by-9-bit random-access memory locations. Must be stable for the duration of the write cycle.
A1	23	
A2	5	
A3	4	
A4	3	
A5	2	
A6	19	
A7	20	
A8	21	
D0	7	Data inputs. Compared with memory location addressed by A0-A8 when \overline{W} is at V_{IH} and \overline{S} is at V_{IL} . Provide input data to RAM when \overline{W} is at V_{IL} and \overline{S} is at V_{IL} .
D1	8	
D2	9	
D3	6	
D4	17	
D5	18	
D6	15	
D7	16	
\overline{W}	10	Write control input. Writes D0 through D7 and generated parity into RAM and forces MATCH high when \overline{W} is at V_{IL} and \overline{S} is at V_{IL} . Places selected device in compare mode if \overline{W} is at V_{IH} .
\overline{PE}	11	Parity error input/output. During write cycles, \overline{PE} can force a parity error into the 9-bit location specified by A0 through A8 when \overline{PE} is at V_{IL} . For compare cycles, \overline{PE} at V_{OL} indicates a parity error in the stored data. \overline{PE} is an open-drain output so an external pull-up resistor is required.
GND	12	Ground
\overline{S}	13	Chip select input. Enables device when \overline{S} is at V_{IL} . Deselects device and forces MATCH high when \overline{S} is at V_{IH} .
MATCH	14	When MATCH output is at V_{OH} during a compare cycle, D0 through D7 plus parity equal the contents of the 9-bit memory location addressed by A0 through A8.
VCC	24	5-V supply voltage



LSI Devices

absolute maximum ratings over operating free-air temperature range (unless otherwise specified)

Supply voltage range, VCC (see Note 1)	-1.5 to 7 V
Input voltage range, any input	-1.5 to 7 V
Continuous power dissipation	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, VCC	4.5	5	5.5	V
High-level input voltage, V_{IH}		2	6	V
Low-level input voltage, V_{IL} (See Note 2)	-1		0.8	V
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

TMS2150 CACHE ADDRESS COMPARATOR

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TMS2150-3			TMS2150-4 TMS2150-5			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH(M)} MATCH high-level output voltage	I _{OH} = -2 mA, V _{CC} = 4.5 V	2.4			2.4			V
	I _{OH} = -20 μA, V _{CC} = 4.5 V	3.5			3.5			
V _{OL(M)} MATCH low-level output voltage	I _{OL} = 4 mA, V _{CC} = 4.5 V		0.4			0.4		V
V _{OL(PE)} \overline{PE} low-level output voltage	I _{OL} = 12 mA, V _{CC} = 4.5 V		0.4			0.4		V
I _I Input current	V _I = 0 V to 5.5 V			10			10	μA
I _{OL(PE)} \overline{PE} output sink current	V _{OL} = 0.4 V, V _{CC} = 4.5 V	12			12			mA
I _{OS} Short-circuit MATCH output current	V _O = GND, V _{CC} = 5.5 V			-150			-150	mA
I _{CC1} Supply current (operative)	$\overline{RESET} = V_{IH}$			145			135	mA
I _{CC2} Supply current (reset)	$\overline{RESET} = V_{IL}$			155			145	mA
C _i Input capacitance	V _I = 0 V, f = 1 MHz			5			5	pF
C _o Output capacitance	V _O = 0 V, f = 1 MHz			6			6	pF

2

LSI Devices

TMS2150 CACHE ADDRESS COMPARATOR

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TMS2150-3		TMS2150-4		TMS2150-5		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
$t_a(A)$ Access time from address to MATCH		35		45		55	ns
$t_a(A-P)$ Access time from address to \overline{PE}		45		55		65	ns
$t_a(S)$ Access time from \overline{S} to MATCH		20		25		35	ns
$t_p(D)$ Propagation time, data inputs to MATCH		20		35		45	ns
$t_p(R-MH)$ Propagation time, \overline{RESET} low to MATCH high		30		30		40	ns
$t_p(S-MH)$ Propagation time, \overline{S} high to MATCH high		20		25		35	ns
$t_p(W-MH)$ Propagation time, \overline{W} low to MATCH high		20		25		35	ns
$t_p(W-PH)$ Propagation time, \overline{W} low to \overline{PE} high		20		25		35	ns
$t_v(A)$ MATCH valid time after change of address	5		5		5		ns
$t_v(A-P)$ \overline{PE} valid time after change of address	15		15		15		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TMS2150-3		TMS2150-4		TMS2150-5		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
$t_c(W)$ Write cycle time, without writing \overline{PE}	30		40		50		ns
$t_{cPE}(W)$ Write cycle time, writing \overline{PE} (see Note 3)	35		40		50		ns
$t_c(rd)$ Read cycle time	35		45		55		ns
$t_w(RL)$ Pulse duration, \overline{RESET} low	35		35		45		ns
$t_w(WL)$ Pulse duration, \overline{W} low, without writing \overline{PE}	20		25		30		ns
$t_{wPE}(WL)$ Pulse duration, \overline{W} low, writing \overline{PE} (see Note 3)	35		40		45		ns
$t_{su}(A)$ Address setup time before \overline{W} low	0		0		0		ns
$t_{su}(D)$ Data setup time before \overline{W} high	20		25		30		ns
$t_{su}(P)$ \overline{PE} setup time before \overline{W} high (see Note 3)	20		25		30		ns
$t_{su}(S)$ Chip select setup time before \overline{W} high	20		25		30		ns
$t_{su}(RH)$ \overline{RESET} inactive setup time before first tag cycle	0		0		0		ns
$t_h(A)$ Address hold time after \overline{W} high	0		0		5		ns
$t_h(D)$ Data hold time after \overline{W} high	5		5		10		ns
$t_h(P)$ \overline{PE} hold time after \overline{W} high	0		0		5		ns
$t_h(S)$ Chip select hold time after \overline{W} high	0		0		0		ns
t_{AVWH} Address valid to write enable high	30		40		50		ns

NOTE 3: Parameters $t_{wPE}(WL)$ and $t_{su}(P)$ apply only during the write cycle time when writing a parity error, $t_{cPE}(W)$.

ac test conditions

Input pulse levels	GND to 3 V
Input rise and fall times	5 ns
Input timing reference levels	1.5 V
Output timing reference level	1.5 V
Output loading	See Figures 1 and 2

2

LSI Devices

**TMS2150
CACHE ADDRESS COMPARATOR**

PARAMETER MEASUREMENT INFORMATION

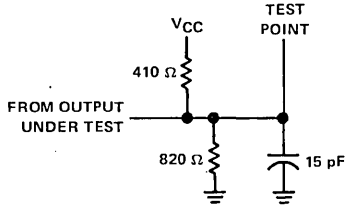


FIGURE 1. \overline{PE} OUTPUT LOAD CIRCUIT

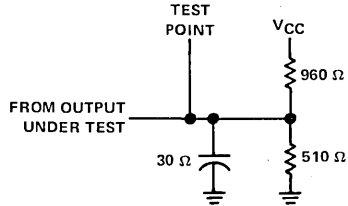
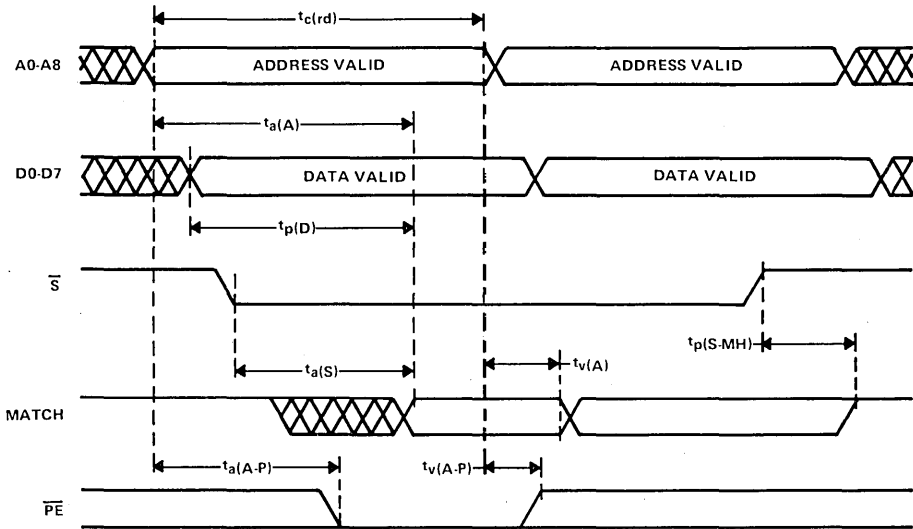


FIGURE 2. MATCH OUTPUT LOAD CIRCUIT

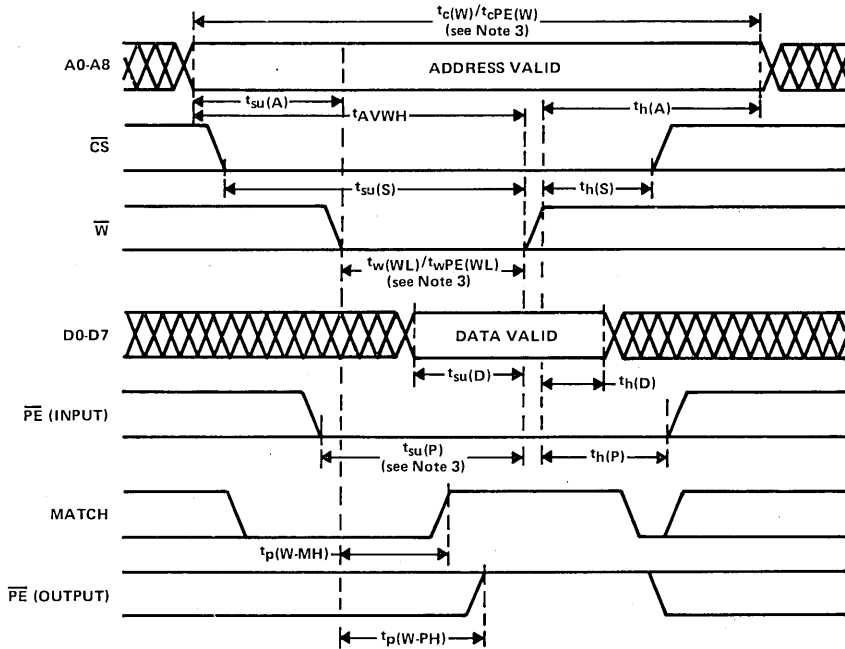
compare cycle timing (see Note 4)



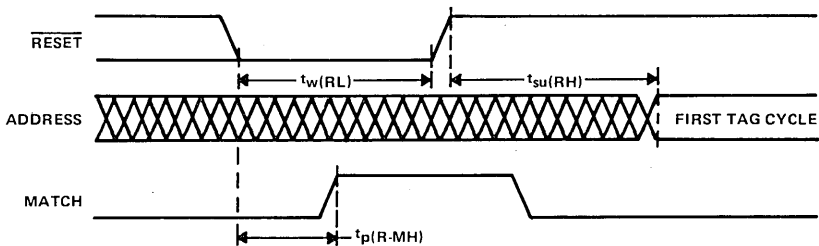
NOTE 4: Input pulse levels are 0 V and 3 V, with rise and fall times of 5 ns. The timing reference levels on the input pulses are 0.8 V and 2.0 V. The timing reference level for output pulses is 1.5 V. See Figures 1 and 2 for output loading.

PARAMETER MEASUREMENT INFORMATION

write cycle timing (see Note 4)



reset cycle timing (see Note 4)



- NOTES: 3. Parameters $t_{wPE}(WL)$ and $t_{su}(P)$ apply only during the write cycle time when writing a parity error, $t_{cPE}(W)$.
 4. Input pulse levels are 0 V and 3 V, with rise and fall times of 5 ns. The timing reference levels on the input pulses are 0.8 V and 2.0 V. The timing reference level for output pulses is 1.5 V. See Figures 1 and 2 for output loading.

2
LSI Devices

TMS4500A DYNAMIC-RAM CONTROLLER

D2674, JANUARY 1982—REVISED AUGUST 1985

- Controls Operation of 8K, 16K, 32K, and 64K Dynamic RAMs
- Creates Static RAM Appearance
- One Package Contains Address Multiplexer, Refresh Control, and Timing Control
- Directly Addresses and Drives Up to 256K Bytes of Memory Without External Drivers
- Operates from Microprocessor Clock
 - No Crystals, Delay Lines, or RC Networks
 - Eliminates Arbitration Delays
- Refresh May Be Internally or Externally Initiated
- Versatile
 - Strap-Selected Refresh Rate
 - Synchronous, Predictable Refresh
 - Selection of Distributed, Transparent, and Cycle-Steal Refresh Modes
 - Interfaces Easily to Popular Microprocessors

- Strap-Selected Wait-State Generation for Microprocessor/Memory Speed Matching
- Ability to Synchronize or Interleave Controller with the Microprocessor System (including Multiple Controllers)
- 3-State Outputs Allow Multiport Memory Configuration
- Performance Ranges of 150 ns, 200 ns, or 250 ns

description

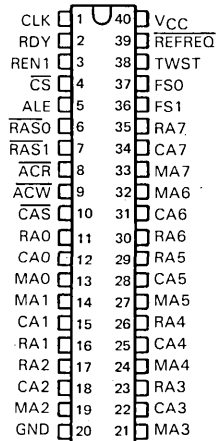
The TMS4500A is a monolithic DRAM system controller designed to provide address multiplexing, timing, control and refresh/access arbitration functions to simplify the interface of dynamic RAMs to microprocessor systems.

The controller contains a 16-bit multiplexer that generates the address lines for the memory device from the 16 system address bits and provides the strobe signals required by the memory to decode the address. An 8-bit refresh counter generates the 256-row addresses required for refresh.

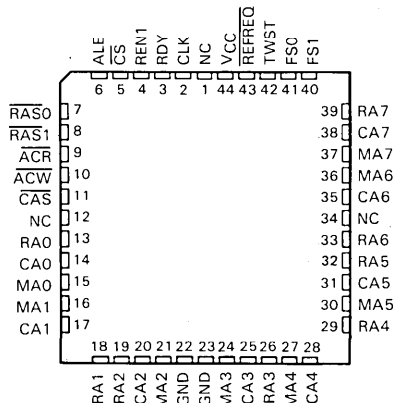
A refresh timer is provided that generates the necessary timing to refresh the dynamic memories and assure data retention.

The TMS4500A also contains refresh/access arbitration circuitry to resolve conflicts between memory access requests and memory refresh cycles. The TMS4500A is offered in a 40-pin, 600-mil dual-in-line plastic package and 44-pin, 650-mil square plastic chip carrier package. It is characterized for operation from 0°C to 70°C.

TMS4500A . . . NL PACKAGE
(TOP VIEW)



TMS4500A . . . FN PACKAGE
(TOP VIEW)



LSI Devices

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

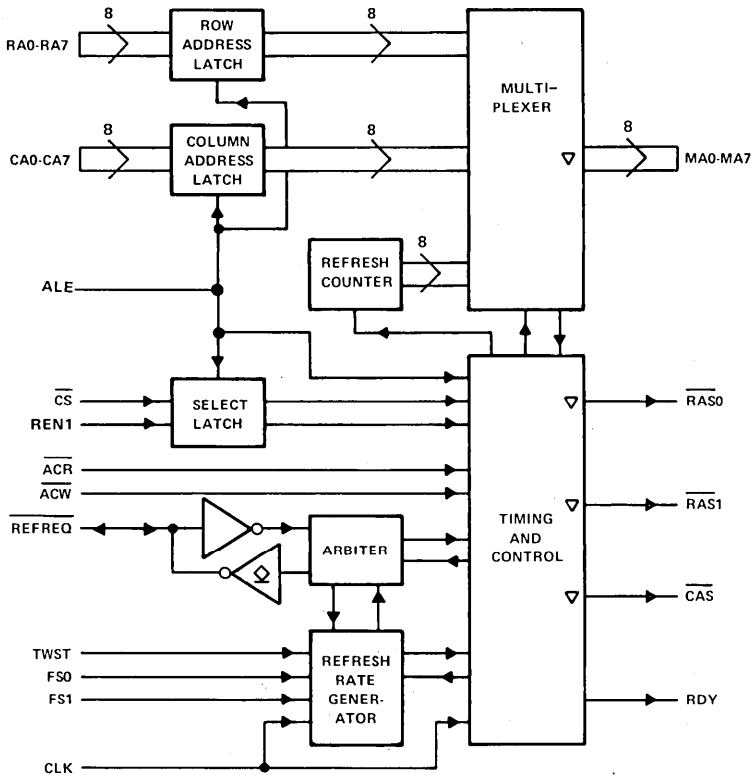


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**TMS4500A
DYNAMIC-RAM CONTROLLER**

BLOCK DIAGRAM



2

LSI Devices

pin descriptions

RA0-RA7	Input	Row Address — These address inputs are used to generate the row address for the multiplexer.
CA0-CA7	Input	Column Address — These address inputs are used to generate the column address for the multiplexer.
MA0-MA7	Output	Memory Address — These three-state outputs are designed to drive the addresses of the dynamic RAM array.
ALE	Input	Address Latch Enable — This input is used to latch the 16 address inputs, CS and REN1. This also initiates an access cycle if chip select is valid. The rising edge (low level to high level) of ALE returns RAS to the high level.
CS	Input	Chip Select — A low on this input enables an access cycle. The trailing edge of ALE latches the chip select input.

pin descriptions (continued)

REN1	Input	RAS Enable 1 — This input is used to select one of two banks of RAM via the $\overline{\text{RAS0}}$ and $\overline{\text{RAS1}}$ outputs when chip select is present. When it is low, $\overline{\text{RAS0}}$ is selected; when it is high, $\overline{\text{RAS1}}$ is selected.
$\overline{\text{ACR}}$, ACW	Input	Access Control, Read; Access Control, Write — A low on either of these inputs causes the column address to appear on MA0—MA7 and the column address strobe. The rising edge of $\overline{\text{ACR}}$ or ACW terminates the cycle by ending $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ strobes. When $\overline{\text{ACR}}$ and ACW are both low, MA0—MA7, $\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$, and $\overline{\text{CAS}}$ go into a high-impedance (floating) state.
CLK	Input	System Clock — This input provides the master timing to generate refresh cycle timings and refresh rate. Refresh rate is determined by the TWST, FS1, FS0 inputs.
$\overline{\text{REFREQ}}$	Input/Output	Refresh Request — (This input should be driven by an open-collector output.) On input, a low-going edge initiates a refresh cycle and will cause the internal refresh timer to be reset on the next falling edge of the CLK. As an output, a low-going edge signals an internal refresh request and that the refresh timer will be reset on the next low-going edge of CLK. $\overline{\text{REFREQ}}$ will remain low until the refresh cycle in progress and the current refresh address is present on MA0—MA7. (Note: $\overline{\text{REFREQ}}$ contains an internal pull-up resistor with a nominal resistance of 10 kilohms.)
$\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$	Output	Row Address Strobe — These three-state outputs are used to latch the row address into the bank of DRAMs selected by REN1. On refresh both signals are driven.
$\overline{\text{CAS}}$	Output	Column Address Strobe — This three-state output is used to latch the column address into the DRAM array.
RDY	Output	Ready — This totem-pole output synchronizes memories that are too slow to guarantee microprocessor access time requirements. This output is also used to inhibit access cycles during refresh when in cycle-steal mode.
TWST	Input	Timing/Wait Strap — A high on this input indicates a wait state should be added to each memory cycle. In addition it is used in conjunction with FS0 and FS1 to determine refresh rate and timing.
FS0, FS1	Input	Frequency Select 0; Frequency Select 1 — These are strap inputs to select Mode and Frequency of operation as shown in Table 1.

TMS4500A DYNAMIC-RAM CONTROLLER

TABLE 1. STRAP CONFIGURATION

STRAP INPUT MODES			WAIT STATES FOR MEMORY ACCESS	REFRESH RATE	MINIMUM CLK FREQ. (MHz)	REFRESH FREQ. (kHz)	CLOCK FOR EACH FOR EACH REFRESH
TWST	FS1	FS0					
L	L	L [†]	0	EXTERNAL	—	REFREQ	4
L	L	H	0	CLK + 31	1,984	64-95 [‡]	3
L	H	L	0	CLK + 46	2,944	64-85 [‡]	3
L	H	H	0	CLK + 61	3,904	64-82 [§]	4
H	L	L	1	CLK + 46	2,944	64-85 [‡]	3
H	L	H	1	CLK + 61	3,904	64-80 [‡]	4
H	H	L	1	CLK + 76	4,864	64-77 [‡]	4
H	H	H	1	CLK + 91	5,824	64-88 [†]	4

[†] This strap configuration resets the Refresh Timer circuitry.

[‡] The highest frequency in the refresh frequency column is the frequency that is produced if the minimum CLK frequency of the next select state is used.

[§] The highest frequency in the refresh column is the refresh frequency if the CLK frequency is 5 MHz.

[†] The highest frequency in the refresh column is the refresh frequency if the CLK frequency is 8 MHz.

2

LSI Devices

functional description

TMS4500A consists of six basic blocks; address and select latches, refresh rate generator, refresh counter, the multiplexer, the arbiter, and timing and control block.

address and select latches

The address and select latches allow the DRAM controller to be used in systems that multiplex address and data on the same lines without external latches. The row address latches are transparent, meaning that while ALE is high, the output at MA0—MA7 follows the inputs RAO—RA7.

refresh rate generator

The refresh rate generator is a counter that indicates to the arbiter that it is time for a refresh cycle. The counter divides the clock frequency according to the configuration straps as shown in Table 1. The counter is reset when a refresh cycle is requested or when TWST, FS1 and FS0 are low. The configuration straps allow the matching of memories to the system access time.

Upon Power-Up it is necessary to provide a reset signal by driving all three straps to the controller low to initialize internal counters. A system's low-active, power-on reset (RESET) can be used to accomplish this by connecting it to those straps that are desired high during operation. During this reset period, at least four clock cycles should occur.

refresh counter

The refresh counter contains the address of the row to be refreshed. The counter is decremented after each refresh cycle. [A low-to-high transition on TWST sets the refresh counter to FF₁₆ (255₁₀).]

multiplexer

The multiplexer provides the DRAM array with row, column, and refresh addresses at the proper times. Its inputs are the address latches and the refresh counter. The outputs provide up to 16 multiplexed addresses on eight lines.

arbiter

The arbiter provides two operational cycles: access and refresh. The arbiter resolves conflicts between cycle requests and cycles in execution, and schedules the inhibited cycle when used in cycle-steal mode.

timing and control block

The timing and control block executes the operational cycle at the request of the arbiter. It provides the DRAM array with RAS and CAS signals. It provides the CPU with a RDY signal. It controls the multiplexer during all cycles. It resets the refresh rate generator and decrements the refresh counter during refresh cycles.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	- 1.5 V to 7 V
Input voltage range (any input)	- 1.5 V to 7 V
Continuous power dissipation	1.2 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	- 65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to the ground terminal.

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level input voltage, V_{IH}		2.4		6	V
Low-level input voltage, V_{IL}		-1‡		0.8	V
High-level output current, I_{OH}				-1	mA
Low-level output current, I_{OL}				4	mA
Short-circuit output current, I_{OS} §				-50	mA
Operating free-air temperature, T_A		0		70	°C

‡ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

§ Not more than one output should be shorted at a time.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
V_{OH}	High-level output voltage	MA0-MA7, RDY	$V_{CC} = 4.5 \text{ V}, I_{OH} = -1 \text{ mA}$			2.4	V	
		RAS0, RAS1, CAS				2.7		
		REFREQ				2.4		
V_{OL}	Low-level output voltage	$V_{CC} = 4.5 \text{ V}, I_{OL} = 4 \text{ mA}$				0.4	V	
I_{IH}	High-level input current except REFREQ	$V_I = 5.5 \text{ V}$				10	µA	
I_{IL}	Low-level input current	REFREQ	$V_I = 0$				-1.25	mA
		All others					-10	µA
I_{OZ}	Off-state output current	$V_{CC} = 5.5 \text{ V}, V_O = 0 \text{ to } 4.5 \text{ V}$				±50	µA	
I_{CC}	Operating supply current	$T_A = 0^\circ\text{C}$				100	140	mA
C_i	Input capacitance	$V_I = 0, f = 1 \text{ MHz}$				5	pF	
C_o	Output capacitance	$V_O = 0, f = 1 \text{ MHz}$				6	pF	

† All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

TMS4500A DYNAMIC-RAM CONTROLLER

timing requirements over recommended supply voltage range and operating free-air temperature (unless otherwise noted)

PARAMETER		TMS4500A-15		TMS4500A-20		TMS4500A-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(C)}$	CLK cycle time	100		120		140		ns
$t_{w(CH)}$	CLK high pulse duration	40		40		40		
$t_{w(CL)}$	CLK low pulse duration	40		45		45		
t_t	Transition time, all inputs		50		50		50	
t_{AEL-CL}	Time delay, ALE low to CLK starting low (see Note 1)	10		10		15		
t_{CL-AEL}	Time delay, CLK low to ALE starting low (see Note 1)	10		10		15		
t_{CL-AEH}	Time delay, CLK low to ALE starting high (see Note 2)	15		20		20		
$t_{w(AEH)}$	Pulse duration, ALE high	50		60		60		
t_{AV-AEL}	Time delay, address REN1, \overline{CS} valid to ALE low	5		10		15		
t_{AEL-AX}	Time delay, ALE low to address not valid	10		10		10		
$t_{AEL-ACL}$	Time delay, ALE low to \overline{ACX} low (see Notes 3, 4, 5, and 6)	$t_{h(RA)} + 30$		$t_{h(RA)} + 40$		$t_{h(RA)} + 50$		
t_{ACH-CL}	Time delay, \overline{ACX} high to CLK low (see Notes 3 and 7)	20		20		20		
t_{ACL-CH}	Time delay, \overline{ACX} low to CLK starting high (to remove RDY)	30		30		30		
t_{RQL-CL}	Time delay, \overline{REFREQ} low to CLK starting low (see Note 8)	20		20		20		
$t_{w(RQL)}$	Pulse duration, \overline{REFREQ} low	20		20		20		
$t_{w(ACL)}$	\overline{ACX} low duration (see Note 9)	110		140		175		

- NOTES:
1. Coincidence of the trailing edge of CLK and the trailing edge of ALE should be avoided as the refresh/access occurs on the trailing CLK edge. A trailing edge of CLK should occur during the interval from \overline{ACX} high to ALE low.
 2. If ALE rises before \overline{ACX} and a refresh request is present, the falling edge of CLK after t_{CL-AEH} will output the refresh address to MA0-MA7 and initiate a refresh cycle.
 3. These specifications relate to system timing and do not directly reflect device performance.
 4. On the access grant cycle following refresh, the occurrence of \overline{CAS} low depends on the relative occurrence of ALE low to \overline{ACX} low. If \overline{ACX} occurs prior to or coincident with ALE then \overline{CAS} is timed from the CLK high transition that causes \overline{RAS} low. If \overline{ACX} occurs 20 ns or more after ALE then \overline{CAS} is timed from the CLK low transition following the CLK high transition causing \overline{RAS} low.
 5. For maximum speed access (internal delays on both access and access grant cycles), \overline{ACX} should occur prior to or coincident with ALE.
 6. $t_{h(RA)}$ is the dynamic memory row address hold time. \overline{ACX} should follow ALE by t_{AEL-CL} in systems where the required $t_{h(RA)}$ is greater than $t_{REL-MAX}$ minimum.
 7. The minimum of 20 ns is specified to ensure arbitration will occur on falling CLK edge, t_{ACH-CL} also affects precharge time such that the minimum t_{ACH-CL} should be equal or greater than: $t_{w(RH)} - t_{w(CL)} + 30$ ns (for a cycle where \overline{ACX} high occurs prior to ALE high) where $t_{w(RH)}$ is the DRAM \overline{RAS} precharge time.
 8. This parameter is necessary only if refresh arbitration is to occur on this low-going CLK edge (in systems where refresh is synchronized to external events).
 9. The specification $t_{w(ACL)}$ is designed to allow a \overline{CAS} pulse. This assures normal operation of the device in testing and system operation.

2

LSI Devices

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 1)

PARAMETER	TEST CONDITIONS	TMS4500A-15		TMS4500A-20		TMS4500A-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{AEL-REL}	Time delay, ALE low to RAS starting low		35		40		50	ns
t _{RAV-MAV}	Time delay, row address valid to memory address valid		45		50		60	
t _{AEH-MAV}	Time delay, ALE high to valid memory address		65		75		90	
t _{AEL-RYL}	Time delay, ALE to RDY starting low (TWST = 1 or refresh in progress)		40		40		40	
t _{AEL-CEL}	Time delay, ALE low to $\overline{\text{CAS}}$ starting low (see Note 10)	60	150	70	200	80	250	
t _{AEH-REH}	Time delay, ALE high to $\overline{\text{RAS}}$ starting high		30		30		40	
t _{ACL-MAX}	Row address valid after $\overline{\text{ACX}}$ low		15		20		25	
t _{MAV-CEL}	Time delay, memory address valid to $\overline{\text{CAS}}$ starting low		0		0		0	
t _{ACL-CEL}	Time delay, $\overline{\text{ACX}}$ low to $\overline{\text{CAS}}$ starting low (see Note 10)	40	100	45	130	50	165	
t _{ACH-REH}	Time delay, $\overline{\text{ACX}}$ to $\overline{\text{RAS}}$ starting high		30		40		50	
t _{ACH-CEH}	Time delay, $\overline{\text{ACX}}$ high to $\overline{\text{CAS}}$ starting high	5	30	10	40	15	50	
t _{ACH-MAX}	Column address valid after $\overline{\text{ACX}}$ high		10		15		15	
t _{CH-RYH}	Time delay, CLK high to RDY starting high (after $\overline{\text{ACX}}$ low) (see Note 11)		40		45		60	
t _{RFL-RFL}	Time delay, REFREQ external till supported by REFREQ internal		30		35		35	
t _{CH-RFL}	Time delay, CLK high till REFREQ internal starting low		30		35		45	
t _{CL-MAV}	Time delay, CLK low till refresh address valid		75		100		125	
t _{CH-RRL}	Time delay, CLK high till refresh RAS starting low	10	50	15	60	20	80	
t _{MAV-RRL}	Time delay, refresh address valid till refresh RAS low		5		5		5	
t _{CL-RFH}	Time delay, CLK low to REFREQ starting high (3 cycle refresh)		50		55		75	
t _{CH-RFH}	Time delay, CLK high to REFREQ starting high (4 cycle refresh)		50		55		75	
t _{CH-RRH}	Time delay, CLK high to refresh RAS starting high	5	35	10	45	10	60	
t _{CH-MAX}	Refresh address valid after CLK high		15		20		25	

- NOTES: 10. The falling edge of $\overline{\text{CAS}}$ occurs when both ALE low to $\overline{\text{CAS}}$ low time delay (t_{AEL-CEL}) and $\overline{\text{ACX}}$ low to $\overline{\text{CAS}}$ low time delay (t_{ACL-CEL}) have elapsed, i.e., if $\overline{\text{ACX}}$ goes low prior to (t_{AEL-CEL} - t_{ACL-CEL}) after the falling edge of ALE, the falling edge of $\overline{\text{CAS}}$ is measured from the falling edge of ALE (t_{AEL-CEL}). Otherwise, the access time increases and the falling edge of $\overline{\text{CAS}}$ is measured from the falling edge of $\overline{\text{ACX}}$ (t_{ACL-CEL}).
11. RDY returns high on the rising edge of CLK. If TWST = 0, then on an access grant cycle RDY goes high on the same edge that causes access RAS low. If TWST = 1, then RDY goes to the high level on the first rising CLK edge after $\overline{\text{ACX}}$ goes low on access cycles and on the next rising edge after the edge that causes access RAS low on access grant cycles (assuming $\overline{\text{ACX}}$ low).

2
LSI Devices

TMS4500A DYNAMIC-RAM CONTROLLER

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 1) (continued)

PARAMETER	TEST CONDITIONS	TMS4500A-15		TMS4500A-20		TMS4500A-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{CH-REL} Time delay, CLK high till access R _{AS} starting low	C _L = 160 pF	60		70		95		ns
t _{CL-CEL} Time delay, CLK low to access C _{AS} starting low (see Note 12)		125		140		185		
t _{CL-MAX} Row address valid after CLK low		25		30		40		
t _{REL-MAX} Row address valid after R _{AS} low		25		30		35		
t _{AEH-MAX} Column address valid after ALE high	C _L = 160 pF	10		15		20		
t _{dis} Output disable time (3-state outputs)		100		125		165		
t _{en} Output enable time (3-state outputs)		75		80		105		
t _{CAV-CEL} Time delay, column address valid to C _{AS} starting low after refresh		0		0		0		
t _{CH-CEL} Time delay, CLK high to access C _{AS} starting low (see Note 12)		180		200		235		
t _{ACL-CL} ACX low to CLK starting low		C _L = 40 pF	25		35		45	
t _{ACL-RYH} ACX low to RDY starting high	C _L = 40 pF	40		50		60		
t _{CL-ACL} CLK low to ACX starting low	C _L = 40 pF	0		0		0		
t _{t(CEL)} C _{AS} fall time	C _L = 320 pF	15		20		25		
t _{t(CEH)} C _{AS} rise time		30		35		45		
t _{t(REL)} R _{AS} fall time		15		20		25		
t _{t(REH)} R _{AS} rise time	C _L = 160 pF	15		20		25		
t _{t(MAV)} Address transition time		20		20		25		
t _{t(RYL)} RDY fall time	C _L = 40 pF	10		15		20		
t _{t(RYH)} RDY rise time		20		25		35		

NOTE 12: On the access grant cycle following refresh, the occurrence of C_{AS} low depends on the relative occurrence of ALE low to ACX low. If ACX occurs prior to or coincident with ALE then C_{AS} is timed from the CLK high transition that causes R_{AS} low. If ACX occurs 20 ns or more after ALE then C_{AS} is timed from the CLK low transition following the CLK high transition causing R_{AS} low. (See Refresh Cycle Timing Diagram)

PARAMETER MEASUREMENT INFORMATION

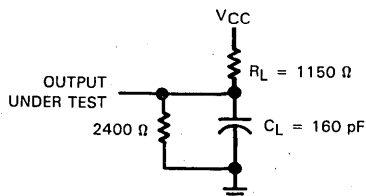
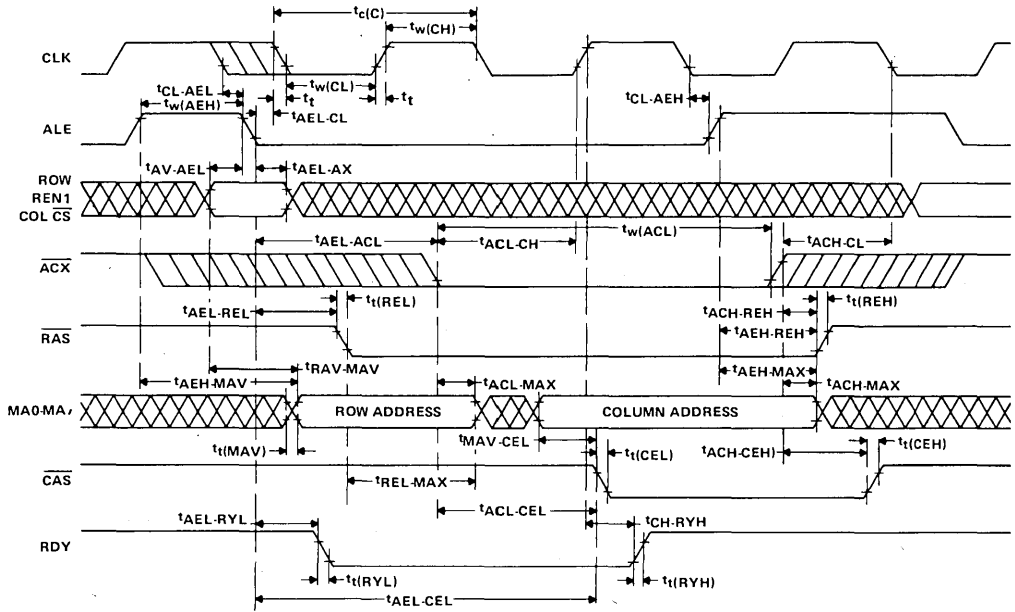
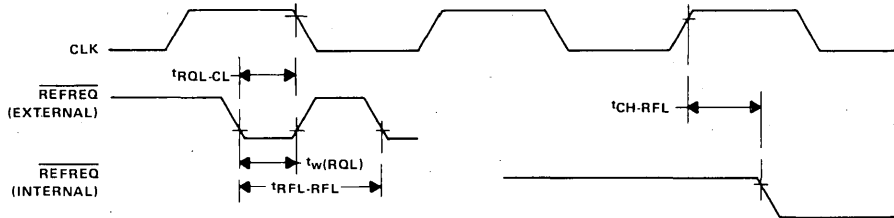


FIGURE 1 - LOAD CIRCUIT

access cycle timing



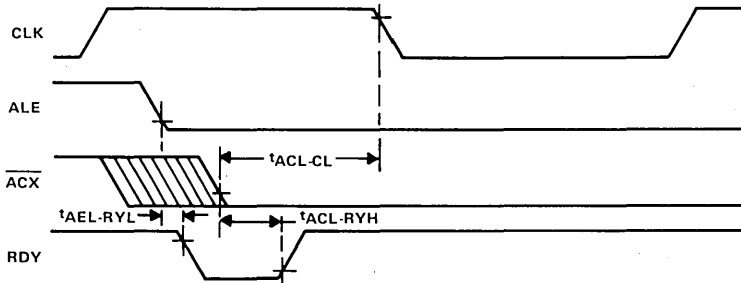
refresh request timing



2
LSI Devices

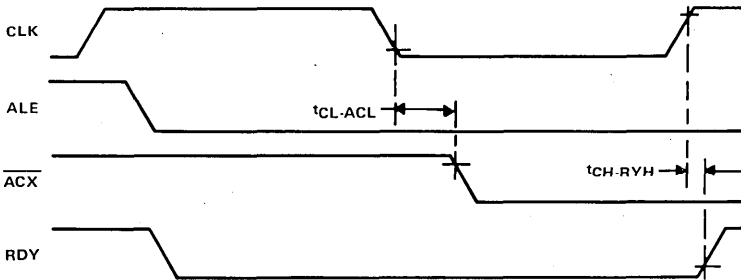
**TMS4500A
DYNAMIC-RAM CONTROLLER**

ready timing (ACX during CLK high) (see notes 13 thru 16)



RDY starting high is timed from \overline{ACX} low ($t_{ACL-RYH}$) for the condition \overline{ACX} going low while CLK high.

ready timing (ACX during CLK low) (see notes 13 thru 16)



RDY starting high is timed from CLK high (t_{CH-RYH}) for the condition ACX going low while CLK low.

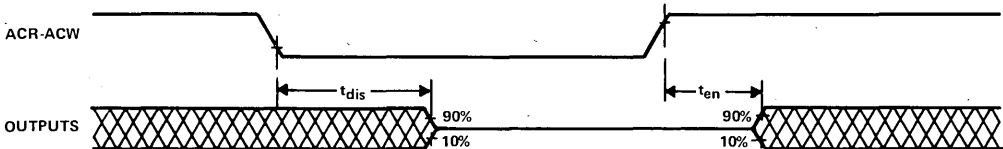
NOTES: 13. For RDY high transition (during normal access) to be timed from the rising edge of CLK, \overline{ACX} must occur t_{CL-ACL} after the falling edge of CLK.

14. For \overline{ACX} prior to the falling edge of CLK by t_{ACL-CL} , the RDY high transition will be $t_{ACL-RYH}$.

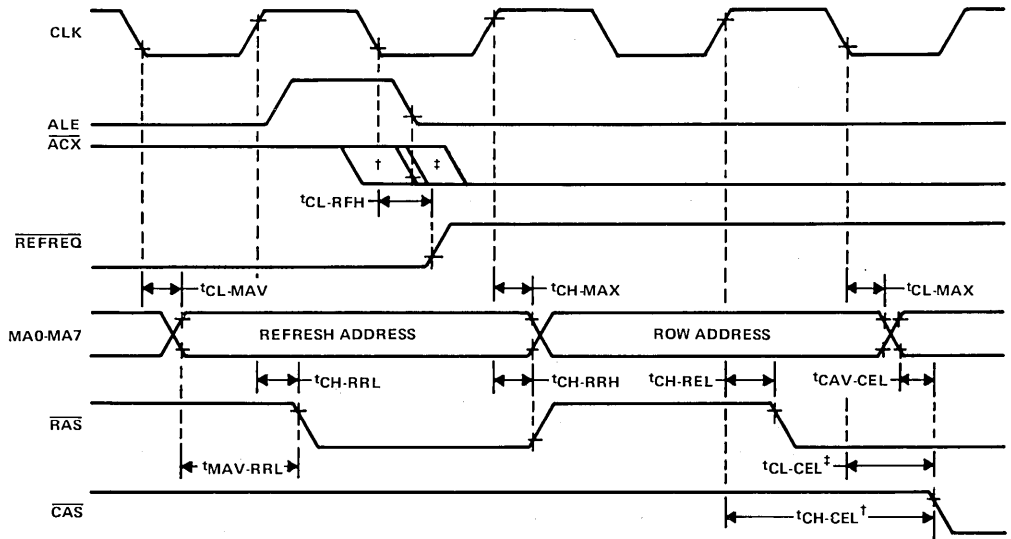
15. t_{ACL-CL} is a limiting parameter for control of RDY to be dependent upon \overline{ACX} low.

16. During the interval for $t_{ACL-CL} < \text{MINIMUM}$ to $t_{CL-ACL} > \text{MINIMUM}$, the control of RDY may vary between the rising clock edge or falling edge of \overline{ACX} .

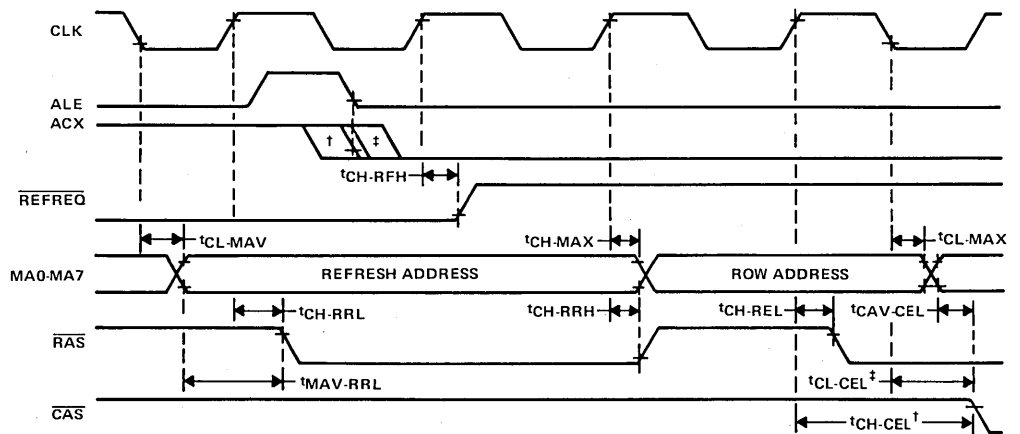
output 3-state timing



refresh cycle timing (three-cycle)



refresh cycle timing (four-cycle)



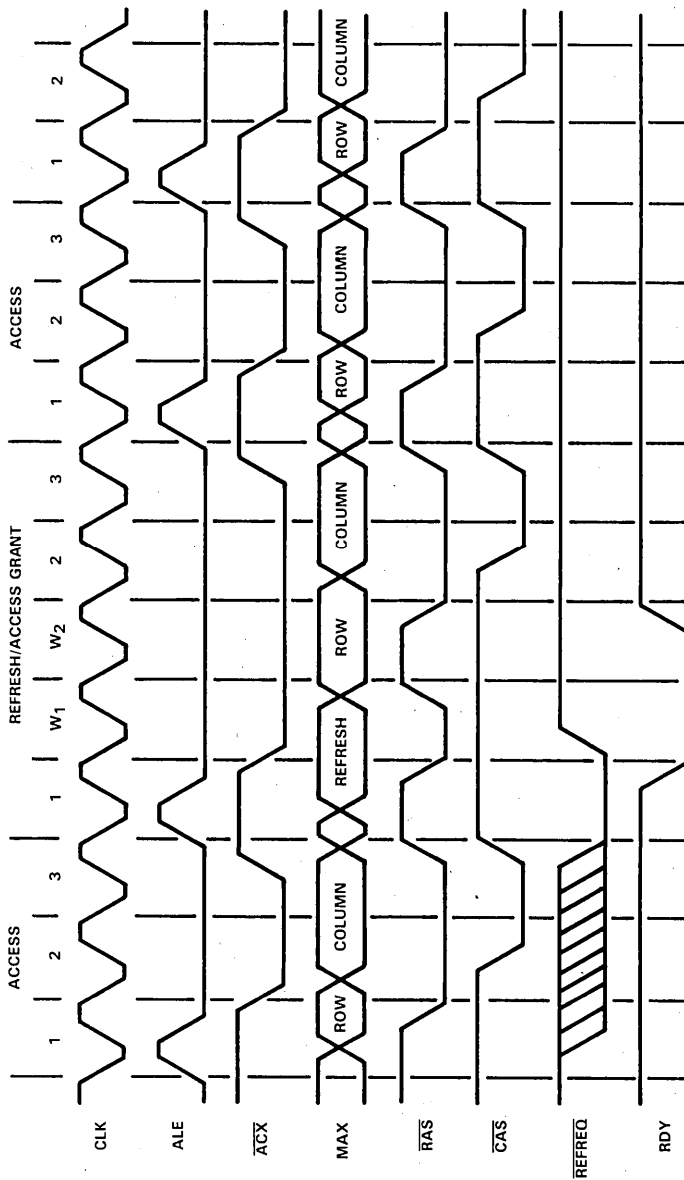
[†] On access grant cycle following refresh, \overline{CAS} low and address multiplexing are timed from CLK high transition (t_{CH-CEL}) if \overline{ACX} low occurs prior to or coincident with the falling edge of ALE.

[‡] On access grant cycle following refresh, \overline{CAS} low and address multiplexing are timed from CLK low transition (t_{CL-CEL}) if \overline{ACX} low occurs 20 ns or more after the falling edge of ALE.

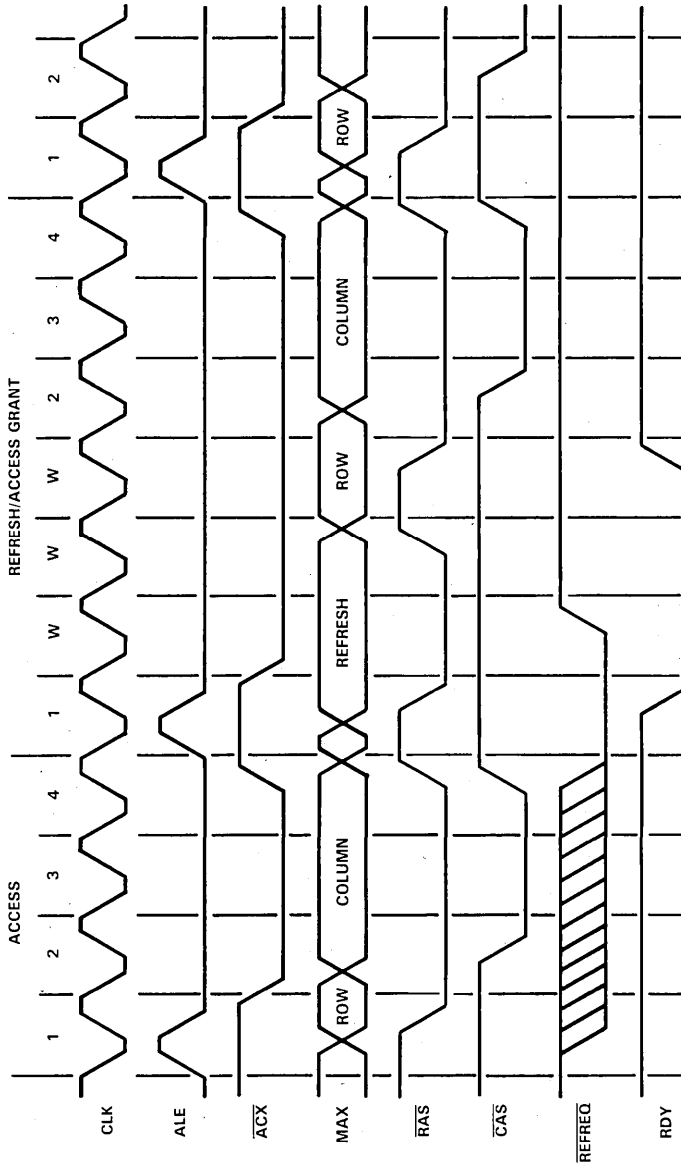
2
LSI Devices

**TMS4500A
DYNAMIC-RAM CONTROLLER**

typical access/refresh/access cycle
(three-cycle, TWST is low)

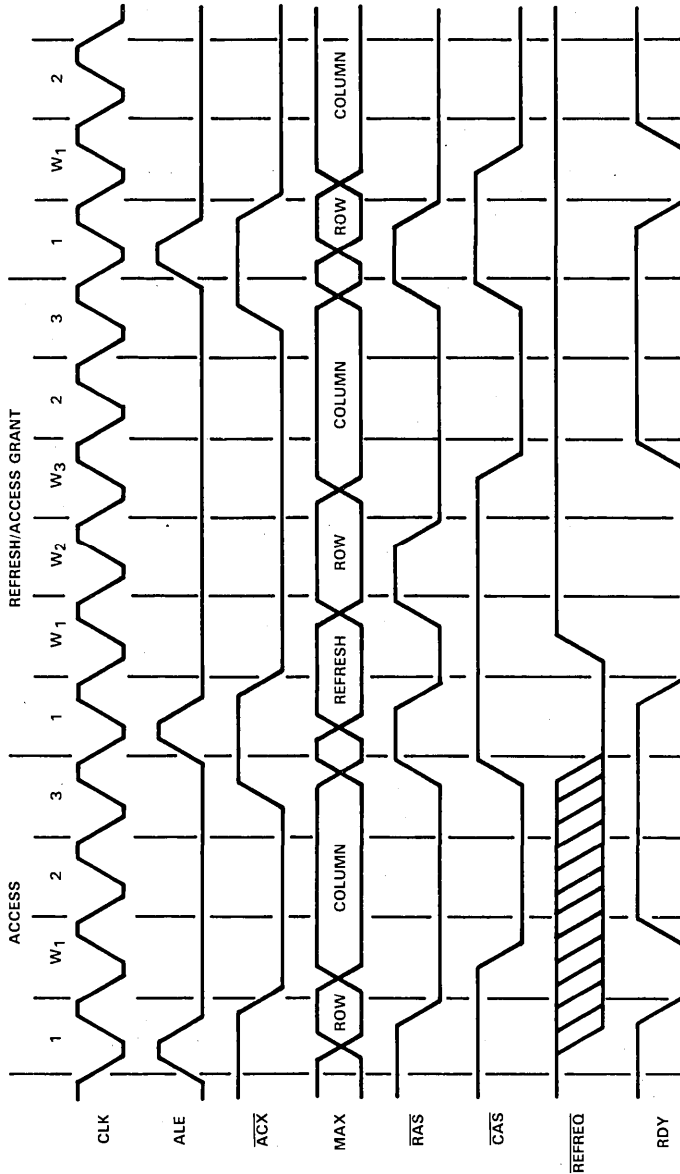


typical access/refresh/access cycle
(four-cycle, TWST is low)

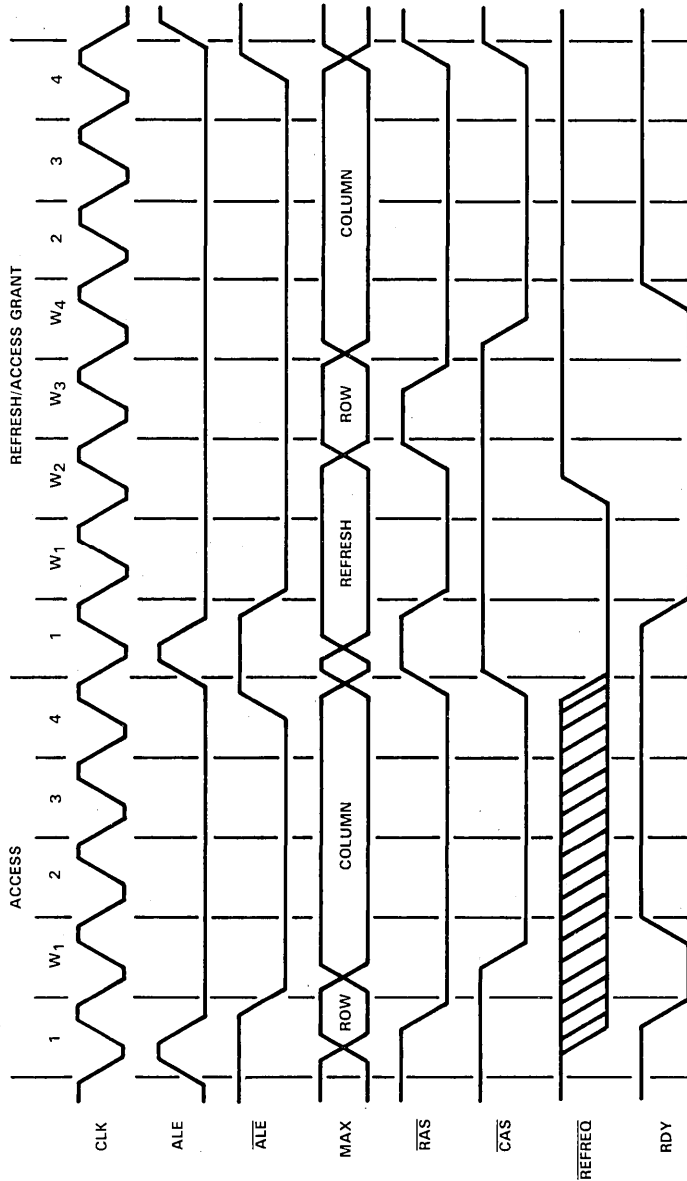


**TMS4500A
DYNAMIC-RAM CONTROLLER**

typical access/refresh/access cycle
(three-cycle, TWST is high)



typical access/refresh/access cycle
(four-cycle, TWST is high)



General Information

1

Numerical Index
Glossary
Explanation of Function Tables
Parameter Measurement Information
Functional Index

LSI Devices

2

Application Reports

3

Advanced Schottky Family
Error Detection and Correction
Memory Mapping
Bit-Slice Processor 8-Bit Family
Excerpt — SN74AS888, SN74AS890
Bit-Slice Processor User's Guide

Mechanical Data

4



Advanced Schottky Family



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Advanced Schottky Family (ALS/AS) Application

Contents

	<i>Title</i>	<i>Page</i>
INTRODUCTION TO ADVANCED SCHOTTKY FAMILY		3-9
Speed-Power Slots Filled By Advanced Schottky TTL		3-9
Additional Advantages Offered by 'ALS and 'AS Devices		3-9
Concepts of Defining 'ALS and 'AS		3-10
Compatibility With Other TTL		3-10
Fanout		3-10
Using the Schottky Barrier-Diode		3-10
Analysis of Schottky-Clamped Transistor		3-10
Analysis of 'ALS and 'AS NAND Gates		3-13
Circuit Parameters		3-16
Transfer Characteristics		3-16
Input Characteristics		3-17
Low-Level Input Current		3-17
Input Clamping Diode Test		3-18
High-Level Input Current		3-18
Input Breakdown Test		3-18
Output Characteristics		3-18
High-Level Output Characteristics		3-18
Low-Level Output Characteristics		3-19
Switching Speed		3-19
DC Noise Margins		3-20
Specified Logic Levels and Thresholds		3-22
Noise Rejection		3-22
GUIDELINES FOR SERIES 'ALS/'AS TTL SYSTEM DESIGN		3-24
Power Supply Regulation		3-25
Supply Voltage Ripple		3-27
Noise Considerations		3-28
Noise Types and Control Methods		3-28
Shielding		3-29
Grounding and Decoupling		3-29
Cross Talk		3-34
Back-Panel Interconnections		3-34
Printed Circuit Card Conductors		3-36
Transmission-Line Driving Reflections		3-37
APPENDIXES		
A Normalized Load Factors		3-45
B Letter Symbols, Terms, and Definitions		3-46

List of Illustrations

<i>Figure</i>	<i>Title</i>	<i>Page</i>
1	Speed-Power Relationships of Digital Integrated Circuits	3-10
2	Series 54/74 TTL Family Compatible Levels Showing DC Noise Margins	3-11
3	Fanout Capability	3-11
4	Baker Clamp	3-11
5	Schottky Clamped-Transistor	3-11
6	Schottky Barrier-Diode	3-12
7	Schottky Barrier-Diode Energy Diagrams	3-12
8	Metal-N Diode Current-Voltage Characteristics	3-12
9	Difference Between P-N and Schottky Barrier-Diodes	3-13
10	Standard Process ('LS/'S)	3-13
11	Advanced Process ('ALS/'AS)	3-13
12	'ALS00A NAND Gate Schematic	3-14
13	'AS00 NAND Gate Schematic	3-15
14	Input Voltage vs Output Voltage 'ALS/'AS	3-16
15	Input Current vs Input Voltage for TTL Families	3-17
16	Low-Level Input Current vs High-Level Input Voltage	3-18
17	DC Equivalent Input Circuit for Series 'ALS Gates	3-18
18	Equivalent Output Circuit for 'ALS/'AS Gates	3-19
19	High-Level Output Voltage vs High-Level Output Current	3-19
20	Low-Level Output Circuit for 'ALS/'AS Gates	3-20
21	Low-Level Output Voltage vs Low-Level Output Current	3-20
22	High- to Low-Level Propagation Delay vs Load Capacitance	3-21
23	Low- to High-Level Propagation Delay vs Load Capacitance	3-21
24	Power Dissipation per Gate vs Frequency	3-22
25	Stray Coupling Capacitance	3-23
26	Evaluations of Gate Response to Fast Input Pulses	3-23
27	Theoretical Required Pulse Width vs Pulse Amplitude for 'ALS and 'AS Inputs	3-24
28	Parameter Measurement Information	3-25
29	Effect of Source Impedance on Input Noise	3-28
30	Spurious Output Produced by Supply Voltage Ripple	3-28
31	Effect of Ground Noise on Noise Margin	3-28
32	Typical Logic Circuit with Noisy Input	3-28
33	Diagram Representing a Gate Driving a Transmission Line	3-29
34	Noise Generation Caused by Poor Transmission-Line Return	3-29
35	Ideal Transmission-Line Current Handling	3-30
36	Circuit with Effective Capacitive Loading	3-30
37	Supply Current Transient Comparisons	3-31
38	Transmission-Line Power Buses	3-33
39	Capacitive Storage Supply Voltage System	3-33
40	Commonly Used Power Distribution and Decoupling System	3-33
41	Equivalent Circuit for Sending Line	3-34
42	Equivalent Circuit for Cross Talk	3-34
43	Capacitive Cross Talk Between Two Signal Lines	3-35
44	Coupling Impedances Involved in Cross Talk	3-35
45	Equivalent Cross-Talk Network	3-35
46	Microstrip Line	3-36
47	Strip Line	3-36
48	Line Spacing Versus Cross-Talk Constant	3-37
49	TTL Bergeron Diagram	3-37
50	'ALS/'AS Driving Twisted Pair	3-37

List of Illustrations (Continued)

<i>Figure</i>	<i>Title</i>	<i>Page</i>
51	'AS -ve Transition Bergeron Diagram	3-38
52	'AS -ve Voltage/Time Plot	3-38
53	'AS +ve Transition Bergeron Diagram	3-39
54	'AS +ve Voltage/Time Plot	3-39
55	'ALS -ve Transition Bergeron Diagram	3-40
56	'ALS -ve Voltage/Time Plot	3-40
57	'ALS +ve Transition Bergeron Diagram	3-41
58	'ALS +ve Voltage/Time Plot	3-41
59	Oscilloscope Photograph of 'AS00 -ve Transition Using 50-Ohm Line	3-42
60	Oscilloscope Photograph of 'AS00 +ve Transition Using 50-Ohm Line	3-42
61	Oscilloscope Photograph of 'AS00 -ve Transition Using 25-Ohm Line	3-42
62	Oscilloscope Photograph of 'AS00 +ve Transition Using 25-Ohm Line	3-42
63	Oscilloscope Photograph of 'ALS00A -ve Transition Using 50-Ohm Line	3-42
64	Oscilloscope Photograph of 'ALS00A +ve Transition Using 50-Ohm Line	3-42
65	Oscilloscope Photograph of 'ALS00A -ve Transition Using 25-Ohm Line	3-43
66	Oscilloscope Photograph of 'ALS00A +ve Transition Using 25-Ohm Line	3-43

List of Tables

<i>Table</i>	<i>Title</i>	<i>Page</i>
1	Typical Performance Characteristics by TTL Series	3-10
2	Worst-Case Output Parameters	3-22
3	Guidelines for Systems Design for Advanced Schottky TTL	3-26
4	Guidelines for Printed Circuit Board Layout Advanced Schottky TTL	3-26
5	Guidelines for General Usage of Advanced Schottky TTL	3-27
6	Guidelines for Gates and Flip-Flops Using Advanced Schottky TTL	3-27
7	Typical Impedance of Microstrip Lines	3-36
8	Typical Impedance of Strip Lines	3-36
A-1	Normalized Input Currents	3-45
A-2	Fanout Capability	3-46

INTRODUCTION

The purpose of this Application Report is to assist the designers of high-performance digital logic systems in the use of the new series of Advanced Schottky-clamped* TTL integrated circuits.

Detailed electrical characteristics of these devices are provided and, if available, tables have been included that compare specific parameters of the devices with those of other logic families. In addition, interfamily information is provided to allow system designers to mix logic families in the same circuit. This allows the designer to use the relative merits of each logic family in high performance state-of-the-art designs.

The major subject areas covered in this Application Report are as follows:

- Advanced Schottky process
- Fanouts
- Transfer characteristics
- Input and output parameters
- Speed and power information
- Noise margins
- Power supply considerations
- Noise sources and their abatement
- Back panel and printed circuit wiring guidelines
- Line driving and receiving

INTRODUCTION TO ADVANCED SCHOTTKY-CLAMPED TTL

Series 54/74 transistor-transistor logic (TTL) has, since its introduction in 1965, become the most popular digital integrated circuit logic family ever offered. Its popularity has allowed the development of high-volume production techniques which have made it the most economical approach to the implementation of major portions of medium-to-high performance digital logic systems. These systems range from simple decision making to highly complex real-time computer installations that handle worldwide data processing.

The proliferation of and economical impact of these digital logic systems has created a demand for constant improvement in efficiency. In response to demand, Texas Instruments examined the advantages gained by Schottky clamping. An increase in speed and performance was discovered in the use of Schottky barrier-diode clamping. The process was patented in the United States and the Schottky series 54S/74S catalog parts were made available in the early 1970s. A series 54LS/74LS was introduced later. The series 54LS/74LS was slower than the 54S/74S series but had a much lower power consumption.

*Integrated Schottky-Barrier-diode-clamped transistor is patented by Texas Instruments Incorporated, U.S. Patent Number 3,463,975.

Recent innovations in integrated circuit design have made it possible to develop two new families: the Advanced Schottky (54AS/74AS) series and the Advanced Low-Power Schottky (54ALS/74ALS) series. The 'ALS and 'AS series provide considerable higher speeds than the 'LS and 'S series, respectively. The 'ALS series offers a substantial reduction in power consumption over the 'LS series, and the 'AS series offers a substantial reduction in power consumption over the 'S series. The 'ALS/'AS series is pin-to-pin compatible with the 'LS/'S series.

SPEED-POWER SLOTS FILLED BY 'ALS AND 'AS TTL

Digital integrated circuits have historically been characterized for both speed and power. The series 54S/74S devices contain 19 mW NAND gates and 125-MHz flip-flops and the series 54LS/74LS devices contain 2-mW NAND gates and 45-MHz flip-flops. Either of these logic families could be used to design a 2-MHz system, therefore categorization strictly on the basis of power and speed is inconclusive with respect to system efficiency. To provide a means of measuring the overall circuit efficiency and performance, a speed-power product efficiency index for integrated circuits was developed. The rating of an integrated circuit is obtained by multiplying the gate propagation delay by the gate power dissipation.

Table 1 provides propagation delay times, power dissipation, and speed-power product for the Texas Instruments TTL series. In addition, it provides flip-flop frequency for each family as an indicator of system performance. The speed-power product rating system (measured in picojoules) is divided into circuits where speed is the prime factor and circuits where low-power is the prime factor. The 'ALS series speed-power product is approximately 4 times less than that of the 'LS series and the 'AS series speed-power product is approximately 4 times less than the 'S series. Figure 1 is a graphic analysis of the speed-power points for the various TTL families.

ADDITIONAL ADVANTAGES OFFERED BY 'ALS AND 'AS DEVICES

The 'ALS and 'AS devices offer the following additional advantages:

1. TTL compatible with 54/74, 54S/74S, 54L/74L, 54LS/74LS, and 54H/74H series gates for selectively upgrading existing systems
2. Suppresses the effects of line ringing and significantly reduces undershoot
3. Higher thresholds (noise immunity) and better stability across operating free-air temperature range
4. Input current requirement reduced by up to 50%

Table 1. Typical Performance Characteristics by TTL Series

CIRCUIT TECHNOLOGY	MINIMIZING POWER					MINIMIZING DELAY TIME				
	FAMILY	PROP DELAY (ns)	PWR DISS (mW)	SPD/PWR PRODUCT (pJ)	MAXIMUM FLIP-FLOP FREQ (MHz)	FAMILY	PROP DELAY (ns)	PWR DISS (mW)	SPD/PWR PRODUCT (pJ)	MAXIMUM FLIP-FLOP FREQ (MHz)
Gold Doped	TTL	10	10	100	35	TTL	10	10	100	35
	L TTL	33	1	33	3	H TTL	6	22	132	50
Schottky Clamped	LS TTL	9	2	18	45	S TTL	3	19	57	125
	'ALS	4	1.2	4.8	70	'AS	1.7	8	13.6	200

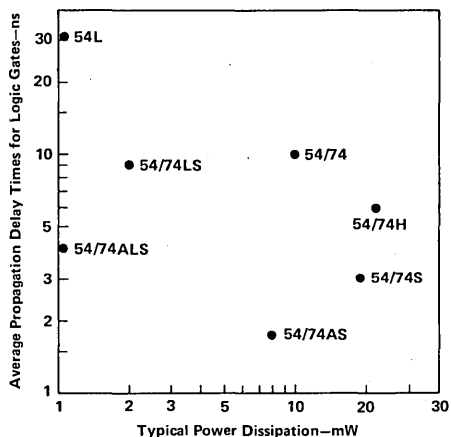


Figure 1. Speed-Power Relationships of Digital Integrated Circuits

5. Fanout is doubled
6. Terminated lines or controlled impedance circuit boards are normally not required.
7. The 'AS series offers shorter propagation delays and higher clock frequencies with relatively low power consumption.
8. The maximum flip-flop frequency has been increased to 200 MHz.

are ideal for replacement of high-speed logic families including ECL 10K series.

Compatibility With Other TTL Families

To ensure complete electrical compatibility in systems using or intending to use a mixture of existing TTL families and the new 'ALS/'AS families, specific guidelines have been implemented. These guidelines ensure the continuation of desirable characteristics and incorporate newer techniques to improve performance and/or simplify the use of TTL families. Figure 2 illustrates the comparison of essential parameters of each family and shows that complete compatibility is maintained throughout the 54/74 families.

Fanout

The compatible ratings for fanout simplify the implementation of logic and provide a freedom of choice in the use of any of the seven performance ranges to design a digital logic system. Any of the Texas Instruments TTL series gates can be used to drive any other gate without the use of an interface or level-shifting circuit. The use of totem-pole-(push-pull) type output stages provides a low output impedance and the capability for both sourcing and sinking current. The output is easily adapted for driving MOS and CMOS circuits as well as the interface circuits between the output and the devices it controls. Figure 3 illustrates fanout capability.

USING THE SCHOTTKY BARRIER DIODE

The Advanced Schottky Family has been developed from two earlier concepts: the Baker Clamp and the Schottky Barrier-Diode (SBD). The use of the Baker Clamp and SBD concepts resulted in the Schottky Clamped Transistor. The Schottky clamped transistor produced the increased switching speed associated with the S series integrated circuits. The additional advances that have led to the development of 'ALS and 'AS gates and the actual gates are discussed later.

Analysis of the Schottky Clamped Transistor

The use of the Baker Clamp, shown in Figure 4, is a method of avoiding saturation of a discrete transistor. The diode forward voltage is 0.3 V to 0.4 V as compared to 0.7 V for the base-emitter junction diode. When the transistor is turned on, base current drives the transistor toward

CONCEPTS OF DEFINING SERIES 'AS AND 'ALS

Both the 'ALS and 'AS series are electrically and pinout compatible with existing TTL series. The 'ALS series is suitable for replacing all TTL families except in the very highest frequency applications. Replacement with 'ALS will result in lower power consumption, smaller power supply current spikes, and, in some cases, better noise immunity than the other families. In those cases where a very high operating frequency is required, the 'AS series can be used. The 'AS devices require less than one-half of the supply current of the 'S series and has approximately twice the clocking frequency. The 'ALS devices are ideal for improving efficiency at the lower speeds. The 'AS devices

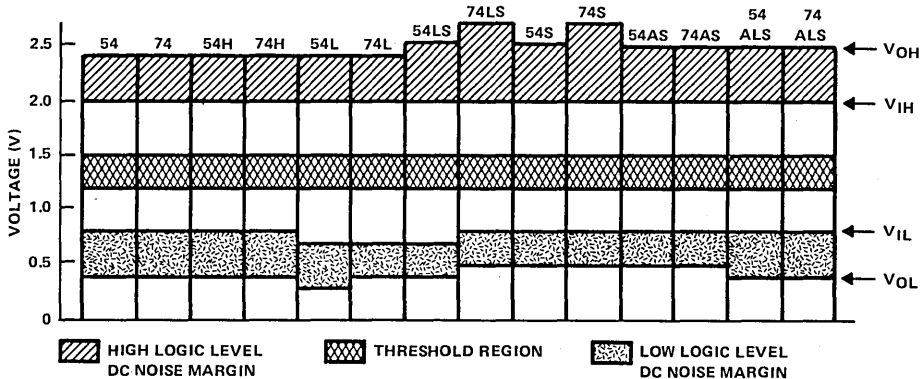


Figure 2. Series 54/74 TTL Family Compatible Levels Showing DC Noise Margins

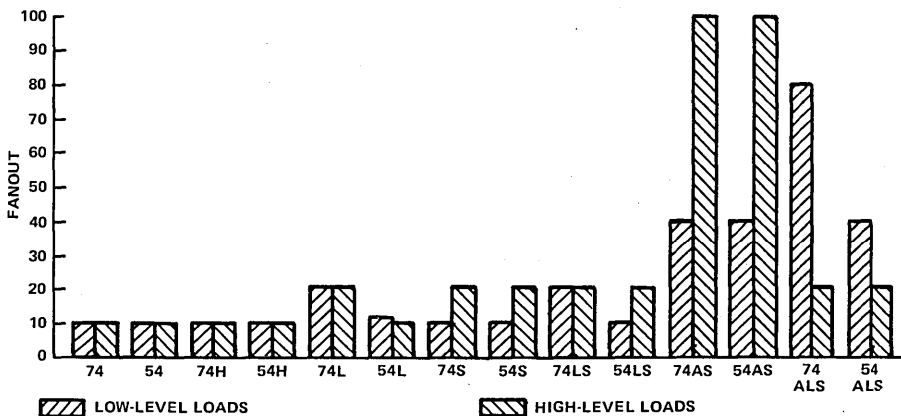


Figure 3. Fanout Capability

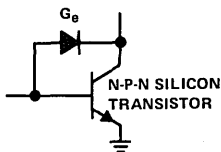
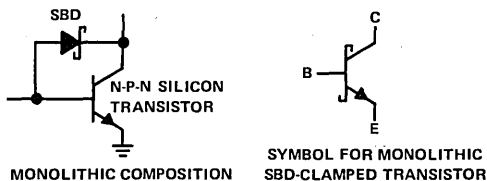


Figure 4. Baker Clamp

saturation. The collector voltage drops, the germanium diode begins to conduct forward current, and excess base drive is diverted from the base-collector junction of the transistor. This causes the transistor to be held out of deep saturation, the excess base charge to not be stored, and the turn-off time to be dramatically reduced.

A germanium diode cannot be incorporated into a monolithic silicon integrated circuit. Therefore, the germanium diode must be replaced with a silicon diode which



MONOLITHIC COMPOSITION SYMBOL FOR MONOLITHIC SBD-CLAMPED TRANSISTOR

Figure 5. The Schottky-Clamped Transistor

has a lower forward voltage drop than the base-collector junction of the transistor. A normal p-n diode will not meet this requirement. The SBD illustrated in Figure 5 can be used to meet the requirement.

The SBD illustrated in Figure 6 is a rectifying metal-semiconductor contact formed between a metal and a highly doped N semiconductor.

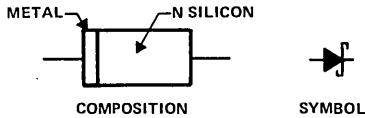


Figure 6. Schottky Barrier-Diode

The qualitative physics of an SBD is illustrated in Figure 7. The valence and conduction bands in a metal overlap make available a large number of free-energy states. The free-energy states can be filled by any electrons which are injected into the conduction band. A finite number of electrons exist in the conduction band of a semiconductor. The number of electrons depends mainly upon the thermal energy and the level of impurity atoms in the material. When a metal-semiconductor junction is formed, free electrons flow across the junction from the semiconductor, via the conduction band, and fill the free-energy states in the metal. This flow of electrons builds a depletion potential across the barrier. This depletion potential opposes the electron flow and, eventually, is sufficient to sustain a balance where there is no net electron flow across the barrier.

Under forward bias (metal positive), there are many electrons with enough thermal energy to cross the barrier potential into the metal. This forward bias is called "hot injection." Because the barrier width is decreased as forward bias V_F increases, forward current will increase rapidly with an increase in V_F .

When the SBD is reverse biased, electrons in the semiconductor require greater energy to cross the barrier. However, electrons in the metal see a barrier potential from the side essentially independent of the bias voltage and a small net reverse current will flow. Since this current flow is relatively independent of the applied reverse bias, the reverse current flow will not increase significantly until avalanche breakdown occurs.

A simple metal-n semiconductor collector contact is an ohmic contact while the SBD contact is a rectifying contact. The difference is controlled by the level of doping in the semiconductor material. As the doping is increased, the contact becomes more ohmic. Figure 8 illustrates the current-voltage characteristics according to the doping applied.

Current in the SBD is carried by majority carriers. Current in the p-n junction is carried by minority carriers. The resultant minority carrier storage causes the switching

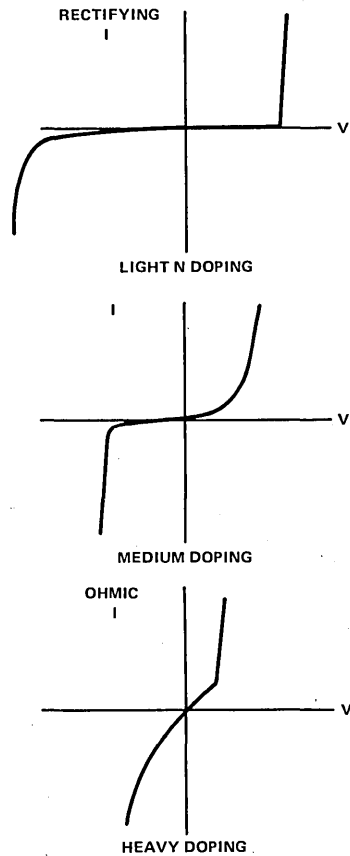


Figure 8. Metal-N Diode Current-Voltage Characteristics

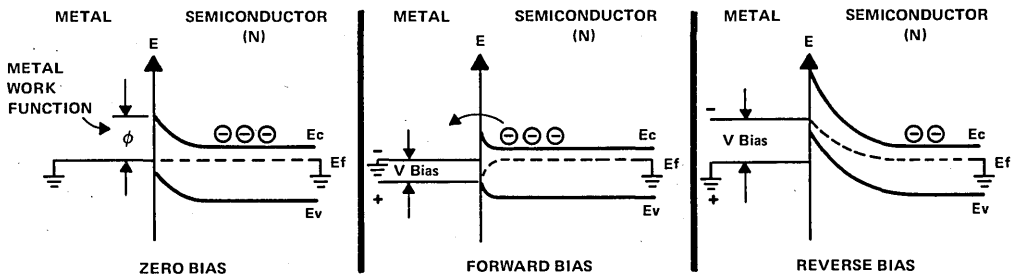


Figure 7. Schottky Barrier-Diode Energy Diagrams

time of a p-n junction to be limited when switched from forward bias to reverse bias. A p-n junction is inherently slower than an SBD even when doped with gold.

Another major difference between the SBD and p-n junction is the forward voltage drop. For diodes of the same surface area, the SBD will have a larger forward current at the same forward bias regardless of the type of metal used. The SBD forward voltage drop is lower at a given current than a p-n junction. Figure 9 illustrates the current carriers and forward current-voltage characteristics differences between the SBD and p-n junction. The SBD meets the requirements of a silicon diode which will clamp a silicon n-p-n transistor out of saturation.

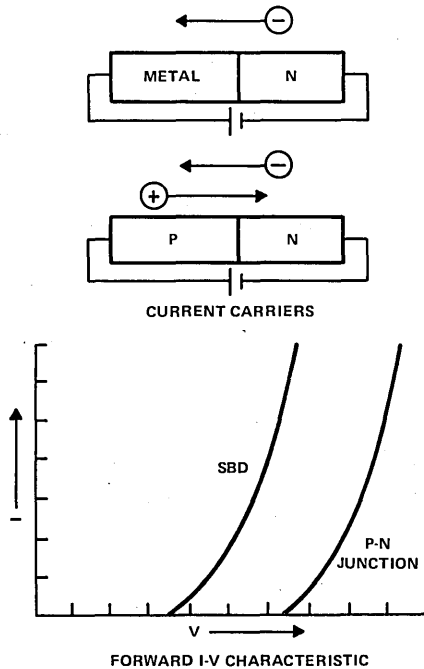


Figure 9. Differences Between P-N and Schottky Barrier-Diodes

The Advanced Schottky process differs from the Schottky process in that it uses ion implantation of impurities instead of diffusion. Ion implantation gives greater control on the depth of doping and resolution. Because of a thinner epitaxial layer and smaller all around geometries, smaller parasitic capacitances are encountered. The performance of the SBD is also enhanced by the use of oxide isolation of the transistors. This reduces the collector-substrate capacitance. Figure 10 illustrates the 'LS/S' process which consists of conventional masks, junction isolation, and a

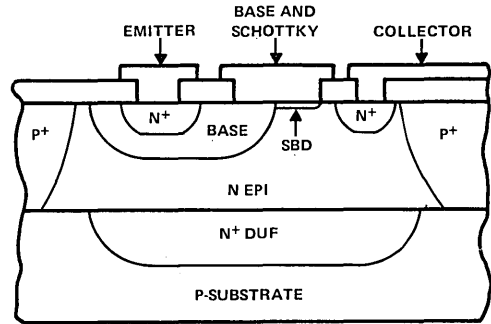


Figure 10. Standard Process ('LS/S')

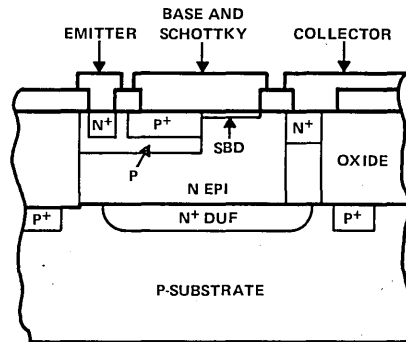


Figure 11. Advanced Process ('ALS/AS')

standard metal system and Figure 11 illustrates the 'ALS/AS' process which consists of composed masks, ion implantation, oxide isolation, and a standard metal system.

Analysis of 'ALS and 'AS NAND Gates

The 'ALS and 'AS NAND gates in Figures 12 and 13 combine the desirable features of improved TTL circuits with the technological advantages of full Schottky clamping, ion implantation, and oxide isolation to achieve very fast switching times at a reduced speed-power product. The improvements and advantages are as follows:

1. Full Schottky clamping of all saturating transistors virtually eliminates storing excessive base charge and significantly enhances turn-off time of the transistors.
2. Elimination of transistor storage time provides stable switching times across the temperature range.
3. An active turn-off is added to square up the transfer characteristic and provide an improved high-level noise immunity.

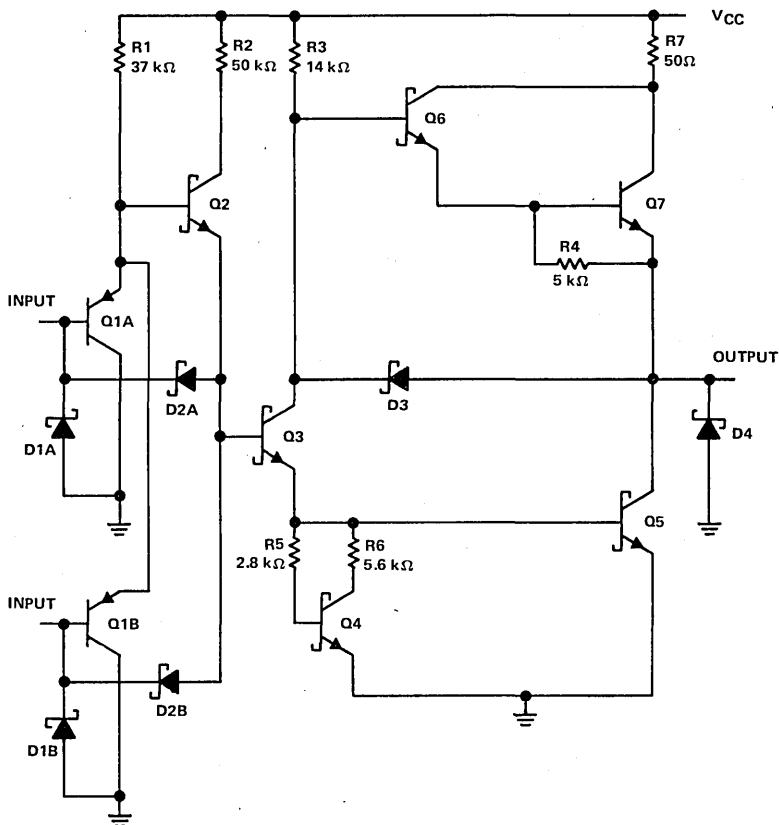


Figure 12. 'ALS00A NAND Gate Schematic

4. Input and output clamping is implemented with Schottky diodes to reduce negative-going excursions on the inputs and outputs. Because of its lower forward voltage drop and fast recovery time, the Schottky input diode provides improved clamping action over a conventional p-n junction diode.
5. The ion implantation process allows small geometries giving less parasitic capacitances so that switching times are decreased.
6. The reduction of the epi-substrate capacitance using oxide isolation also decreases switching times.

A key feature of the 'ALS and 'AS families is the improvement in typical input-threshold voltage. Figure 12 is a schematic diagram of the 'ALS00A NAND gate. Figure 13 is a schematic diagram of the 'AS00 NAND gate. The input threshold voltage of the devices is determined by the equation:

$$V_T = V_{BE} \text{ of } Q2 + V_{BE} \text{ of } Q3 + V_{BE} \text{ of } Q5 - V_{BE} \text{ of } Q1A \text{ (or } V_{BE} \text{ of } Q1B) \quad (1)$$

From Eq. (1) it can be determined that the input threshold voltage is two times V_{BE} or approximately 1.4 V. Low-level input current I_{IL} is reduced in the 'ALS00A/'AS00 gates because of the improved input circuits. Buffering by transistors Q1A (or Q1B) and Q2 causes a significant reduction in low-level input current. Low-level input current is determined by the equation:

$$I_{IL} = \frac{V_{CC} - V_{BE} \text{ of } Q1A}{-V_I/[R(h_{FE} \text{ of } Q1A + 1)]} \quad (2)$$

By using Eq. (2) low-level input current is reduced by at least the factor of h_{FE} of Q1A + 1 and is typically $-10 \mu A$ for the 'ALS00A and $-50 \mu A$ for the 'AS00. High-level output voltage V_{OH} is determined primarily by V_{CC} ,

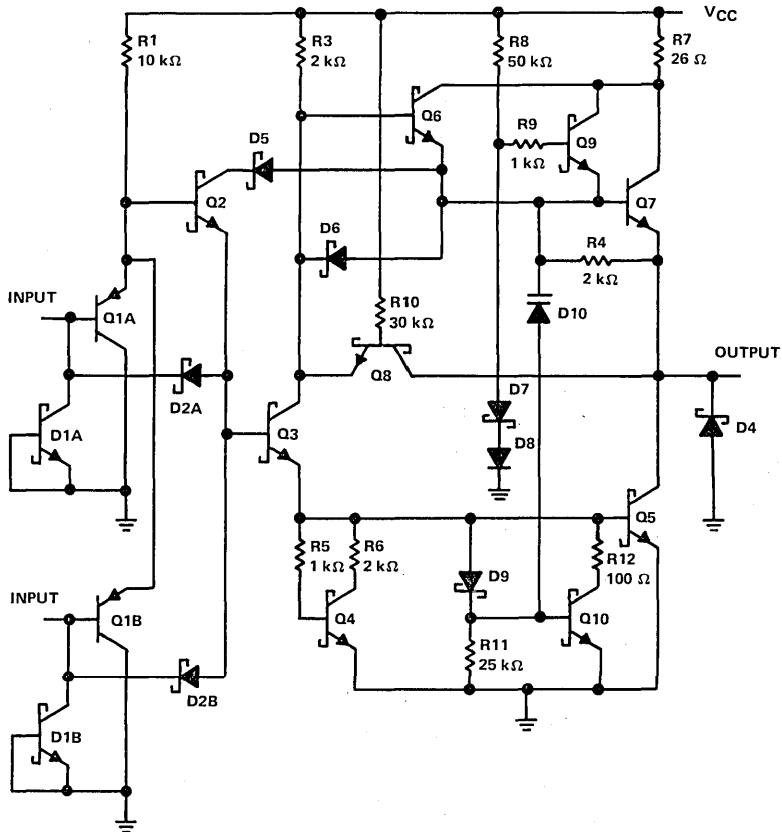


Figure 13. 'AS00 NAND Gate Schematic

resistors R4 and R7, and transistors Q6 and Q7. With no load, the high-level output voltage is approximately equal to $V_{CC} - V_{BE}$ of Q6 because the voltage across resistor R4 is 0 V. For medium-level currents, the high-level output voltage is equal to $V_{CC} - V_{BE}$ of Q7 because of the Darlington gain of transistors Q6 and Q7. The current through resistor R3 is typically less than $1 \mu\text{A}$ and, therefore, the voltage drop is negligible. As conduction through transistors Q6 and Q7 is increased, the voltage drop across limiting resistor R7 will increase until the Schottky clamping diode of transistor Q6 starts to become forward biased. At this point, the current through resistor R3 (and the voltage drop) is no longer negligible and the high-level output voltage is determined by:

$$V_{OH} = V_{CC} - I_{OH \text{ through } R7} \times R7 - V_{CE} \text{ of } Q6 - V_{BE} \text{ of } Q7 \quad (3)$$

Low-level output voltage V_{OL} is determined by the turning on of transistor Q5. When the input is high and transistor

Q2 is turned on, high-current transistor Q5 is turned on by a current path through transistor Q3 and resistor R3. Sufficient base drive is supplied to keep transistor Q5 fully turned on at an apparent output resistance of 14Ω for 'ALS and 6Ω for 'AS.

The fanout is up to 40 for a '54ALS device that is driving a '54ALS device and up to 80 for a '74ALS device, that is driving a '74ALS device and provides a guaranteed low-level output current of 4 mA and 8 mA, respectively.

The increase in speed-power product of '54ALS/'74ALS devices, a factor four times better than '54LS/'74LS devices, is due to the design consideration of the quiescent and switching operations of the circuit. In the quiescent state, transistor Q2 allows the use of a reduced low-level input current. This reduces the fanout and reduces the overall quiescent current requirements.

The design of diodes D2 and D3 (or transistor Q8) and transistor Q4 enhances the speed-power product of the device. Transistor Q4 reduces the turn-off time and consequently the current transients caused by conduction



overlap of transistor Q5. The same principle is used by diodes D2 and D3 and transistor Q3 in turning off transistor Q7. In addition, the active turn-off design produces a square transfer characteristic.

The 'AS00 gate has additional circuits not on the 'ALS00A gate. The circuits are added to enhance the throughput of the 'AS Family.

Transistor Q10 has been added as a discharge path for the base-collector capacitance of transistor Q5. Without transistor Q10, rising voltages at the collector of transistor Q5 would force current, via the base-collector capacitance, into the base of transistor Q5 causing it to turn on. However, diode D10 causes transistor Q10 to turn on (during rising voltage) and keeps transistor Q5 turned off. Diodes D6 and D9 serve as a discharge path for capacitor-diode D10.

CIRCUIT PARAMETERS

Worst-case testing of 'ALS/'AS devices provides a margin of safety. [All dc limits shown on the data sheet are guaranteed over the entire temperature range (-55°C to 125°C) for series 54ALS/54AS and 0°C to 70°C for series 74ALS/74AS]. In addition, the dc limits are guaranteed over the entire supply voltage range (4.5 V to 5.5 V).

Transfer Characteristics

Since the most common application for a logic gate is to drive a similar logic gate, the input and output logic levels

must be compatible. The input and output logic levels for 'ALS/'AS devices are as follows:

- V_{IL} — The voltage value required for a low-level input voltage that guarantees operation
- V_{IH} — The voltage value required for a high-level input voltage that guarantees operation
- V_{OL} — The guaranteed maximum low-level output voltage of a gate
- V_{OH} — The guaranteed minimum high-level output voltage of a gate.

With the exception of high-level output voltage (which is a direct function of supply voltage), these values remain virtually unchanged over the temperature range and under normal operating conditions of the device.

Analysis of the input and output response characteristics of 'ALS/'AS TTL gates is necessary to understand the operation of these devices in most system applications. The dc response characteristics can best be depicted by an input voltage V_I versus output voltage V_O transfer plot.

Figure 14 plots the 'ALS/'AS characteristics as compared with members of other TTL logic families.

As shown in Figure 14, the 'ALS and 'AS devices exhibit a much better output savings when compared with standard TTL devices. The better high-level output voltage is primarily because of the active turn off of the low-level output transistor. The diode voltage drop in the normal output is replaced by a low-current V_{BE} voltage drop. This provides

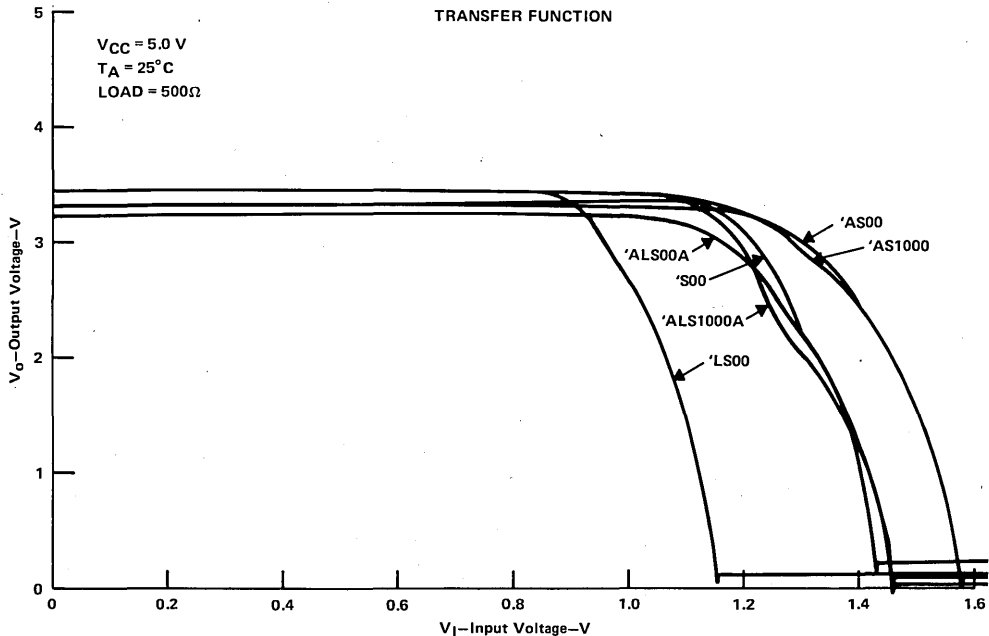


Figure 14. Input Voltage vs Output Voltage of 'ALS/'AS

a better high-level noise immunity in 'ALS and 'AS over standard TTL devices.

Input Characteristics

To use 'ALS/'AS devices fully, a knowledge of the input and output characteristics is required. This is particularly true when a device interfaces with a device not in the same TTL series. In addition, knowledge of voltage and current relationships for all elements is important for proper design.

Figure 15 illustrates a typical plot for input current I_I versus input voltage, V_I , characteristics for 'ALS/'AS gate inputs during normal operation. A typical series 54/74 characteristic plot is also shown for reference. Any device used to drive a TTL gate must source and sink current. Conventionally, current flowing toward a device input terminal is designated as positive and current flowing out

of a device input terminal is designated as negative. Low-level input current is negative current because it flows out of the input terminal. High-level input current is a positive current because it flows into the input terminal.

For transmission line conditions, a more accurate plot of the reverse bias section of these curves is required. These curves, Figure 16, are characteristic of the input clamping diode.

Low-Level Input Current

Figure 17 illustrates the dc equivalent of a standard 'ALS/'AS input circuit and shows the input current paths during a low-level input state. The low-level input current is primarily determined by resistor R1. However, low-level input current is also a function of the supply voltage, the ambient temperature, and the low-level input voltage. To

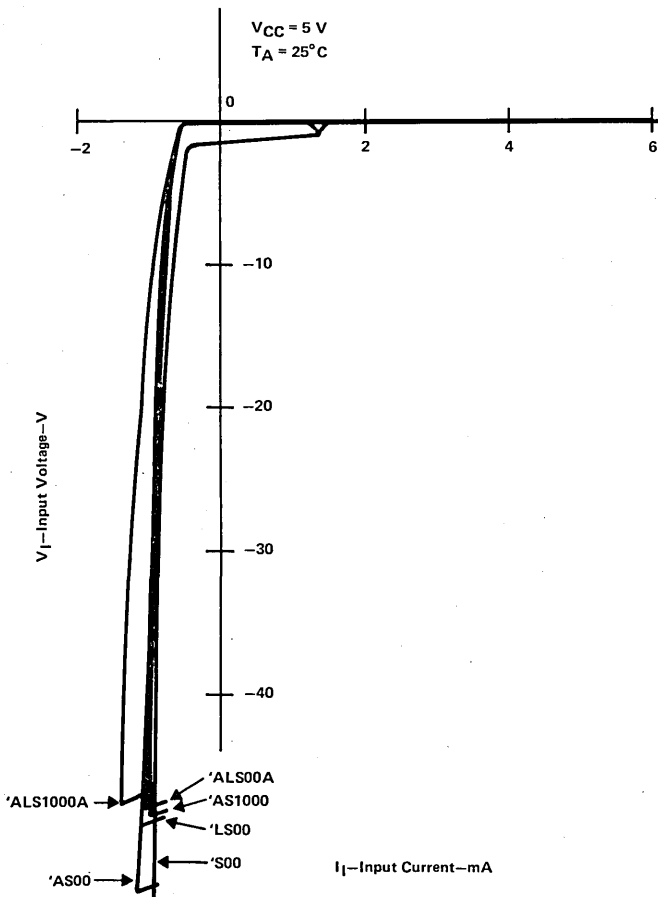


Figure 15. Input Current vs Input Voltage for TTL Families

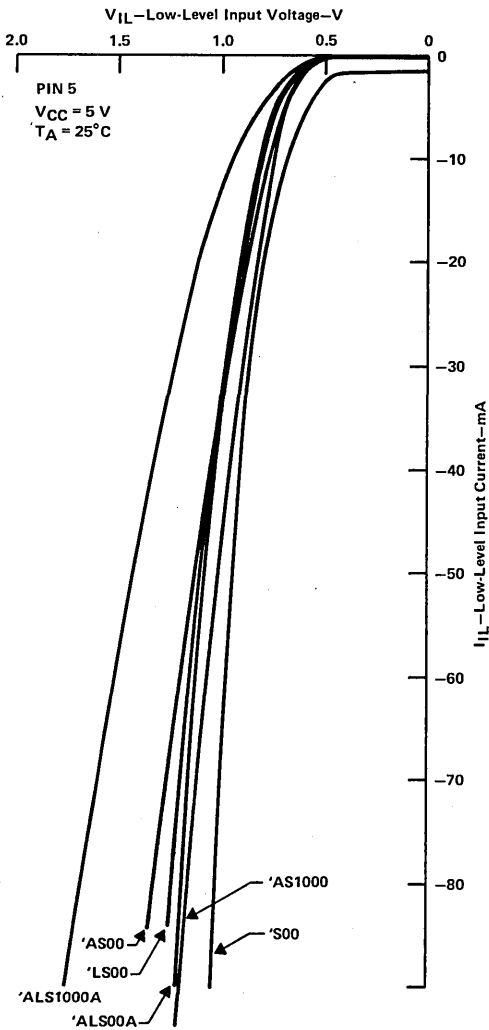


Figure 16. Low-Level Input Current vs High-Level Input Voltage for TTL Families

assure desired device operation under all possible conditions, the worst-case test is performed on all devices. Supply voltage is taken to the highest allowable value to cause the low-level input current to be at a maximum. With the exception of the input under test, all unused inputs are taken to a high level. This enhances any contribution of these inputs to the low-level input current of the emitter under test.

Input Clamping Diode Test

The quality of the input clamping SBD (D2 in Figure 17) is tested by ensuring that the forward voltage drop is not

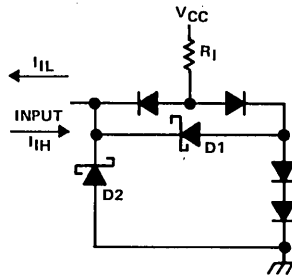


Figure 17. DC Equivalent Input Circuit for Series 'ALS Gate

greater than -1.2 V for 'AS and -1.5 V for 'ALS with a forward current of 18 mA. These values are guaranteed at minimum supply voltage and are valid across the operating temperature range. The characteristic of the input diode is illustrated in Figure 16.

High-Level Input Current

Another input parameter that must be measured and controlled is high-level input current. To ensure desired device operation under all possible conditions, the worst-case test is performed with all unused inputs grounded and supply voltage at its maximum value. This provides the highest value of low-level input current. Those devices with a high-level input current of sufficient magnitude to cause a degradation of high-level output voltage at an output must be screened out.

Input Breakdown Test

An additional high-level input current test is performed to check for base-emitter breakdown under the application of the full range of input voltages. This test is performed under the worst-case supply voltage conditions and is important because the base-emitter junction is small and can easily be overdispipated during the breakdown conditions.

Output Characteristics

The most versatile TTL output configuration is the push-pull (totem-pole) type. The totem-pole output has a low output impedance drive capability at both high and low logic levels. Both 'ALS and 'AS families use this configuration and have fanouts of 40 in both the high- and low-level states.

High-Level Output Characteristics

The ability of the totem-pole output to supply high-level output current is parametrically tested by applying a high-level input current value during measurement of high-level output voltage. However, the quality of the output stage is best indicated by parametrically measuring its current sourcing I_{O5} capability when connected to ground. Figure 18 shows the equivalent output circuit under high-level output conditions.

Figure 19 illustrates typical high-level characteristics. When measuring worst-case high-level output voltage, minimum supply voltage is used. A worst-case low-level

input voltage is applied to an input and all unused inputs are tied to supply voltage.

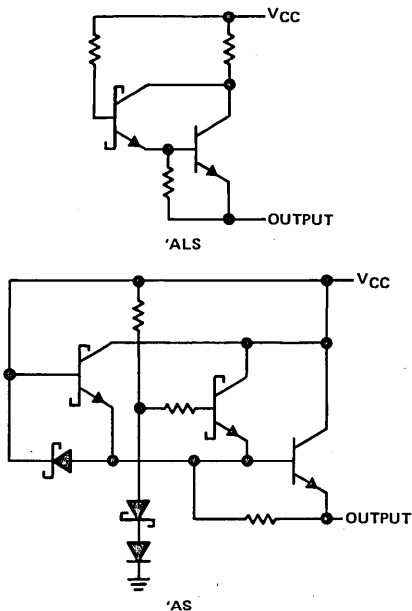


Figure 18. Equivalent Output Circuit for 'ALS/'AS Gates

Low-Level Output Characteristics

Figure 20 shows that section of the output drive circuit which produces a low-level output voltage V_{OL} . This characteristic is also tested at minimum supply voltage. Figure 21 illustrates the typical curve.

Switching Speed

Two switching-speed parameters are guaranteed on Series 'ALS and 'AS gates: propagation delay time for a high-level to a low-level at the output t_{PHL} , and a low-level to high-level transition time t_{PLH} . Both parameters are specified with respect to the input pulse using standard test conditions as follows:

- $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$
- $C_L = 50 \text{ pF}$
- $R_L = 500$
- $T_A = \text{MIN to MAX}$

Under these conditions, times in the order of 4 ns for 'ALS and 1.7 ns for 'AS are typical. Figures 22 and 23 illustrate how the propagation delay time for 'ALS and 'AS devices vary with load capacitance.

Most current in the output stage is drawn when both output transistors are on (i.e., during output transitions, the average power dissipation of a gate with a totem-pole output increases with operating frequency). This is caused by more high-current transitions per second at the output as the frequency increases. Figure 24 illustrates the effect for both 'ALS and 'AS devices.

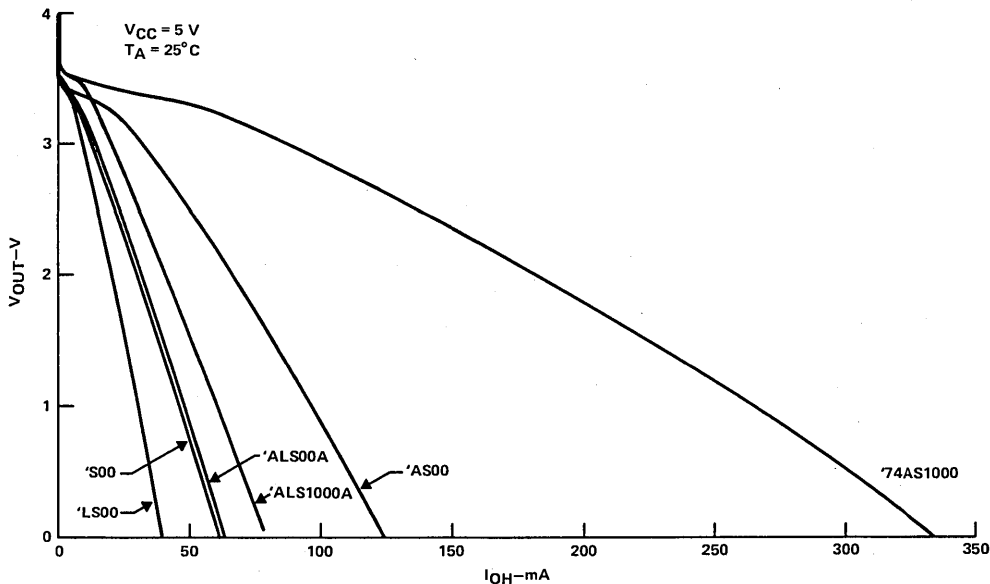


Figure 19. High-Level Output Voltage vs High-Level Output Current

DC Noise Margins

Noise margin is a voltage specification which guarantees the static dc immunity of a circuit to adverse operating conditions. Noise margin is defined as the difference between the worst-case input logic level (V_{IH} minimum or V_{IL}

maximum) and the guaranteed worst-case output (V_{OH} minimum or V_{OL} maximum) specified to drive the inputs. Table 2 lists the worst-case output limits for the 'AS and 'ALS families.

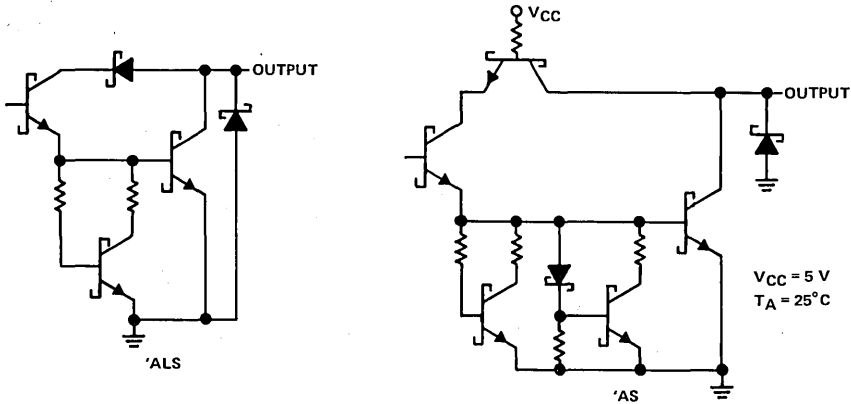


Figure 20. Low-Level Output Circuit for 'ALS/'AS Gates

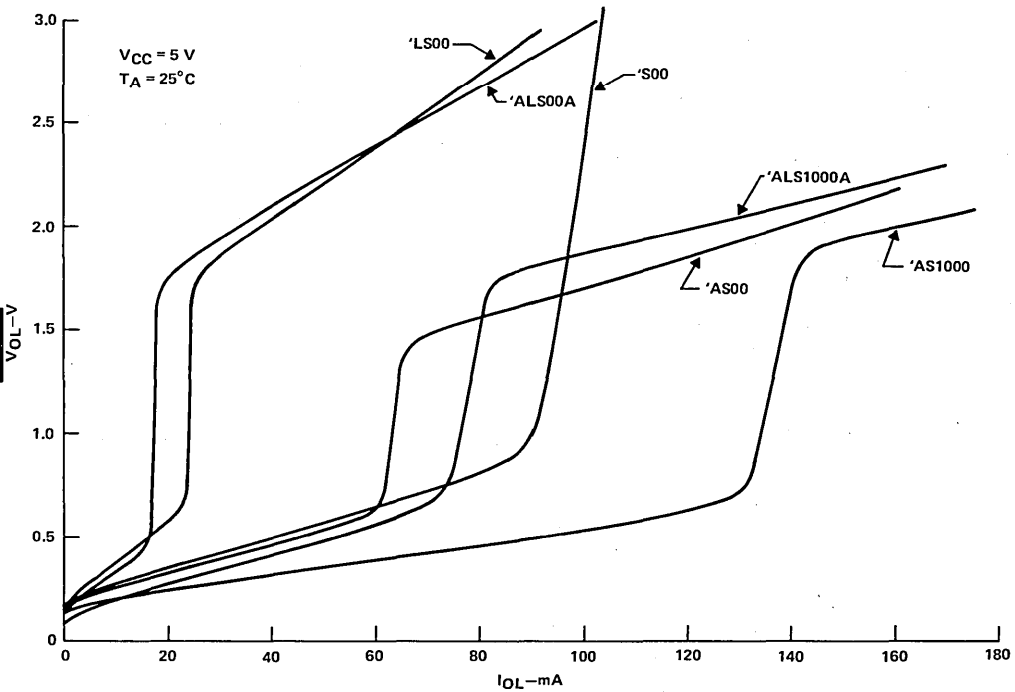


Figure 21. Low-Level Output Voltage vs Low-Level Output Current

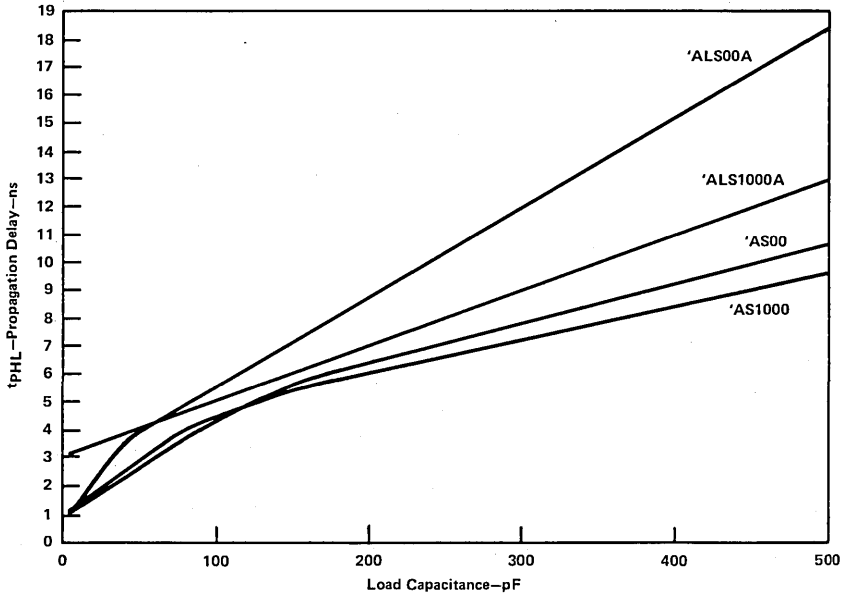


Figure 22. High- to Low-Level Propagation Delay vs Load Capacitance

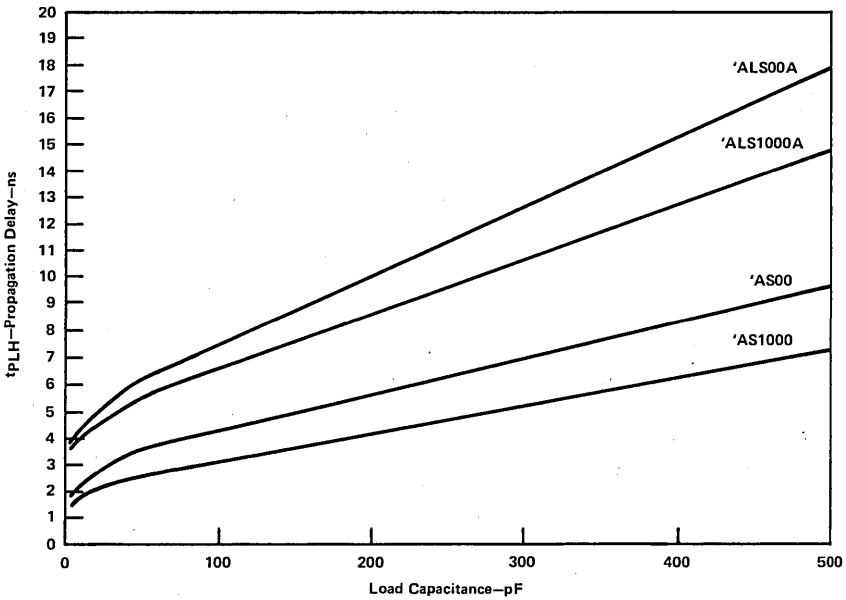


Figure 23. Low- to High-Level Propagation Delay vs Load Capacitance

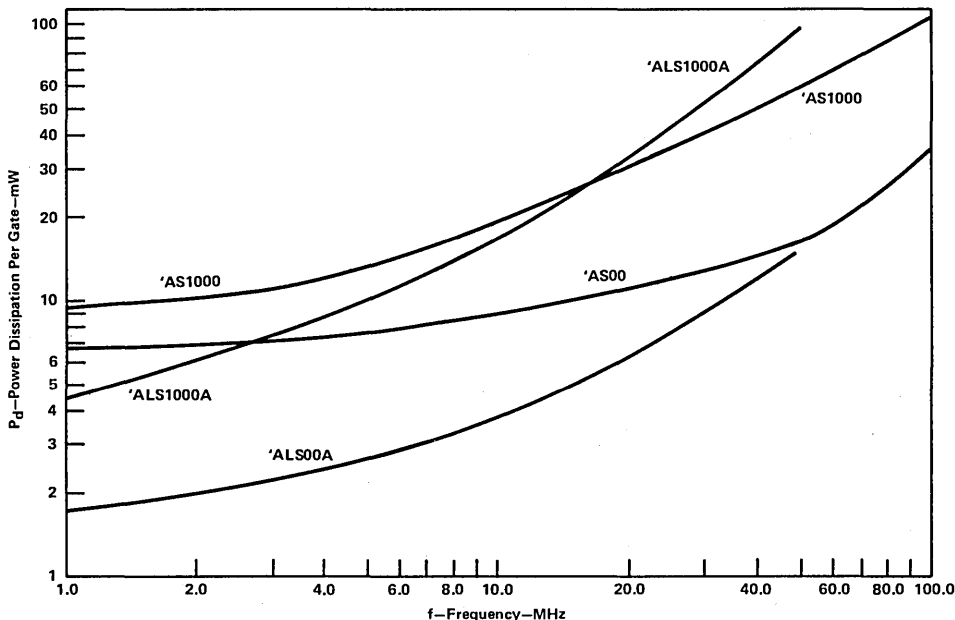


Figure 24. Power Dissipation per Gate vs Frequency

Specified Logic Levels and Thresholds

The high-level noise margin is obtained by subtracting V_{OH} minimum from V_{IH} minimum. The low-level noise margin is obtained by subtracting V_{IL} maximum from V_{OL} maximum. The worst-case high-level noise margin is guaranteed to be at least 500 mV for both 'AS and 'ALS devices and at least 300 mV for low-level noise immunity across the operating free-air temperature ranges.

The usefulness of noise margins at the system design level is the ability of a device to be impervious to noise spikes at the input. The input voltage falls into one of three categories: low-logic state (between ground and 0.8 V), threshold region (between 0.8 V and 2 V), or high-logic state (between 2 V and V_{CC}). If an input voltage remains exclusively in the low-logic or high-logic state, it can undergo

any excursions within that state. A level change from 5.5 V to 2 V or from ground to 0.8 V should not affect the output state of the device. To guarantee an expected output level change, the appropriate input has to undergo a change from one input state to the other input state (i.e., a transition through the threshold region). If a device will not remain in the correct state when voltage excursions on the input are occurring, it is violating its truth table.

Noise Rejection

The ability of a logic element to operate in a noise environment involves more than the dc or ac noise margins previously discussed. To present a problem, an externally generated noise pulse must be received into the system and cause a malfunction. Stable logic systems with no storage

Table 2. Worst Case Output Parameters

PARAMETER (V)	'AS (0°C to 70°C)	'ALS (0°C to 70°C)	'AS (-55°C to 125°C)	'ALS (-55°C to 125°C)
$V_{IH}(MIN)$	2	2	2	2
$V_{IL}(MAX)$	0.8	0.8	0.8	0.8
$V_{OH}(MIN)$ @ $C_C = 4.5 V^*$	2.5	2.5	2.5	2.5
$V_{OL}(MAX)$	0.5	0.5	0.5	0.4
High Level Noise Margin ($V_{OH} - V_{IH}$)	0.5	0.5	0.5	0.5
Low Level Noise Margin ($V_{IL} - V_{OL}$)	0.3	0.3	0.3	0.4

*Actual specification for $V_{OH}(min)$ is $V_{CC} - 2 V$.

elements are practically impervious to ac noise. However, large dc voltages could cause noise problems. Systems with triggerable storage elements or those operating fast enough for the noise to appear as a signal are much more susceptible to noise.

The noise voltage must be radiated or coupled into the circuit. The amount of noise required to develop a given voltage is a function of the circuit impedance. Because of the low output impedance of TTL circuits, noise immunity is improved. Noise is transferred from the source (with some arbitrary impedance) through a coupling impedance to the impedance of the circuit under consideration.

Figure 25 shows a circuit where the coupling impedance is stray capacitance and the load impedance is provided by the gates. The relatively tight coupling of this circuit and the loading effect on the driving source is significant enough

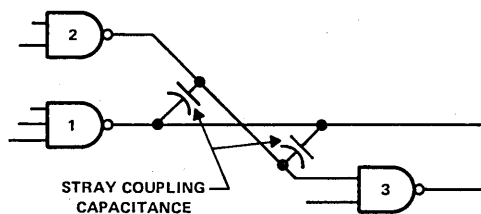


Figure 25. Stray Coupling Capacitance

to be considered. However, since the source effect is difficult to assess and is in a direction to improve rather than degrade the noise rejection, its effects are ignored. This results in a worst-case type of response indication. In the case of radiated noise, the source resistance is a definite factor in noise coupling and essentially replaces the reactive coupling impedance.

By ignoring the driving source impedance to make conditions more nearly standard, it is possible to determine a set of curves relating the developed noise pulse to the noise source amplitude, the noise rise or fall time, the coupling impedance, and the load impedance. Curves have been developed¹ for several different input waveforms. Since the 'ALS waveform is essentially a ramp with a dv/vt of 1 V/ns (approximately 2.5 V/ns for 'AS), the most applicable curve is that for a ramp input.

Figure 26(a) shows the equivalent circuit from which the ramp response plot in Figure 26(b) was developed. The input pulse shown in Figure 26(c) is a ramp input.

$$e_i(t) = \frac{E_i}{T} t$$

where

E_i = Maximum input voltage and
 T = Total rise time of input voltage

The output pulse is represented analytically by

$$e_0(t) = \frac{E_i}{T} RC \left(1 - e^{-\frac{t/T}{RC/T}} \right)$$

$$e_0(i) = E_i \tau \left(1 - e^{-i/\tau} \right)$$

where

$$\tau = \frac{RC}{T}$$

$$\theta(i) = \tau \left(1 - e^{-i/\tau} \right)$$

$$\theta(i) = \frac{e_0(i)}{E_i}$$

with holding for unit time. This is followed by an exponentially decaying voltage with a time constant τ . Values of τ and i on the figure are normalized by the value of the total rise time of the stimulated noise pulse e_i . Using Figure 26(b), the pulse width and amplitude of the coupled noise pulse can be estimated.

As an example, using the circuit shown in Figure 25, apply a noise pulse of 3 V in amplitude and rising at 1 V/ns

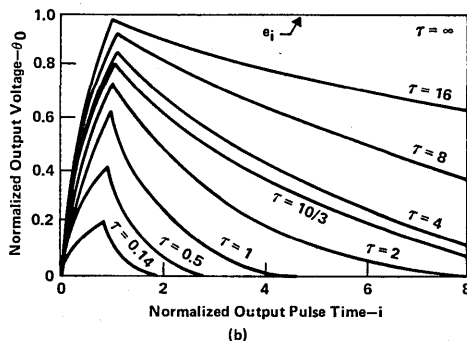
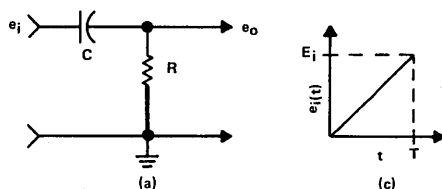


Figure 26. Evaluations of Gate Response to Fast Input Pulses

with gate 2 at a high-logic state. Assume a nominal output impedance of 58Ω (30Ω for 'AS) and coupling capacitance of 10 pF . Use the following formula:

$$\text{Total rise time } T = \frac{3 \text{ V}}{1 \text{ V/ns}^{**}} = 3 \text{ ns}^\dagger$$

$$\begin{aligned} \tau &= \frac{RC}{T} = \frac{(10 \times 10^{-12})(58)}{3} \\ &= \frac{0.58 \times 10^{-9}}{3} = 0.19 \text{ ns} \end{aligned}$$

**2.5 V/ns for 'AS

†1.2 ns for 'AS

To convert the normalized values of τ and i in Figure 26(b) to actual values, multiply by 3 ns . The output voltage scale will be multiplied by 3 V . Using the $\tau = 0.19$ curve gives a peak e_o of 0.57 V (0.19×3) and a pulse width of 3 ns at the 50% points. To determine whether this pulse will cause interference, enter these values (0.57 V and 3 ns) on the graph shown in Figure 27. Since the gates have approximately 1.8 V of noise immunity at this point, they should not be affected.

If an open-collector gate is used with a passive $1 \text{ k}\Omega$ pull-up resistor, the situation would change. Use the following formula:

$$\text{Total rise time} = \frac{3 \text{ V}}{1 \text{ V/ns}^{**}} = 3 \text{ ns}^\dagger$$

$$\begin{aligned} \tau &= \frac{(10 \times 10^{-12})(1 \times 10^3)}{3} \\ &= \frac{10 \times 10^{-9}}{3} = \frac{10}{3} \text{ ns} \end{aligned}$$

**2.5 V/ns for 'AS

†1.2 ns for 'AS

Now the amplitude (from the curves) approaches 2.58 V (0.86×3) and the pulse width at the 50% points is approximately 8.52 ns (2.84×3). The next gate will propagate this pulse.

This example is an oversimplification. The coupling impedances are complex (but resolvable into RLC series coupling elements) and the gate output impedance changes with load. Our purpose is to show why and how the low impedance of the active TTL output rejects noise and to make a comparison with a passive pull-up.

The ability to operate in a noisy environment is an interaction of the built-in operating margins, the time required for the device to react, and the ease with which a noise voltage is developed. In all cases, except the ability to react to short noise pulses, the TTL design has emphasized noise rejection.

Nothing has been discussed concerning noise in devices other than gate circuits. Many MSI devices are complex gate

networks and, because of their small size, are more superior in a noisy environment operation than their discrete gate equivalents. Noise tolerance of latching devices is implied in the setup times, hold times, clock pulse width, data pulse widths, and similar parameters. Output impedances and input noise margins are quite similar to those of the gates and may be treated in a similar manner. If a latching device does become noise triggered, the effective error is stored and does not disappear with the noise.

Parameter measurement information is shown in Figure 28.

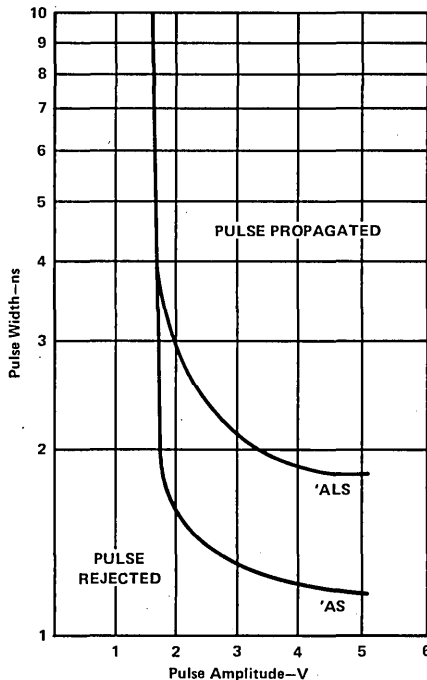
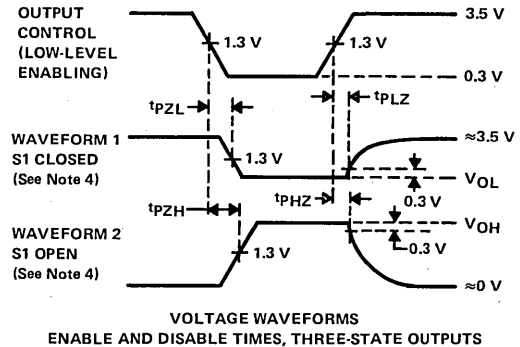
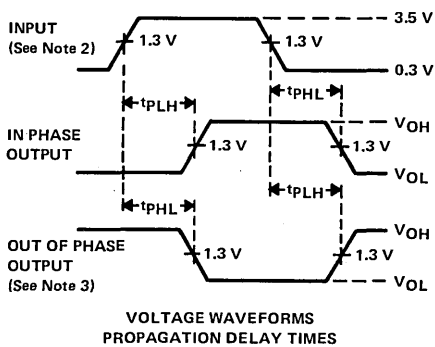
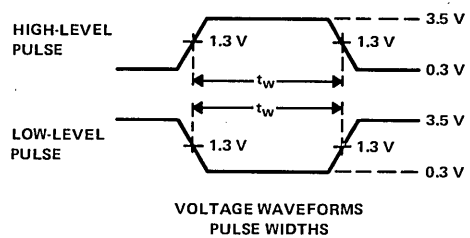
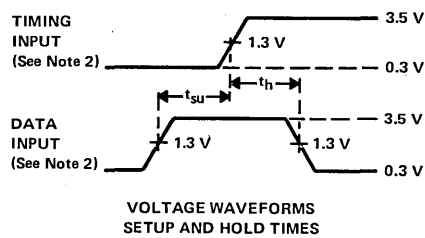
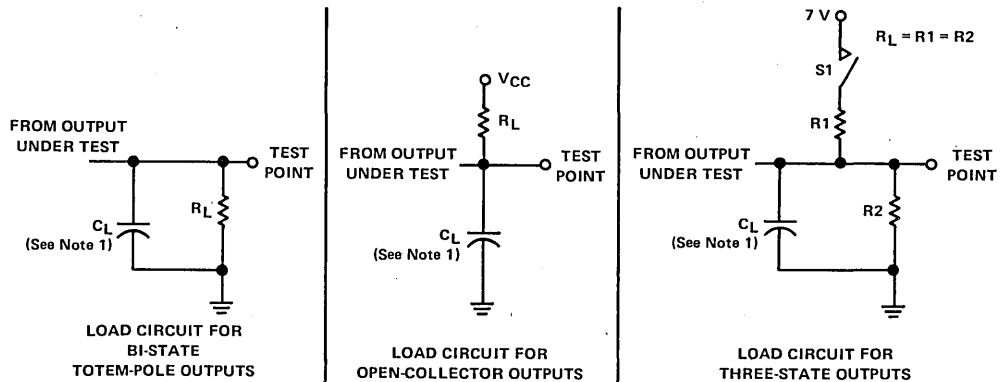


Figure 27. Theoretical Required Pulse Width vs Pulse Amplitude for 'AS and 'ALS Inputs

GUIDELINES FOR SERIES 'ALS/'ALS TTL SYSTEM DESIGN

System layout and design requirements for Advanced Schottky TTL circuits are essentially the same as those guidelines which have previously been established and are applicable for all high-performance digital systems. Tables 3 through 6 provide a brief summary of the solutions to most design decisions needed to implement systems using Advanced Schottky TTL. Supplementary data which may be useful for developing specific answers to unique problems is provided later.



NOTES: 1. C_L includes probe and jig capacitance.

2. All input pulses have the following characteristics $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.

3. When measuring propagation delay times of 3-state outputs, switch S1 is open.

4. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 28. Parameter Measurement Information

POWER SUPPLY REGULATION

Power supply regulation cannot be treated as if it is an independent characteristic of the device involved. Power supply regulation, along with temperature range, affects noise margins, fanout, switching-speed, and several other parameters. The characteristics most affected are noise

margin and fanout. When these two parameters are within the specified limits, the power-supply regulation will normally be within specified limits. However, on a device where auxiliary parameters are more critically specified, a more restrictive power-supply regulation is normally required. When power-supply regulation is slightly outside the specified limits for TTL devices, the device may still

operate satisfactorily. However, if high ambient-noise levels and extreme temperatures are encountered, failures may occur.

Application of a supply voltage above 7 V (absolute maximum rating) will result in damage to the circuit.

Since power dissipation in the package is directly related to supply voltage, the maximum recommended supply voltage for TTL devices is specified at 5.5 V. This provides an adequate margin to ensure that functional capability and long-term reliability are not jeopardized.

High-level output voltage is almost directly proportional to supply voltage (i.e., a drop in supply voltage causes a drop in high-level output voltage and an increase in supply voltage

results in an increase in high-level output voltage). Because of this relationship, high-level output voltage for 'ALS' AS devices is specified as supply voltage -2 V ($V_{CC} - 2\text{ V}$).

Since high-level output voltage is directly related to supply voltage, the output current of the device is also directly related. The output current value is established by choosing output conditions to produce a current that is approximately one-half of the true short-circuit current.

It is advantageous to regulate or clamp the maximum supply voltage at 5.5 V including noise ripple and spikes. When this conditions exists, unused AND and NAND gates can be connected directly to the supply voltage.

Table 3. Guidelines for Systems Design for Advanced Schottky TTL

ITEM	GUIDELINE
Single wire connections	Wire lengths up to approximately 12 inches may be used. A form of ground plane is desirable. Use point-to-point routing rather than parallel. If the wire is longer than 12 inches, use either a dense ground plane with the wire routed as close to it as possible, or use a twisted-pair cable.
Coaxial and twisted-pair cables	Design around approximately 80 Ω to 100 Ω of characteristic impedance. Cross talk increases at higher impedances. Use a coaxial cable of 93 Ω impedance (e.g., Microdot 293–3913). For twisted-pair cable, use number 26 or number 28 wire with the insulation twisted at the rate of 30 turns per foot.
Transmission-line-ground	Ensure that transmission-line ground returns are carried through at both transmitting and receiving ends. V_{CC} decoupling ground, device ground, and transmission-line ground should have a common tie point.
Cross talk	Use point-to-point back-panel wiring to minimize noise pickup between lines. Avoid long unshielded parallel runs. However, if they must be used, they should carry signals that propagate in the same direction.
Reflections	Reflections occur when data interconnects become long enough that 2-line propagation delays are pulse transition times. For series TTL, reflections are normally of no importance for lines shorter than 12 inches.
Resistive pull-up	If fanout of driving output permits, use approximately 300 Ω of resistive pull-up at the receiving end of long cables. This provides added noise margin and more rapid rise times.

Table 4. Guidelines for Printed Circuit Board Layout for Advanced Schottky TTL

ITEM	GUIDELINE
Signal connections	Whenever possible, distribute loads along direct connections. Signal leads should be kept as short as possible. However, lead lengths of up to 15 inches will perform satisfactorily. This is especially for large boards that use a ground plane, ground, and/or V_{CC} plane. In addition, it will perform satisfactorily for small boards using ground mesh or grid. In high-frequency applications, avoid radial fanouts and stubs. If they must be used to drive some loads, reduce lead length proportionally and avoid sharp bends. Normal on-board fanouts and interconnections do not require terminations. Response of lines driving large numbers or highly capacitive loads can be improved with terminations of 300 Ω to V_{CC} and 600 Ω to ground in parallel with the last load if fanout of the driving output permits.
Conductor widths	Signal-line widths down to 0.015 inch are adequate for most signal leads.
Signal-line spacing	Signal-lead spacing on any layer down to 0.015 inch can be used especially if care is taken to avoid adjacent use of maximum length and minimum spacing. Increase spacing wherever layout permits. Pay particular attention to clock and/or other sensitive signals.
Insulator material	Thickness of insulation material used for a multilayer board is not critical. If ground and V_{CC} planes or meshes are used, their capacitive proximity can be used to reduce the number of decoupling capacitors needed and this also supplements the supply bypass capacitor.

Table 5. Guidelines for General Usage of Advanced Schottky TTL

ITEM	GUIDELINE
Power supply	For RF bypass supply primary, maintain ripple and regulation at less than or equal to 10%.
V _{CC} decoupling	Decouple every 2 to 5 packages with RF capacitors of 0.01 to 0.1 μF. Capacitors should be located as near as possible to the decoupled devices. Decouple line driving or receiving devices separately with 0.1 μF capacitors between V _{CC} and the ground pins.
On-board grounding	A ground plane is essential when the PCB is relatively large (over 12 inches). Smaller boards will work with ground and/or V _{CC} mesh or grid.
System grounding	Try to simulate bus bars with a width to thickness ratio greater than or equal to 4. This can be accomplished by multiple parallel wires or by using flat braid. Performance will be enhanced when a copper or silver-copper bus is used. The width to thickness ratio required will vary between systems, but greater than or equal to 4 will satisfy most systems.

Table 6. Guidelines for Gates and Flip-Flops Using Advanced Schottky TTL

ITEM	GUIDELINE
Data input rise and fall times	Reduce input rise and fall times as driver output impedance increases. Rise and fall times should be equal to or less than 15 ns/V and essentially free of noise ripple.
Unused input of AND and NAND gates and unused preset and clear inputs of flip-flops	Tie the unused input of AND and NAND gates and the unused preset and/or clear inputs of flip-flops as follows: <ol style="list-style-type: none"> 1. Directly to V_{CC}, if the input voltage rating of 5.5 V maximum is not exceeded. 2. Through a resistor equal to or greater than 1 kΩ to V_{CC}. Several inputs can be tied to one resistor. 3. Directly to a used input of the same gate, if maximum fanout of driving device will not be exceeded. Only the high-level loading of the driver is increased. 4. Directly to an unused gate output, if the gate is wired to provide a constant high-level output. Input voltage should not exceed 5.5 V.
Unused input of NOR gates	Tie unused input to used input of same gate, if maximum fanout of driving device will not be exceeded or tie unused input to ground.
Unused gates	Tie input of unused NAND and NOR gates to ground for lowest power drain. Tie inputs of unused AND gates high and use output for driving unused AND or NAND gate inputs.
Increasing gate/buffer fanout	Connect gates of same package in parallel.
Clock pulse of flip-flops	Drive clock inputs with a TTL output. If not available, rise and fall times should be less than 50 ns/V and free of ripple noise spikes.

SUPPLY VOLTAGE RIPPLE

Ripple in the supply voltage is generally considered a part of the supply voltage regulation. However, when combined with other effects (e.g., slow rise times), ripple voltage is more significant.

The effect of ripple voltage V_R can appear on either the supply voltage V_{CC} or the ground supply GND. When ripple appears on the supply voltage, it causes modulation of the input signal. The extent of the effect depends upon circuit parameters and source impedance.

The turning on of transistor Q5, shown in Figures 12 and 13, is controlled by the voltage at the base of transistor Q2 with respect to ground in accordance with the formula:

$$V_B = V_{BE} \text{ of } Q2 + V_{BE} \text{ of } Q3 + V_{BE} \text{ of } Q5$$

When ripple voltage is modulated onto the input voltage, the amplitude depends on the source impedance (Figure 29). The amplitude can be determined by the following equation:

$$\begin{aligned} \Delta V_R &= V_R \left(\frac{R1/\beta}{R1/\beta + R2} \right) \\ &= V_R \left(\frac{R1}{R1 + \beta R2} \right) \end{aligned}$$

where R1 = source impedance
β = gain of transistor Q1.

Ripple voltage has the effect of adding extra pulses to the input signal (Figure 30). When ripple voltage appears in the ground supply, the threshold voltage is modulated and extra pulses occur (Figure 31).

Although decreasing the source impedance will reduce the effects of ripple voltage, it cannot be eliminated entirely because the emitter-base junction has an apparent resistance of approximately 30Ω . Because of cancellation between the driving gate and the driven gate, low-frequency ripple is not a problem.

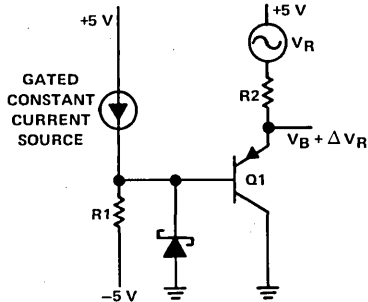


Figure 29. Effect of Source Impedance on Input Noise

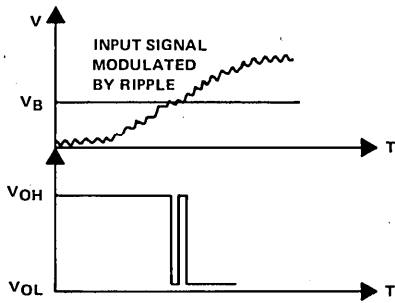


Figure 30. Spurious Output Produced by Supply Voltage Ripple

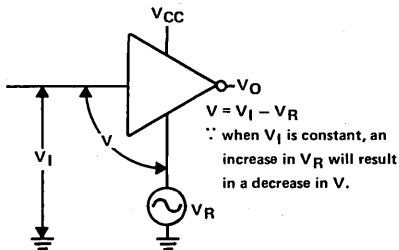


Figure 31. Effect of Ground Noise on Noise Margin

NOISE CONSIDERATIONS

Extraneous voltages and currents (called noise) introduced into a digital logic circuit are discussed in the following paragraphs. Figure 32(a) is a typical digital logic

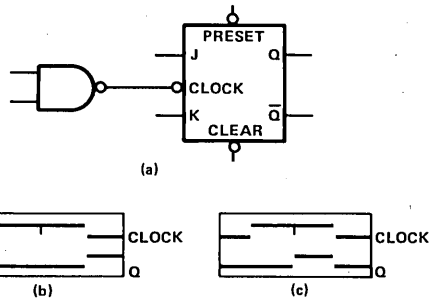


Figure 32. Typical Logic Circuit with Noisy Input

circuit consisting of a NAND gate and a J-K flip-flop. When a small noise pulse is coupled onto the clock input [(Figure 32(b)), the flip-flop does not respond and the Q output is correct. However, when a large noise pulse is coupled onto the clock input [(Figure 32(c)), the flip-flop sees the pulse as a clock transition and an erroneous Q output occurs. Therefore, it is essential to protect digital logic circuits from noise.

Noise Types and Control Methods

The noise types encountered in digital logic systems, their source, and the method of controlling them are as follows:

1. External noise — External noises radiated into the system. The sources include circuit breakers, motor brushes, arcing relay contacts, and magnetic-field-generating. The methods of controlled to be considered are shielding, grounding, or decoupling.
2. Power-line noise — Noise coupled through the ac or dc power distribution system. The initial sources and controlling methods are the same as for external noise.
3. Cross talk — Noise induced into signal lines from adjacent signal lines. Controlling methods to consider are shielding, grounding, decoupling, and, where possible, increasing the distance between the signal lines.
4. Signal-current noise — Noise generated in stray impedances throughout the circuit. The controlling methods to consider are shielding, grounding, decoupling, and, where possible, reduction of stray capacitance in the circuit.
5. Transmission-line reflections — Noise from unterminated transmission lines that cause ringing and overshoot. The method of control is to use, where possible, terminated transmission lines.
6. Supply-current spikes — Noise caused by switching several digital loads simultaneously. The controlling method is to design, where possible, the system so that digital loads are not switched simultaneously.

Shielding

In addition to its own internally generated noise, electrical equipment must operate in an extremely noisy environment. Noise pulses, which may come from a number of sources, consist of an electrostatic field, and electromagnetic field, or both. The noise waveform must be prevented from entering the equipment. This is accomplished by shielding. Since the noise fields are usually changing at a rapid rate, the shield required to exclude them may be very small. For effective exclusion, the sensitive circuits must be completely shielded.

Aluminum or similar materials are effective in stopping electrostatic noise. However, only a ferrous metal can successfully protect equipment against magnetic fields. While it is helpful to connect the system to earth ground, the shield system must be complete and must be grounded to the system ground to prevent the shield from coupling noise into the system.

External noise may be conducted into the system by the power lines. Decoupling and filtering of these lines should be standard design procedure.

Grounding and Decoupling

The total propagation delay is of secondary importance in generation of internal noise. The actual transition time determines the amplitude and frequency spectrum of the generated signal at the higher harmonics. Application of the Fourier integral to series 'ALS/'AS waveforms shows frequency components of significant amplitude that exceed 100 MHz. Because of the frequency spectrum generated when an 'ALS/'AS device switches, a system using these devices must consider problems caused by radio frequency (RF) even though the repetition rates may be only a few megahertz. The transient currents generated by charging capacitors, changes in the levels of dc, line driving, etc., must be considered. In Figure 33 for example, a gate driving a transmission line is represented by a voltage source E, having an output impedance Z_S connected to an impedance Z_0 , and loaded with a resistance R_L .

Until after a reflected pulse returns from the termination of the transmitting device, line termination is not a factor in drive current. In a practical TTL circuit, the line termination must be high relative to the line impedance. For

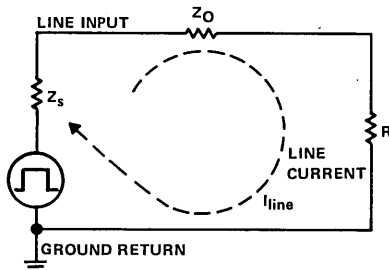


Figure 33. Diagram Representing a Gate Driving a Transmission Line

explanation purposes, assume that the source voltage is 5 V in amplitude, the output impedance of the source is 50 Ω and the line impedance is 50 Ω . When the source voltage makes the transition from 0 V to 5 V, the voltage across the input of the line V_I is determined by the following equation:

$$V_I = E \frac{Z_0}{Z_S + Z_0} = 2.5 \text{ V}$$

where E = source voltage
 Z_0 = line impedance
 Z_S = source impedance

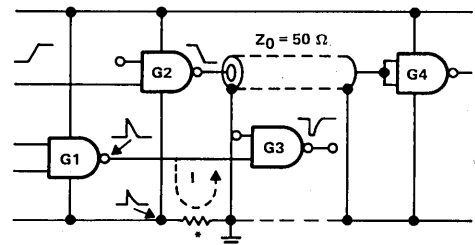
For the 50 Ω line to become charged, the current that must flow onto the line is determined by the following equation:

$$I_{\text{line}} \frac{V_{\text{in}}}{Z_0} = \frac{2.5}{50} = 50 \text{ mA}$$

In addition, this current flows in the ground return, which, in this case, is the transmission-line ground. If the line and return are originated and terminated close to the driving and receiving devices, there is no discontinuity in the line. Where the ground is poorly returned, the current flow sees the discontinuity in the cable as a high impedance and a noise spike is generated (i.e., the ground current sees a low impedance and a current cancellation if the ground is properly carried through and, if not, it sees a high impedance). Figure 34 presents a specific example. Assume that the gate driving the line is switched from the high to low state. Current flow is indicated by the arrow marked with an I. Since the line is improperly returned to the driver, a pulse is developed across the impedance. A possible consequence is the false output of gate 3 (G3).

If the ground return is properly connected, the proper results are obtained. The impedance discontinuity is eliminated and current cancellation occurs at the ground point. Undesirable voltage spikes are then eliminated. Two empirical rules to reduce transmission-line currents have been established and have been found to be effective (Figure 35).

1. Carry all returns, including twisted pair and coaxial cables, to a good ground termination. Ground line returns close to the driving and receiving devices.



Impedance of poor ground return

Figure 34. Noise Generation Caused by Poor Transmission-Line Return

- Decouple the supply voltage of line-driving and line-receiving gates with a 0.1- μF disk ceramic capacitor.

As the devices change state, current levels change because of the different device currents required in each state, the external loading, the transients caused by charging and discharging capacitive loads, and the conduction overlap in the totem-pole output stage. When a gate changes states, its internal supply current changes from high to low (these values are stated on the data sheet for each device). In addition, any capacitance, stray or otherwise, must be charged or discharged for a logic state change. The capacitance must be charged by a current determined by

$$I = C \frac{dv}{dt} \quad (4)$$

If the total stray capacitance on a gate output, the logic-level voltage excursion, and the associated rise or fall times are known, then the ideal-case instantaneous current during the transition can be calculated.

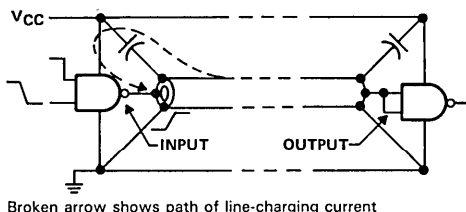
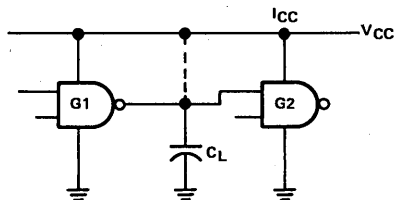


Figure 35. Ideal Transmission-Line Current Handling

From Eq. (4) it can be determined that the current transient for charging load capacitance will increase with higher speed TTL circuits. Therefore, the Series 54ALS/74ALS devices will have lower transient current than the Series 54AS/74AS devices. Another parameter that should be considered is the value of R7 (shown in Figures 12 and 13). Resistor R7 acts as a limit on the charging current.

The current required for charging load capacitance C_L (Figure 36) is supplied by the supply voltage when the transition is from logic low to logic high at the output of gate 1 (G1). When the output of G1 goes from high to low,



C_L includes all capacitance: stray, device, etc.

Figure 36. Circuit with Effective Capacitive Loading

the load capacitance is shorted to ground by transistor Q5 (shown in Figures 12 and 13) and has no effect on supply current.

A characteristic common to all TTL totem-pole output stages contributes an additional current transient when the output changes from a logic low to a logic high. This transient, or spike, is caused by the overlap in conduction of the output transistors Q7 and Q5 (shown in Figures 12 and 13). The situation arises because transistor Q7 can turn on faster than transistor Q5 can turn off. This places a direct circuit consisting of transistors Q7 and Q5 and resistor R4 between supply voltage and ground. For all series 'ALS TTL circuits, the maximum possible peak current can be determined by

$$I_{CCmax} = \frac{V_{CC} - V_{CEQ6} - V_{BEQ7} - V_{CEQ5}}{R7}$$

However, due to the active turnoff circuit (consisting of R5, R6, and Q4), Q5 will be only slightly in the linear region and the current spike will be less.

The total supply-current switching transient is then a combination of three major effects: the difference in high-level and low-level supply current, the charging of load capacitance, and the conduction overlap. Tests were performed to demonstrate these effects. The results are shown in Figure 37. Six types of series TTL devices were tested with no load (i.e., the oscilloscope was connected to the output only when measuring V_O and the photographs were double exposed). This was to approximate the effects of conduction overlap isolated from the transient caused by charging load capacitance. Different vertical scales were used on some of the photographs.

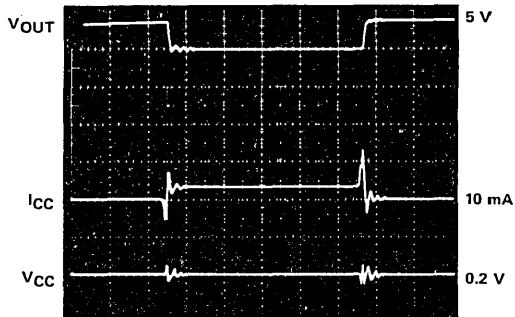
The results are almost as predicted. The low-power devices have the lower transients. Since it is the fastest circuit, the SN74AS00 device should be highest. However, a decrease is shown, and the reason for the decrease is explained (Figure 39). The additional circuits to reduce conduction overlap of the output transistors result in a smaller transient even though the typical switching time is 1.7 ns compared to 9 ns for the Series 54/74LS.

The second series of tests shown in Figure 37 cover a capacitive load of .50 pF. For this test, all of the supply current transient peaks increase in amplitude and width.

Because of the larger transient currents, voltage spikes on the supply voltage measured at the IC package are also increased.

From these tests, it can be concluded that the condition to be avoided (the only one that can be avoided) is unnecessary stray capacitance in circuit wiring. The charging of load capacitance, in most cases, overshadows the other two effects with respect to noise produced on the supply voltage line by switching current transients.

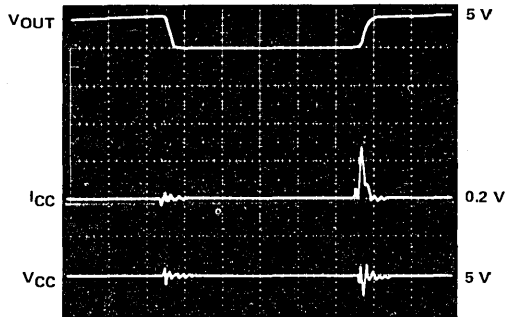
The flow paths of these currents have been investigated to determine the grounding and decoupling necessary to counteract their effects. Supply voltage decoupling may be accomplished by one of two methods. Maintaining low impedance from the individual circuit supply voltage to



a) SN74S00 no load



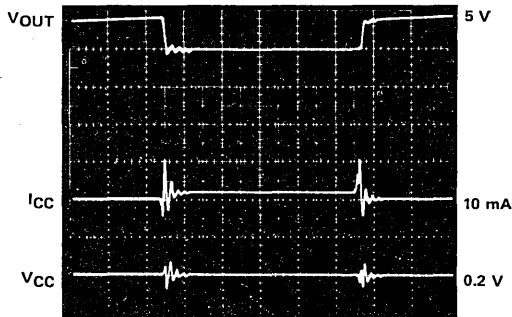
b) SN74S00 load: $C_L = 50 \text{ pF}$



c) SN74LS00 no load



d) SN74LS00 load: $C_L = 50 \text{ pF}$



e) SN74AS00 no load

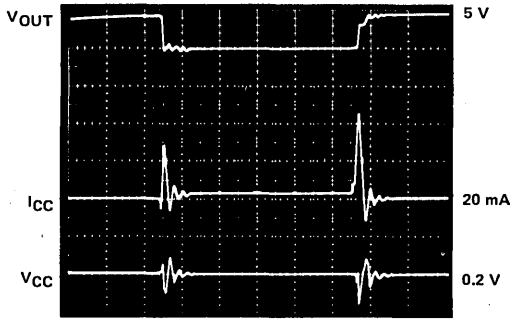


f) SN74AS00 load: $C_L = 50 \text{ pF}$

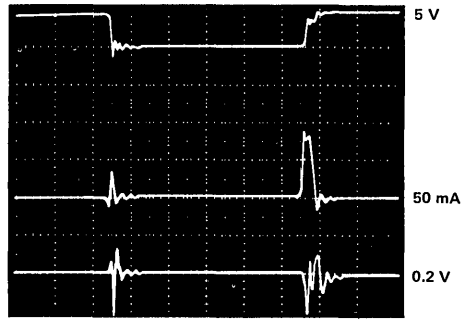
NOTES: 1. $V_{CC} = 5 \text{ V}$
2. Sweep is 50 ns/division

3. Rise and fall times of input pulse are 1 ns
4. Vertical scales are in units shown per division

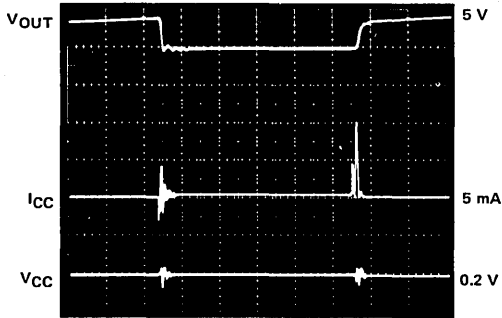
Figure 37(a). Supply-Current Transient Comparisons



g) SN74AS1000 no load



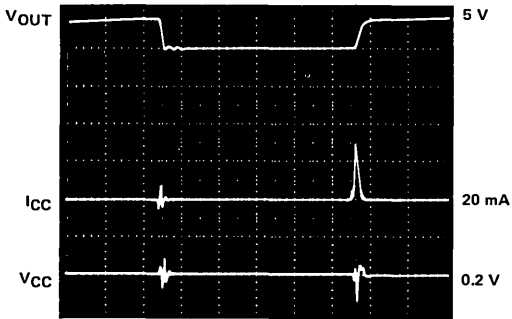
h) SN74AS1000 load: $C_L = 50 \text{ pF}$



i) SN74ALS00A no load



j) SN74ALS00A load: $C_L = 50 \text{ pF}$



k) SN74ALS1000A no load



l) SN74ALS1000A load: $C_L = 50 \text{ pF}$

NOTES: 1. $V_{CC} = 5 \text{ V}$
2. Sweep is 50 ns/division

3. Rise and fall times of input pulse are 1 ns
4. Vertical scales are in units shown per division

Figure 37(b). Supply-Current Transient Comparisons

ground is common to both methods. In the first method, the supply voltage line may be considered as a transmission line back to a low impedance supply. The positive bus can be laminated with a ground bus to form a strip transmission line of extremely low impedance. This line can be electrically approximated with lumped capacitances as shown in Figure 38. The inductances are usually a distributed component which must be minimized to lower the line impedance.

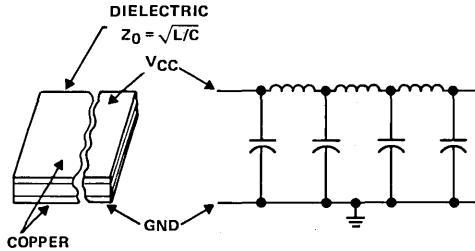


Figure 38. Transmission-Line Power Buses

The second method is to consider the supply voltage bus as a dc connecting element only and to provide a low-impedance path near the devices for the transient currents to be grounded (Figure 39).

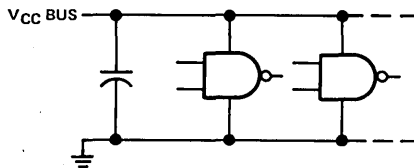


Figure 39. Capacitive Storage Supply Voltage System

For effective filtering and decoupling, the capacitors must be able to supply the change in current for a period of time greater than the pulse width of this current. Since the problem is essentially one of dc changes due to logic state coupled with high-frequency transients associated with the changes, two different values of time constant must be considered. Capacitors combining the high capacitance required for long periods with the low series reactance required for fast transients are prohibitive in cost and size. A good compromise is the arrangement shown in Figure 40.

The typical component values may be found for the RF capacitor C1 by assuming that the parameters have common values as follows:

$$\begin{aligned}\Delta I_{CC} &= 50 \text{ mA} \\ \Delta V &= 0.1 \text{ V} \\ \Delta T &= 20 \text{ ns}\end{aligned}$$

Then the equation is as follows:

$$\begin{aligned}C1 &= \frac{\Delta I_{CC}}{\Delta V/\Delta T} = \frac{(50)(20) \times 10^{-12}}{0.1/(20 \times 10^{-9})} \\ &= \frac{50 \times 10^{-3}}{0.1} = 10,000 \times 10^{-12} \\ &= 0.01 \mu\text{F}\end{aligned}$$

The same method may be used for the low-frequency capacitor C2. However, the factor ΔT , which was a worst-case transient time for calculating C2, now becomes a bit ambiguous. An analysis of the current cycling on a statistical basis is the best method in all but the simplest systems. The recommended procedure is to decouple using 10 μF to 50 μF capacitors.

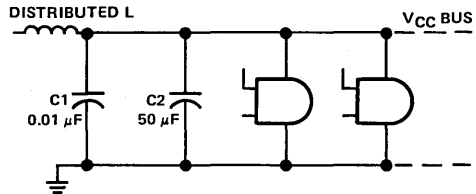


Figure 40. Commonly Used Power Distribution and Decoupling System

A discrete inductance of 2 μH to 10 μH is sometimes used for additional decoupling. However, its benefits are questionable and its usefulness should be evaluated for the individual system. The low-pass filter formed must be capable of keeping the transients confined and off the distribution bus. The possibility of resonance in the inductor or LC combination must be considered.

Noise spikes on the supply voltage line that do not force the gate output below the threshold level do not present a serious problem. Downward spikes as large as 3 V can be tolerated on the supply voltage line without propagating through the logic system. The system designer can be confident that supply voltage noise can be handled even with minimal consideration.

Ground noise, however, cannot be treated lightly. Pulses on a high-impedance ground line can easily exceed the noise threshold. Only if a good ground system is maintained can this problem be overcome. If proper attention is paid to the ground system, noise problems can be minimized.

The concept of a common-ground-plane structure as used in RF and high-speed digital systems is quite different from the concept of the common-ground point as used in low-frequency circuits. The more closely the chassis and ground can approach to being an integral unit, the better the noise suppression characteristics of the system. Consequently, all

parts of the chassis and ground bus system must be bound tightly together both electrically and mechanically. Floating or poorly grounded sections not only break the integrity of the ground system, but may actually act as a noise distribution system.

For grounds and decoupling on printed circuit boards, the most desirable arrangement is a double-clad or multilayer board with a solid ground plane or a mesh. Where component density prohibits this, the ideal should be relaxed only as far as necessary. Cross talk and ground noise can be reduced on large boards with a ground plane. Some suggestions for board grounds where a plane is not practical are as follows:

1. Use as wide a ground strap as possible.
2. Form a complete loop around the board by bringing both sides of the board through separate pins to the system ground.

The supply voltage line can provide part of the ground mesh on the board, provided it is properly decoupled. For a TTL system, a good guideline is 0.01 μF per synchronously driven gate and at least 0.1 μF for each 20 gates, regardless of synchronization. This capacitance may be lumped, but is more effective if distributed over the board. A good rule is to permit no more than 5 inches of wire between any two package supply-voltage points. Radio-frequency-type capacitors must be used for decoupling. Disk ceramics are best. It is sometimes a good practice to decouple the board from the external supply-voltage line with a 2.2 μF capacitor. However, this is optional and the RF capacitors are still required. In addition, it is recommended that gates driving long lines have the supply voltage decoupled at the gate supply voltage terminal and that the capacitor ground, device ground, and transmission-line ground be connected to a common point.

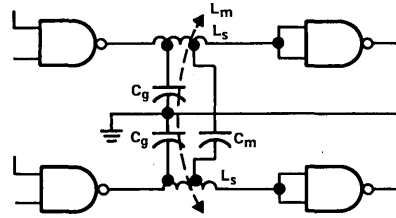
Cross Talk

When currents and voltages are impressed on a connecting line in a system, it is impossible for adjacent lines to remain unaffected. Static and magnetic fields interact and opposing ground currents flow, creating linking magnetic fields. These cross-coupling effects are lumped together and called cross talk.

Back-Panel Interconnections

Interconnecting signal lines can be grouped into three broad categories: coaxial lines, twisted-pair lines, and straight wire lines. Because of the low impedance and shielding characteristics of coaxial cable, its cross talk is minimal and is not a problem with TTL.

Figure 41 illustrates a practical type of signal transmission line. The mutual reactances L_m and C_m which form the noise coupling paths and the line parameters L_s and C_g which govern the line impedance, will vary with the type of line used. Since cross talk is a function of the ratio of the mutual impedances to the line characteristic impedances, the selection of transmission-line type must be at least partially a factor in cross-talk considerations.

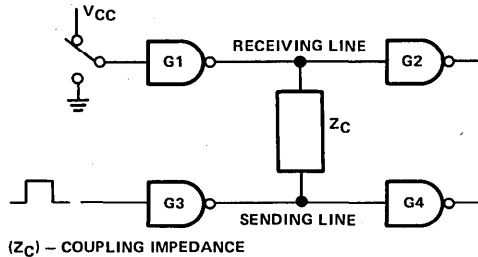


ALL GATES SN74ALS00

Figure 41. Equivalent Circuit for Sending Line

The use of direct-wired connections is the simplest and lowest cost method, but they are also the poorest for noise rejection. If the lead is not cabled tightly together with similar leads, direct leads up to 12 inches in length can be used.

When the length of the signal line is increased, the line impedance is seen by the driving and receiving gates. As shown in Figure 42, a pulse sent along the sending line G3 and G4 will be coupled via the coupling impedance Z_c onto the receiving line G1 and G2, which can be in either of the two logic states. The extent to which cross talk will occur depends on the type of lines used and their relationship to each other.



(Z_c) - COUPLING IMPEDANCE

Figure 42. Equivalent Circuit for Cross Talk

The voltage impressed on the sending line by gate G3 is determined by the equation:

$$V_{SL} = \frac{V_{G3}Z_0}{R_{S3} + Z_0} \quad (5)$$

where

V_{G3} = open-circuit logic voltage swing generated by gate G3

R_{S3} = output impedance of gate G3

Z_0 = line impedance

V_{SL} = voltage impressed on the sending line.

The relationship for the equation is illustrated in Figures 43 and 44.

The coupling from the sending line to the receiving line can be represented by taking coupling impedance Z_c into

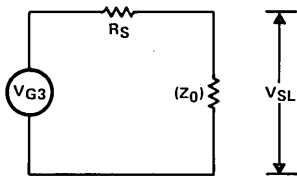


Figure 43. Capacitive Cross Talk Between Two Signal Lines

account. An equivalent circuit to represent the coupling from the sending line to the receiving line is shown in Figure 44.

As the voltage impressed on the sending line propagates farther along the line, it can be represented as voltage source V_{SL} with a source impedance of Z_{01} (Figure 45). V_{SL} is then coupled to the receiving line via the coupling capacitance, where the impedance looking into the line is line impedance in both directions. Therefore the equation becomes

$$V_{RL} = V_{SL} \frac{\frac{Z_0}{2}}{(1.5 Z_0 + Z_c)}$$

The voltage impressed on the receiving line (V_{RL}) then propagates along the receiving line to gate G2 which can be considered as an open circuit and voltage doubling occurs. Therefore:

$$V_{in(2)} = 2 V_{RL} = V_{G3} \left(\frac{1}{1.5 + \frac{Z_c}{Z_0}} \right) \left(\frac{Z_0}{RS3 + Z_0} \right)$$

In the switching period, the transistor has a very low output impedance. Then $RS3 \ll Z_0$ and $V_{in(2)}$ can be simplified to the following:

$$V_{in(2)} = V_{G3} \left(\frac{1}{1.5 + \frac{Z_c}{Z_0}} \right)$$

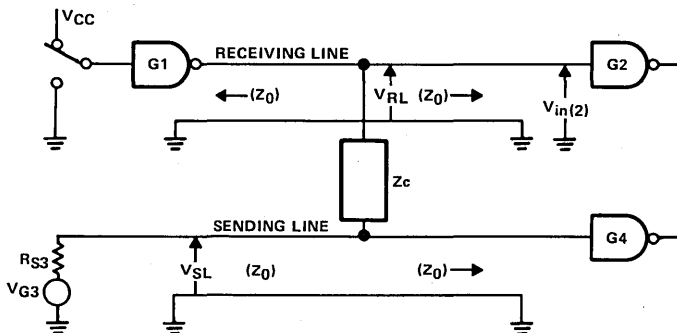


Figure 44. Coupling Impedances Involved in Cross Talk

The term $V_{in(2)}/V_{G3}$ can be defined as the cross-talk coupling constant.

The worst-case for signal line cross talk occurs when sending and receiving lines are close together but widely separated from a ground return path. The lines then have a high characteristic impedance and a low coupling impedance.

For example, if we assume a coupling impedance of 50 pF at 150 MHz with a line impedance of approximately 200 Ω then:

$$\frac{V_{in(2)}}{V_{G3}} = 0.62$$

This level is unsatisfactory because none of the very high-speed logic circuits has a guaranteed noise margin greater than one-third of the logic swing. Such potential cross talk can be avoided by not using the close spacing of conductors.

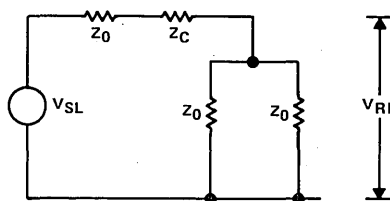


Figure 45. Equivalent Cross-Talk Network

Mutual coupling can be reduced by using coaxial cable or shielded twisted pairs. When mutual inductance and capacitance are decreased, line capacitance is increased and imposes restrictions on the driver. Coaxial cable combines very high mutual impedance with low characteristic impedance and shielding. It effectively eliminates cross talk, but is necessary in only the noisiest environments. Twisted pairs are adequate for most applications and are typically less expensive and easier to use.

Printed Circuit Card Conductors

Signal interconnections on a two-sided or multilayer printed circuit card can be grouped into two general categories: microstrip lines and strip lines. The microstrip line (Figure 46) consists of a signal conductor separated from a ground plane by a dielectric insulating material. A strip line (Figure 47) consists of a signal conductor within a dielectric insulating material and the conductor being centered between two parallel conductor planes. The important features of these type of printed circuit conductors are that the impedances are highly predictable, can be closely controlled, and the process is relatively inexpensive because standard printed circuit board manufacturing techniques are used. Typical impedances of these types of conductors with respect to their physical size and relative spacings are shown in Tables 7 and 8.

Table 7. Typical Impedance of Microstrip Lines

Dimensions		Line Impedance Z_0 (Ω)	Capacitance per Foot (pF)
H (mils)	W (mils)		
6	20	35	40
6	15	40	35
15	20	56	30
15	15	66	26
30	20	80	20
30	15	89	18
60	20	105	16
60	15	114	14
100	20	124	13
100	15	132	12

Relative dielectric constant ≈ 5

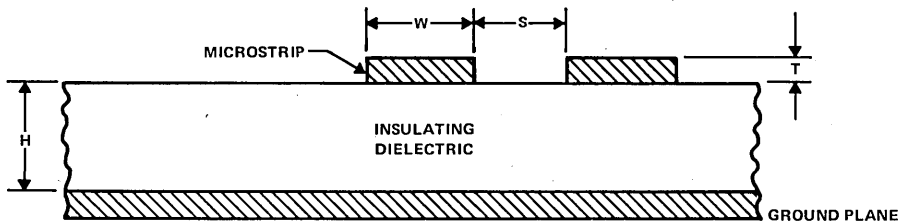


Figure 46. Microstrip Line

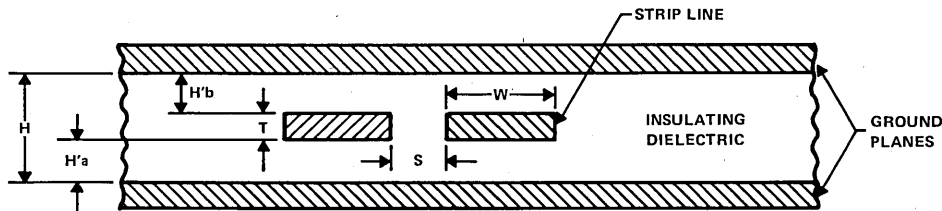


Figure 47. Strip Line

Table 8. Typical Impedance of Strip Lines

Dimensions		Line Impedance Z_0 (Ω)	Capacitance per Foot (pF)
$H'a = H'b =$ (mils)	W (mils)		
6	20	27	80
6	15	32	70
10	20	34	67
10	15	40	56
12	20	37	57
12	15	43	48
20	20	44	48
20	15	51	42
30	20	55	39
30	15	61	35

Relative dielectric constant ≈ 5 , and $H'a = H'b$

Cross talk on a printed circuit board is also a function of the mutual reactances and the line parameters which govern the line impedance. A microstrip line and a strip line are, by definition, conductors placed relatively close to a ground plane. Therefore, they have at least one inherent property which tends to reduce cross talk. In addition, the thickness (H) of the dielectric and the spacing (S) of the conductors can be implemented selectively to reduce the amount of possible cross talk. The effects of these two dimensions on cross talk have been evaluated and are shown graphically in Figure 48. The data shown can be used to estimate the maximum crosstalk which will be encountered under the most unfavorable conditions.

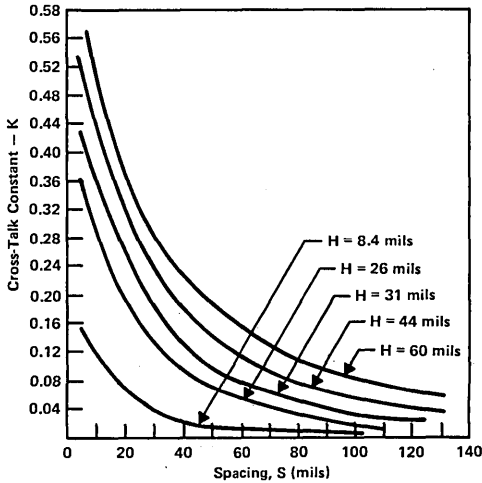


Figure 48. Line Spacing Versus Cross-Talk Constant

Transmission-Line Driving Reflections

When the interconnections used to transfer digital information become long enough so that line propagation delay is equal to or greater than the pulse transition times, the effects of reflections must be considered. These reflections are created because most TTL interconnections are not terminated in their characteristic impedance. Reflections lead to reduced noise margins, excessive delays, ringing, and overshoot. Some method must be used to analyze these reflections. Because neither the gate input nor output impedance is linear, basic transmission-line equations are applicable but unwieldy. Transmission-line characteristics of TTL interconnections can be analyzed by using a simple graphic technique.

Figure 49 shows piecewise linear plots of a gate input and both (logic-high and logic-low) states of the output for a typical TTL device. The output curves are plotted with positive slopes. The input is inverted because it is at the receiving end of a transmission line. The logic-high and logic-low intersections are indicated on the plot. These points are the steady-state values which will be observed on a lossless transmission line (Figure 50).

Figure 50 shows a typical TTL interconnection using a twisted-pair cable which, in this example, has a characteristic impedance of approximately $30\ \Omega$. To evaluate a logic-high to logic-low 'AS transition see Figures 51 and 52. The equation $-1/Z_0$ ($Z_0 = 30\ \Omega$), which represents the transmission line, is superimposed on the output characteristic curves in the Bergeron plot. Since evaluation of a logic-high to logic-low transition is desired, the $-1/Z_0$ line starts at the point of intersection of the impedance curves of the input and output for a logic-high state. The slope $-1/Z_0$ then proceeds toward the logic-low output curve. At time t_0 , the driver output voltage is determined by the intersection of

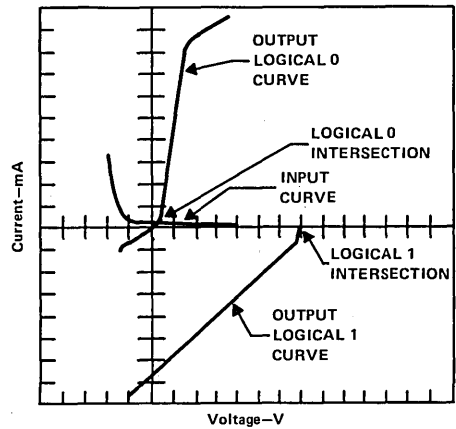


Figure 49. TTL Bergeron Diagram

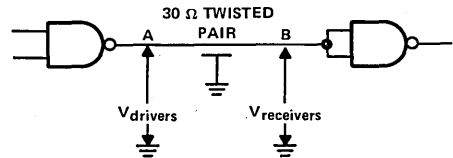


Figure 50. 'ALS/'AS Driving Twisted Pair

$-1/Z_0$ and the logic-low output curve (1.2 V). The transmission-line slope now becomes $1/Z_0$ and is drawn toward the input curve. At time t_1 [$t_{(n+1)} - t_n =$ time delay of line], the receiving gate sees -0.7 V . Now the line slope changes back to $-1/Z_0$ and the output curve for a logic low is approached. This action continues until the logic-low intersection is reached. Figure 52 plots driver and receiver voltages versus time for this example.

A logic-low to logic-high transition is treated in approximately the same manner (Figure 53). The Bergeron line $-1/Z_0$ starts at the intersection for a logic low. At time t_0 , the driver output rises to 2.2 V and, at time t_1 , the receiving gate input goes to approximately 4.35 V. Both output and input voltages are plotted in Figure 54.

Figures 55 through 58 illustrate 'ALS transitions and are treated in the same manner as the 'AS.

The scope photographs in Figures 59 through 66 show the effectiveness of the graphic techniques. In most cases, the calculated and experimental values of voltage steps agree within reason. The ringing that appears for the open wire is not immediately obvious. This is because the input and output curves in this region lie practically along the positive horizontal axis. At the scale used for graphic analysis, it is difficult to go much beyond the first few reflections. The graphic analysis is idealized and stray capacitance and inductance are not considered.

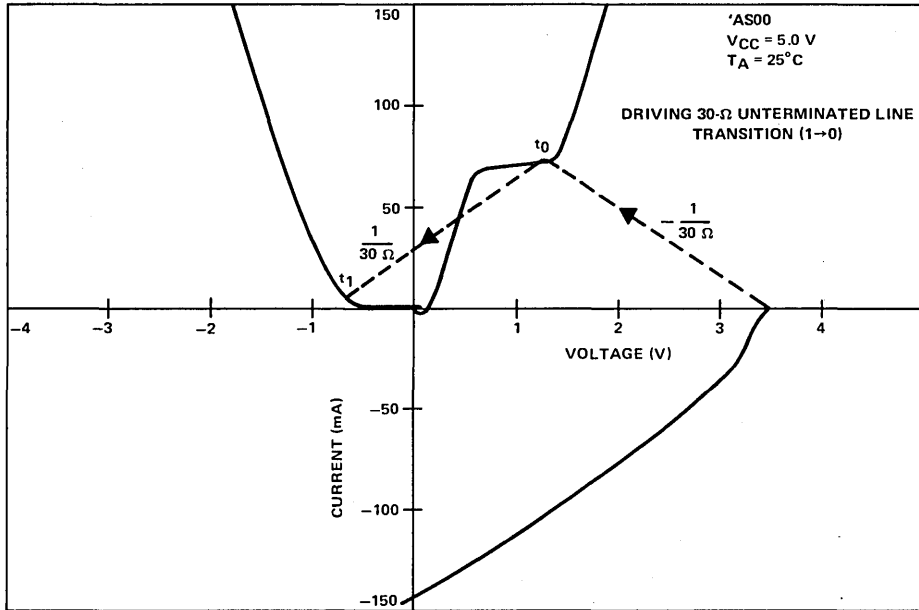


Figure 51. 'AS -ve Transition Bergeron Diagram

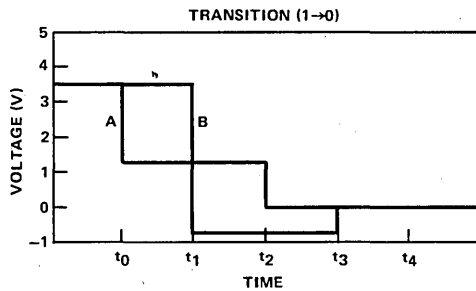


Figure 52. 'AS -ve Voltage/Time Plot

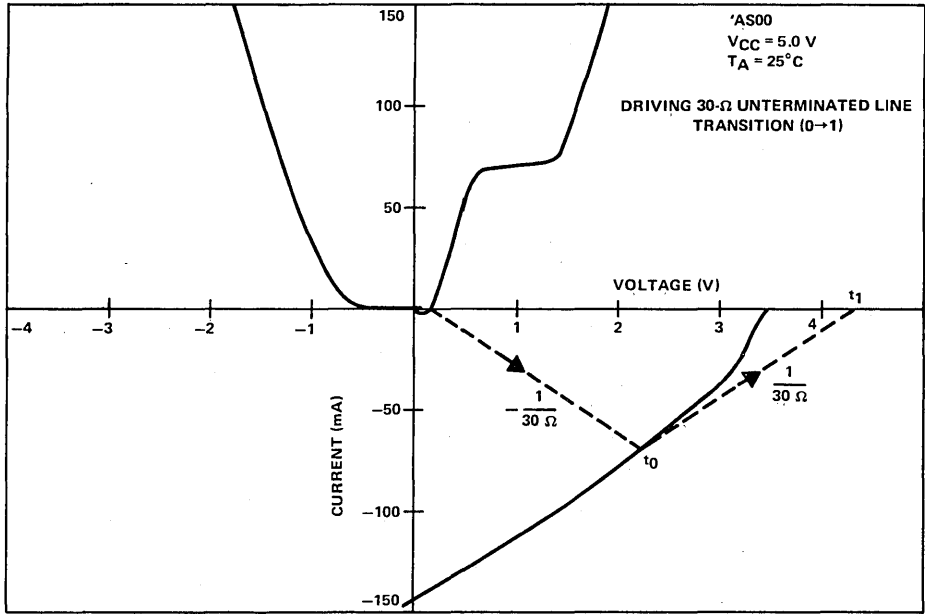


Figure 53. 'AS +ve Transition Bergeron Diagram

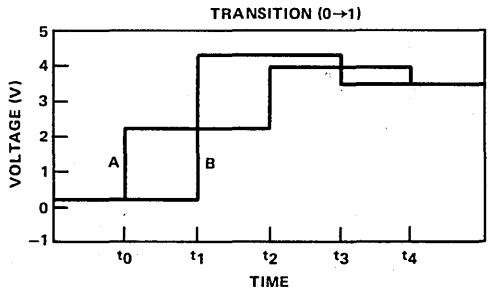


Figure 54. 'AS +ve Voltage/Time Plot

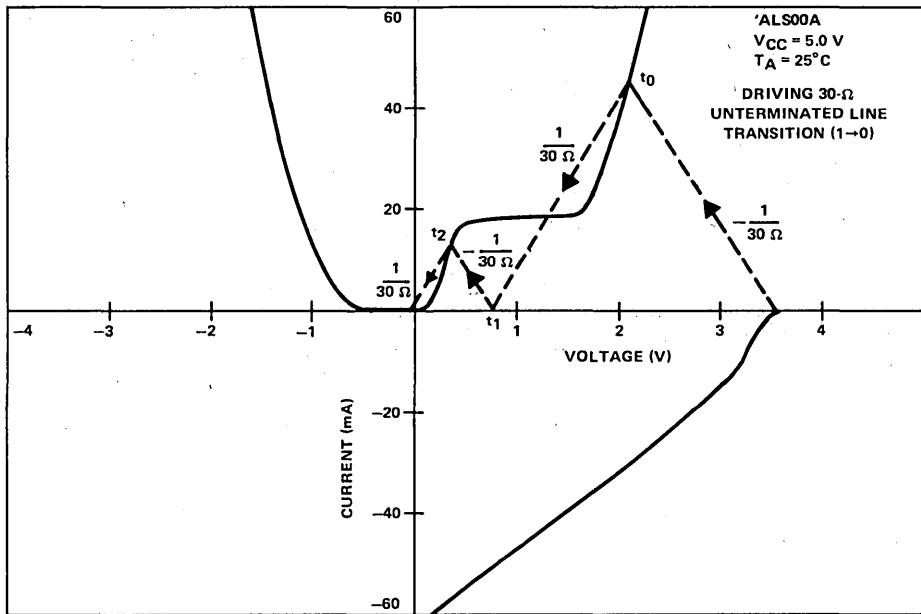


Figure 55. 'ALS - ve Transition Bergeron Diagram

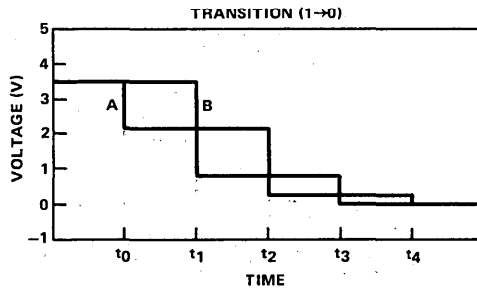


Figure 56. 'ALS - ve Voltage/Time Plot

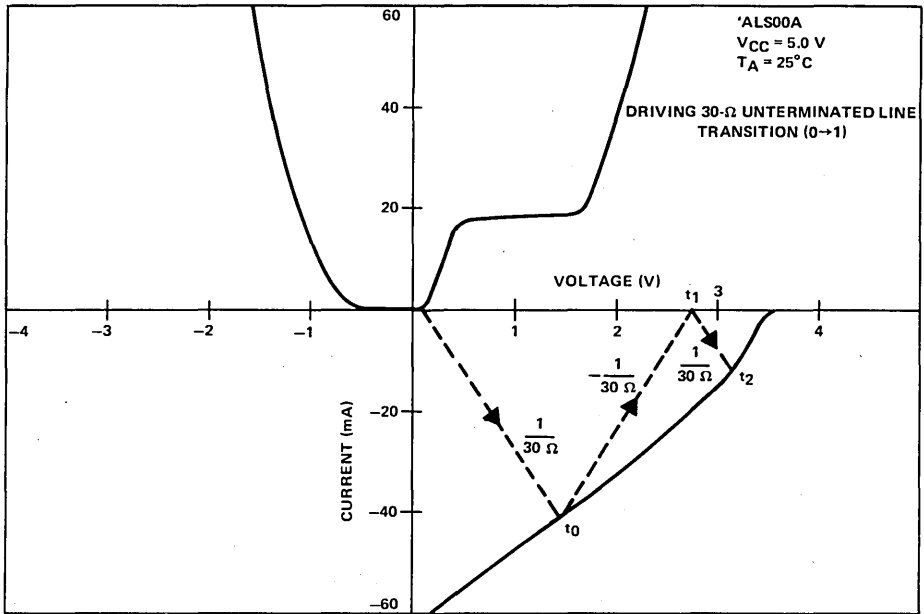


Figure 57. 'ALS + ve Transition Bergeron Diagram

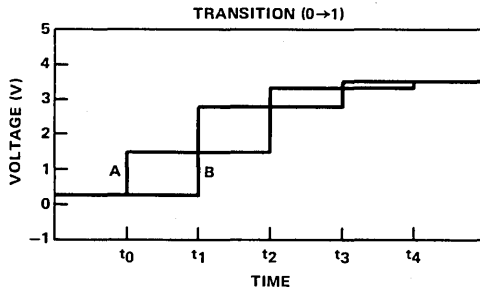


Figure 58. 'ALS + ve Voltage/Time Plot

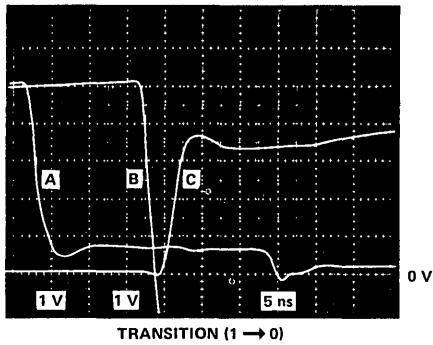


Figure 59. Oscilloscope Photograph of 'AS001 -ve Transition Using 50-Ohm Line

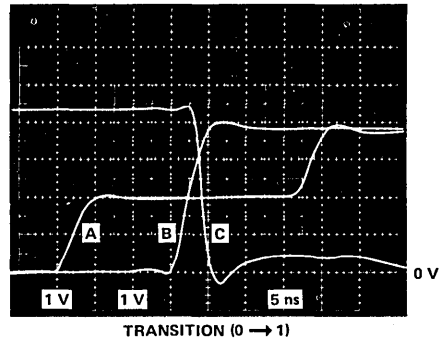


Figure 62. Oscilloscope Photograph of 'AS00 +ve Transition Using 25-Ohm Line

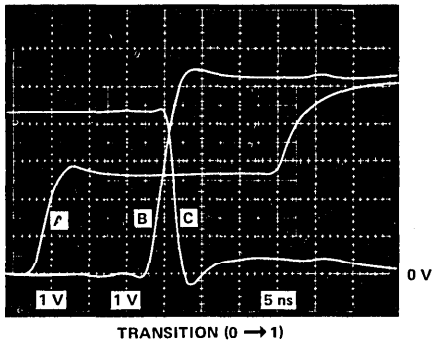


Figure 60. Oscilloscope Photograph of 'AS00 +ve Transition Using 50-Ohm Line

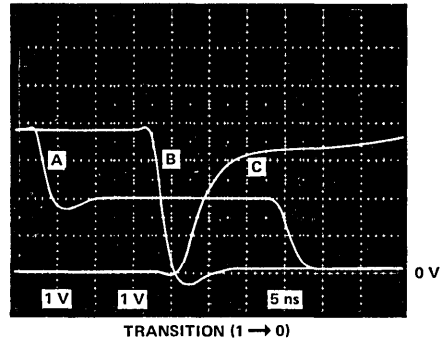


Figure 63. Oscilloscope Photograph of 'ALS00A -ve Transition Using 50-Ohm Line

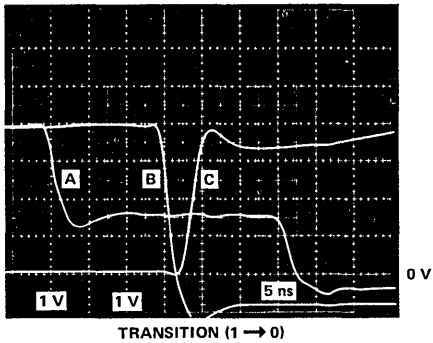


Figure 61. Oscilloscope Photograph of 'AS00 -ve Transition Using 25-Ohm Line

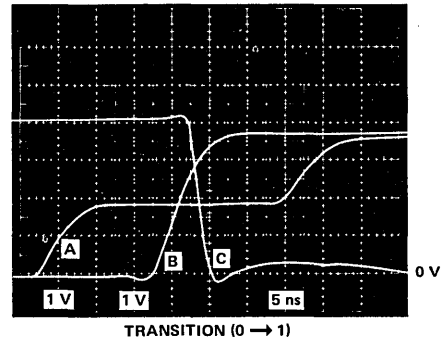


Figure 64. Oscilloscope Photograph of 'ALS00A +ve Transition Using 50-Ohm Line

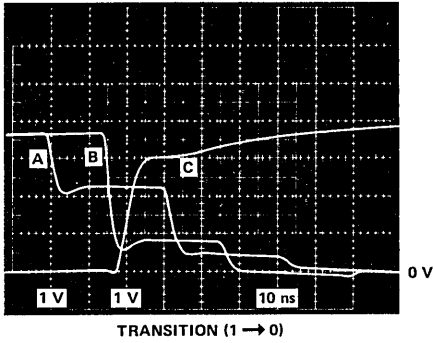


Figure 65. Oscilloscope Photograph of 'ALS00A -ve Transition Using 25-Ohm Line

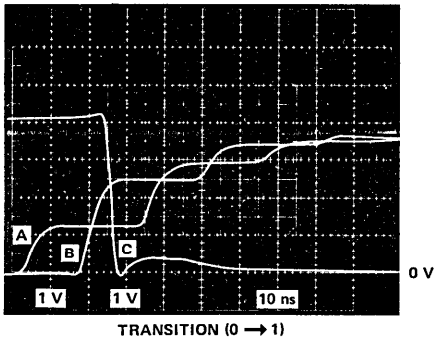


Figure 66. Oscilloscope Photograph of 'ALS00A +ve Transition Using 25-Ohm Line

References

1. W.C. Elmore and M. Sands, *Electronics Experimental Techniques*, McGraw-Hill Book Co., New York, 30ff. (1949).
2. M. Williams and S. Miller, *Series 54ALS/74ALS Schottky TTL Applications B215*, Texas Instruments Limited, Bedford, England, August 1982.

Acknowledgment

This application report is an updated version of Reference 2 with significant contributions by the technical engineering staff at Texas Instruments and particularly by Rock Cozad, Rich Moore, and Bob Strong.

Appendix A Normalized Load Factors

Normalizing output drive capability and input current requirements can be very useful to designers of systems using two or more of the TI TTL series of devices. It provides a set of load factors (input current requirements in Table A-1), which can be summed and compared directly to the fanout capability (see Table A-2) of the output being considered. The load factor values shown are valid for any input rated at one unit load.

The loading of these type of outputs can be checked from any column. However, most designs use one of the series as the basic building block and, since the tables cover each series individually, the designer has the choice of working from the column containing the normalized fanout. As an example, the designers of a system using series 'AS as the basic circuit will probably find that the use of the 'AS00 and 'AS1000 columns will suit best because both fanout and load factors are expressed for these series of devices.

The use of these simple and easy-to-remember numbers was developed within each series to make the verification of output loading a matter of counting the number of inputs connected to a particular output. When mixtures of series are used, a common denominator (normalized factor) becomes useful.

USE OF TABLES A-1 AND A-2

Every possible combination of the seven 54/74 TTL families is included in these tables. If, for example, the existing system used 74S series logic and it is desired that some of it be replaced by series 74ALS logic, a quick check should be made on whether the 'ALS can be supplied with sufficient input current. By taking the 74S row and 'ALS, column figures of 2.5 and 20 are obtained for high- and low-level loads, respectively (see Table A-1). This indicates that, for high logic levels, two and one-half 'ALS gates can be driven for each 'S series gate removed. However, if more 74S series gates are being driven by this 'ALS device, the fanout between 'ALS and 'S series gate is required, you can now use Table A-2.

The 'ALS row and the 'S column are chosen. The figures are 8 for the high-logic level and 4 for the low-logic level. In this case the lowest figure is taken so that the interconnection is reliable for both logic states. So each 'ALS gate inserted will drive 4 'S series gates.

Table A-1. Normalized Input Currents

SERIES	I/O	INPUT CURRENT (mA)	INPUT CURRENT NORMALIZED								
			'00	'H00	'L00	'LS00	'S00	'AS00	'ALS00A	'AS1000	'ALS1000A
54/7400	HI	0.04	1	0.8	4	2	0.8	2	2	2	2
54/7400	LO	1.6	1	0.8	8.89	4	0.8	3.2	16	3.2	16
54H/74H00	HI	0.05	1.25	1	5	2.5	1	2.5	2.5	2.5	2.5
54H/74H00	LO	2	1.25	1	11.11	5	1	4	20	4	20
54/74L00	HI	0.01	0.25	0.2	1	0.5	0.2	0.5	0.5	0.5	0.5
54/74L00	LO	0.18	0.11	0.09	1	0.45	0.09	0.36	1.8	0.36	1.8
54LS/74LS00	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54LS/74LS00	LO	0.4	0.25	0.2	2.22	1	0.2	0.8	4	0.8	4
54S/74S00	HI	0.05	1.25	1	5	2.5	1	2.5	2.5	2.5	2.5
54S/74S00	LO	2	1.25	1	11.11	5	1	4	20	4	20
54AS/74AS00	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54AS/74AS00	LO	0.5	0.31	0.25	2.78	1.25	0.25	1	5	1	5
54ALS/74ALS00A	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54ALS/74ALS00A	LO	0.1	0.06	0.05	0.56	0.25	0.05	0.2	1	0.2	1
54AS1000	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54AS1000	LO	0.5	0.31	0.25	2.78	1.25	0.25	1	5	1	5
54ALS1000A	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54ALS1000A	LO	0.1	0.06	0.05	0.56	0.25	0.05	0.2	1	0.2	1

Table A-1 is normally used (in combination with Table A-2) when replacing one logic family with another in an existing system.

Table A-2 is normally used when originally designing a system which employs several TTL families to optimize performance.

Table A-2. Fanout Capability (Output Currents Normalized to Input Currents)

SERIES	I/O	OUTPUT CURRENT (mA)	OUTPUT DRIVE NORMALIZED									
			'00	'H00	'L00	'LS00	'S00	'AS00	'ALS00A	'AS1000	'ALS1000A	
			*HI †LO 0.04	0.05	0.01	0.02	0.05	0.02	0.02	0.02	0.02	0.02
54/7400	HI	0.4		8	40	20	8	20	20	20	20	20
54/7400	LO	16		8	88.89	40	8	32	160	32	160	160
54H/74H00	HI	0.5		10	50	25	10	25	25	25	25	25
54H/74H00	LO	20		10	111.11	50	10	40	200	40	200	200
54L00	HI	0.1		2	10	5	2	5	5	5	5	5
54L00	LO	2		1	11.11	5	1	4	20	4	20	20
74L00	HI	0.2		4	20	10	4	10	10	10	10	10
74L00	LQ	3.6		1.8	20	9	1.8	7.2	36	7.2	36	36
54LS/74LS00	HI	0.4		8	40	20	8	20	20	20	20	20
54LS00	LO	4		2	22.22	10	2	8	40	8	40	40
74LS00	LO	8		4	44.44	20	4	16	80	16	80	80
54S/74S00	HI	1		20	100	50	20	50	50	50	50	50
54S/74S00	LO	20		10	111.11	50	10	40	200	40	200	200
54AS/74AS00	HI	2		40	200	100	40	100	100	100	100	100
54AS/74AS00	LO	20		10	111.11	50	10	40	200	40	200	200
54ALS/74ALS00A	HI	0.4		8	40	20	8	20	20	20	20	20
54ALS00A	LO	4		2	22.22	10	2	8	40	8	40	40
74ALS00A	LO	8		4	44.44	20	4	16	80	16	80	80
54AS1000	HI	40		800	4000	2000	800	2000	2000	2000	2000	2000
54AS1000	LO	40		20	222.22	100	20	80	400	80	400	400
74AS1000	HI	48		960	4800	2400	960	2400	2400	2400	2400	2400
74AS1000	LO	48		24	266.67	120	24	96	480	96	480	480
54ALS1000A	HI	1		20	100	50	20	50	50	50	50	50
54ALS1000A	LO	12		6	66.67	30	6	24	120	24	120	120
74ALS1000A	HI	2		52	260	130	52	130	130	130	130	130
74ALS1000A	LO	24		12	133.33	60	12	48	240	48	240	240

*Input Current HI

†Input Current LO

Appendix B

Letter Symbols, Terms, and Definitions

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronics Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use. The definitions are grouped into sections applying to voltages, currents, switching characteristics, and classification of circuit complexity.

VOLTAGES

- V_{IH}** **High-level input voltage**
An input voltage level within the more positive (less negative) of the two ranges of values used to represent the binary variables. A minimum value is specified which is the least-positive (most-negative) value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.
- V_{IL}** **Low-level input voltage**
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables. A maximum value is specified which is the most-positive (least-negative) value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.
- V_{T+}** **Positive-going threshold voltage**
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.
- V_{T-}** **Negative-going threshold voltage**
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.
- V_{OH}** **High-level output voltage**
The voltage at an output terminal for a specified output current I_{OH} with input conditions applied that according to the product specification will establish a high level at the output.
- V_{OL}** **Low-level output voltage**
The voltage at an output terminal for a specified output current I_{OL} with input conditions applied that according to the product specification will establish a low level at the output.
- V_{O(on)}** **On-state output voltage**
The voltage at an output terminal for a specified output current with input conditions applied that according to the product specification will cause the output switching element to be in the on state.

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.
- V_{O(off)}** **Off-state output voltage**
The voltage at an output terminal for a specified output current with input conditions applied that according to the specification will cause the output switching element to be in the off state.

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

CURRENT

- I_{IH}** **High-level input current**
The current flowing into* an input when a specified high-level voltage is applied to that input.
- I_{IL}** **Low-level input current**
The current flowing into* an input when a specified low-level voltage is applied to that input.

*Current flowing out of a terminal is a negative value.

- I_{OH}** **High-level output current**
 The current flowing into* the output with a specified high-level output voltage V_{OH} applied.
 Note: This parameter is usually specified for open-collector outputs intended to drive other logic circuits.
- I_{O(off)}** **Off-state output current**
 The current flowing into* an output with a specified output voltage applied and input conditions applied that according to the product specification will cause the output switching element to be in the off state.
 Note: This parameter is usually specified for open-collector outputs intended to drive devices other than logic circuits or for three-state outputs.
- I_{OS}** **Short-circuit output current**
 The current flowing into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).
- I_{CCH}** **Supply current, output(s) high**
 The current flowing into* the V_{CC} supply terminal of a circuit when the reference output(s) is (are) at a high-level voltage.
- I_{CCL}** **Supply current, output(s) low**
 The current flowing into* the V_{CC} supply terminal of a circuit when the reference output(s) is (are) at a low-level voltage.

DYNAMIC CHARACTERISTICS

- f_{max}** **Maximum clock frequency**
 The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause a change of output state with each clock pulse.
- t_{HZ}** **Output disable time (of a three-state output) from high level**
 The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.
- t_{LZ}** **Output disable time (of a three-state output) from low level**
 The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.
- t_{PLH}** **Propagation delay time, low-to-high-level output**
 The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.
- t_{PHL}** **Propagation delay time, high-to-low-level output**
 The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.
- t_{TLH}** **Transition time, low-to-high-level output**
 The time between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from the defined low level to the defined high level.
- t_{THL}** **Transition time, high-to-low-level output**
 The time between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from the defined high level to the defined low level.
- t_w** **Average pulse width**
 The time between 50% amplitude points (or other specified reference points) on the leading and trailing edges of a pulse.

*Current flowing out of a terminal is a negative value.

- t_h** **Hold time**
The time interval for which a signal or pulse is retained at a specified input terminal after an active transition occurs at another specified input terminal.
- t_{release}** **Release time**
The time interval between the release from a specified input terminal of data intended to be recognized and the occurrence of an active transition at another specified input terminal.

Note: When specified, the interval designated "release time" falls within the setup interval and constitutes, in effect, a negative hold time.
- t_{su}** **Setup time**
The time interval for which a signal is applied and maintained at a specified input terminal before an active transition occurs at another specified input terminal.
- t_{ZH}** **Output enable time (of a three-state output) to high level**
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.
- t_{ZL}** **Output enable time (of a three-state output) to low level**
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

CLASSIFICATION OF CIRCUIT COMPLEXITY

Gate equivalent circuit

A basic unit-of-measure of relative digital-circuit complexity. The number of gate equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

LSI **Large-scale integration**

A concept whereby a complete major subsystem or system function is fabricated as a single microcircuit. In this context a major subsystem or system, whether logical or linear, is considered to be one that contains 100 or more equivalent gates or circuitry of similar complexity.

MSI **Medium-scale integration**

A concept whereby a complete subsystem or system function is fabricated as a single microcircuit. The subsystem or system is smaller than for LSI, but whether digital or linear, is considered to be one that contains 12 or more equivalent gates or circuitry of similar complexity.

SSI **Small-scale integration**

Integrated circuits of less complexity than medium-scale integration (MSI).

*Current flowing out of a terminal is a negative value.

Error Detection and Correction

**Using SN54/74ALS632A,
SN54/74ALS633 through SN54/74ALS635**

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INTRODUCTION

NEED FOR ERROR CORRECTION

With memory systems continuing to expand and the expectation of 256K DRAMs in the near future, it has become increasingly important that system designers consider error detection and correction. Generally, the larger the chip density, the greater the probability for device errors. It is easy to recognize this probability when one considers that a 32-bit X 64K memory, using 64K DRAMs, equates to approximately 2.1 million bits of information. This expands to 8.4 million bits of information when using 256K DRAMs. For memory sizes larger than 1/2 million bits, it is generally considered that error detection and correction is required to guarantee high reliability.

The SN54/74ALS632A, SN54/74ALS633 through SN54/74ALS635 provide a simple solution to these requirements in 32-bit machines. In addition, the 'ALS632A and ALS633 provide the necessary hardware to perform byte-write operations which are typically used in the more advanced systems. To ensure the integrity of the error detection and correction circuit itself, diagnostic capabilities have been provided in all four devices.

The 'ALS632A series devices are not limited to only 32-bit systems. They can easily be implemented in 16- or 24-bit systems. In the case of 16-bit systems, the additional memory needed for holding the check bits can be reduced when compared to conventional 16-bit EDAC's.

The pin function table and mechanical data for the 'ALS632A, ALS633 through 'ALS635 are shown respectively as Table 1 and Figure 1.

OPERATIONAL DESCRIPTION

WRITE MODE

During a memory write cycle, the EDAC is required to generate a 7-bit check word to accompany the 32-bit data word before being written into memory. To place the 'ALS632A, 'ALS633 through 'ALS635 in the write mode, simply take S1 and S0 low. Output enable controls $\overline{OE}B0$ through $\overline{OE}B3$ for the 'ALS632A, 'ALS633, or $\overline{OE}DB$ for the 'ALS634, 'ALS635, must be taken high before the data word can be applied. Output enable control $\overline{OE}CS$ must be taken low to pass the check word to the external bus.

The check word will be generated in not more than 48 ns* after the data word has been applied. The 'ALS632A series EDACs can be made to appear transparent to memory, during the write mode, because typical write times of most DRAMs are much larger than the propagation delay of data to check word.

READ-FLAG-CORRECT OPERATION

During a memory read cycle, the function of the 'ALS632A series EDACs is to compare the 32-bit data word against the 7-bit check word previously stored in memory. It will then flag and correct any single-bit error which may have occurred. Single bit errors will be detected through the \overline{ERR} flag and double bit errors will be detected through the \overline{MERR} flag. Figure 2 shows a typical timing diagram of the read-flag-correct operation.

When S0 is taken high, the EDAC will internally begin the correction process, although it should be noted that the error flags are enabled while in the read mode. For many applications, the simplest operation can be obtained by always executing the correction cycle, regardless if a single-bit error has occurred.

IMPORTANT TIMING CONSIDERATIONS FOR READ-FLAG-CORRECT MODE

The most frequently asked question for an EDAC is how fast can a correction cycle be executed. Before S0 can be taken high, the data and check word must be set up at least 10 ns*. In addition, the data and check word must be held for at least 15 ns* after S0 goes high. This ensures the data and check word is saved in the EDAC's input latches. After the hold time has been satisfied, the source which is driving the data bus can be placed in high impedance and the EDAC's output drivers can be enabled. This is accomplished by taking $\overline{OE}B0$ through $\overline{OE}B3$ ('ALS632A, 'ALS633) or $\overline{OE}DB$ ('ALS634, 'ALS635) low.

If the minimum data set up time is used as a reference, and the output drivers are enabled after the minimum data hold time, then correction will be accomplished in not more than 58 ns*.

READ MODIFY-WRITE OPERATIONS

The 'ALS632A and 'ALS633 contain the necessary hardware to perform byte-write operations. The 'ALS634 and 'ALS635 are not capable of byte-write operations because they do not contain an output data latch or individual byte controls. When performing a read-modify-write function, typically the user would first want to perform the read-flag-correct cycle as discussed before, and shown in Figure 2. This ensures that corrected data is used at the start of the modify-write operation.

The corrected data is then latched into the output data latch by taking $\overline{LE}DB0$ from low to high. Upon completing this, modifying any byte or bytes is easily accomplished by taking the appropriate byte control $\overline{OE}B0$ through $\overline{OE}B3$ high. This allows the user to place the modified byte or bytes back onto the data bus while retaining the other byte or bytes. An example of a read-

*These times are based on SN74ALS632A data.

ceramic packages – side-braze (JD suffix)

This is a hermetically sealed ceramic package with a metal cap and side-brazed tin-plated leads.

'ALS632A, ALS633 . . . JD PACKAGE

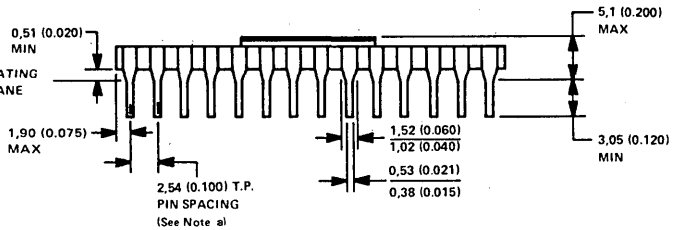
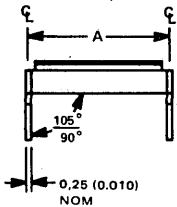
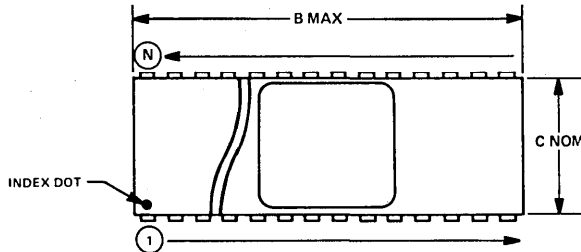
(TOP VIEW)

LEDB0	1	52	VCC
MERR	2	51	S1
ERR	3	50	S0
DB0	4	49	DB31
DB1	5	48	DB30
DB2	6	47	DB29
DB3	7	46	DB28
DB4	8	45	DB27
DB5	9	44	DB26
OEB0	10	43	OEB3
DB6	11	42	DB25
DB7	12	41	DB24
GND	13	40	GND
DB8	14	39	DB23
DB9	15	38	DB22
OEB1	16	37	OEB2
DB10	17	36	DB21
DB11	18	35	DB20
DB12	19	34	DB19
DB13	20	33	DB18
DB14	21	32	DB17
DB15	22	31	DB16
CB6	23	30	CB0
CB5	24	29	CB1
CB4	25	28	CB2
OECB	26	27	CB3

'ALS634, 'ALS635 . . . JD PACKAGE

(TOP VIEW)

MERR	1	48	VCC
ERR	2	47	S1
DB0	3	46	S0
DB1	4	45	DB31
DB2	5	44	DB30
DB3	6	43	DB29
DB4	7	42	DB28
DB5	8	41	DB27
OEB8	9	40	DB26
DB6	10	39	DB25
DB7	11	38	DB24
GND	12	37	GND
DB8	13	36	DB23
DB9	14	35	DB22
DB10	15	34	DB21
DB11	16	33	DB20
DB12	17	32	DB19
DB13	18	31	DB18
DB14	19	30	DB17
DB15	20	29	DB16
CB6	21	28	CB0
CB5	22	27	CB1
CB4	23	26	CB2
OECB	24	25	CB3



DIM	PINS	
	48	52
A ± 0,25 (0.010)	15,24 (0.600)	15,24 (0.600)
B MAX	62,2 (2.45)	67,3 (2.65)
C NOM	15,0 (0.590)	15,0 (0.590)

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

Figure 1. Mechanical Data for 'ALS632A, 'ALS633 through 'ALS635

Table I. Pin Function for 'ALS632A, 'ALS633 through 'ALS635

PIN NAME	DESCRIPTION
S1, S0	Selects the operating mode of the EDAC
	S1 S0 MODE OPERATION
	L L WRITE Input dataword and output checkword
	H L READ & FLAG Input dataword and output error flags
	H H CORRECT Latched input data and checkword/output corrected Data and error syndrome code
L H DIAGNOSTIC Input various datawords against latched checkword/output valid error flags	
DB0 through DB31	I/O port for entering or outputting data
$\overline{OE}B0$ through $\overline{OE}B3$ (ALS632A, 'ALS633)	Three state control for the data I/O port. A high allows data to be entered, and low outputs the data. Each pin controls 8 data I/O ports (or one byte). $\overline{OE}B0$ controls DB0 through DB7, $\overline{OE}B1$ controls DB8 through DB15, $\overline{OE}B2$ controls DB16 through DB23, and $\overline{OE}B3$ controls DB24 through DB31.
$\overline{OED}B$ (ALS634, ALS635)	Three state control for the data I/O port. When low allows data to be outputted and a high allows data to be entered.
LEDB0	Controls the dataword output latch. When low, the data output latch is transparent. When high, the latch stores whatever data was setup at its inputs when the last low to high transition occurred on the pin.
CS0 through CS6	I/O Port for entering or outputting the checkword. It is also used to output the syndrome error code during the error correction mode.
$\overline{OEC}S$	Three state control for the checkword I/O port. A high allows data to be entered and a low allows either the checkword or syndrome code (depending on EDAC mode) to be outputted.
\overline{ERR}	Single error output flag, a low indicates at least a single bit error.
\overline{MERR}	Multiple error output flag, when low indicates two or more errors present

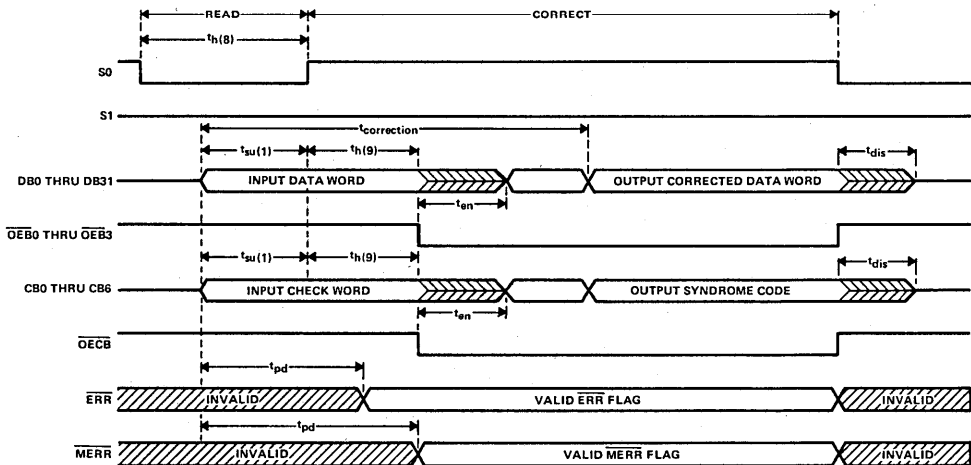


Figure 2. Read-Flag-Correct Timing Diagram

modify-write for byte 0 is shown in Figure 3. Since the check word is no longer valid for the modified data word, a new one is easily generated by taking S0 and S1 low. After the appropriate propagation delay, the new check word will be available.

IMPORTANT TIMING CONSIDERATIONS FOR READ-MODIFY WRITE OPERATIONS

LEDB0 should not be brought from low to high until 45 ns* after S0 goes high. This will ensure that corrected data is latched into the data output latches. On the other hand, LEDB0 should be brought high no later than 0 ns*

before S0 and S1 goes low. Again, this is to ensure that the corrected data is stored into the data output latches. Also of importance is the new check word will be available no later than 48 ns^* after S0 and S1 goes low.

DIAGNOSTIC MODE OPERATION

The purpose of the diagnostic mode is to provide the user with the capability of easily detecting when the EDAC or memory is failing. There are several possibilities as to how a user might employ this feature, but Figure 4 shows a typical timing diagram of some diagnostics which can be performed with these devices. Generally, the user would first place the EDAC in the read mode ($S0 = L, S1 = H$), then apply a valid check word and data word. A valid check word is one in which the user knows what the associated data word. The user would next place the EDAC into the diagnostic mode by taking S0 high, and S1 low. This latches the valid check word into its input latches but leaves the data input latches transparent. To verify that the valid check word was latched properly, OECS can be taken low causing the valid check word to be placed back onto the bus. Since the data input latches remain transparent, this allows the user to apply various diagnostic data words

against the valid check word. A diagnostic data word is one in which either a single or double bit error exists. In either case, the error flags should respond. The output data latch can be verified by taking $\overline{\text{LEDBO}}$ high and confirming the stored diagnostic data word is the same. This is made possible because error correction is disabled while in the diagnostic mode ($S0 = H, S1 = L$). Taking S1 high and $\overline{\text{LEDBO}}$ low will verify that the EDAC will correct the data word. Also, the error syndrome code can be verified by taking $\overline{\text{OECS}}$ low. It should be noted that only the 'ALS632A and 'ALS633 are capable of this pass through verification of the diagnostic data word. The 'ALS634 and 'ALS635 do not have the output data latch required to perform this function.

16-BIT SYSTEMS USING THE ALS632A SERIES EDACs

The 'ALS632A series EDACs can reduce the memory size required in 16-bit systems where conventional 16-bit EDACs (6 check bits, 16 data bits) are presently used. Figure 5 shows the typical system architecture for the 16-bit EDAC. In this system, 88 devices would be required for the 22-bit X 256K memory array, assuming 64K DRAMs are used. It is easy to see that 27.3%, or 24 devices, are

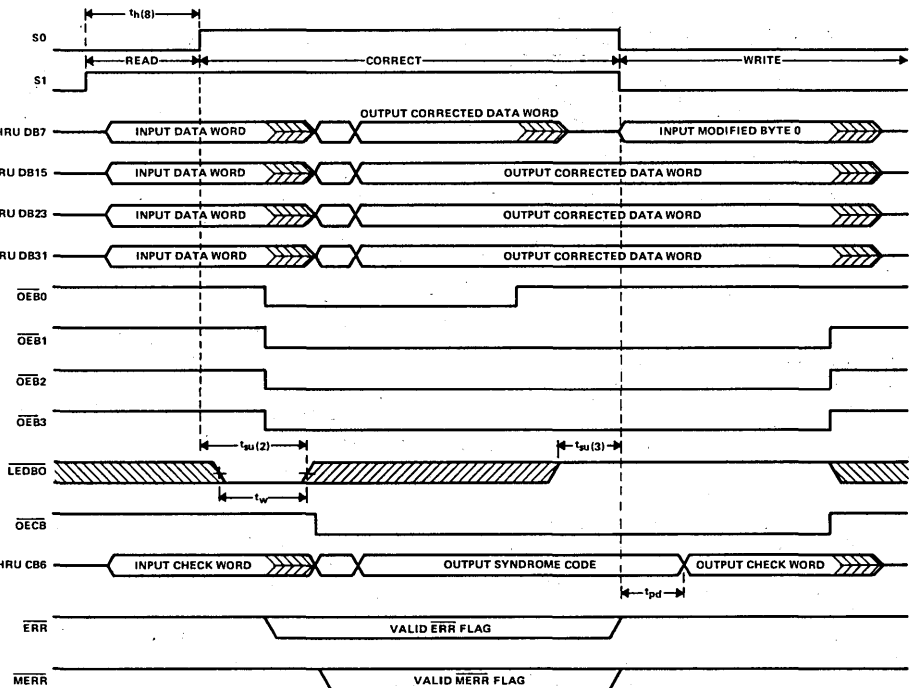


Figure 3. Read-Modify-Write Operation

required for storing the check bits. When using the 'ALS632A series EDACs, the memory required for the check bits can be reduced to 17.9%, or only 14 devices. This reduces the total number of DRAMs required by 10 devices. Figure 6 shows the architecture when using the 32-bit EDAC. The

four 'LS646s are used to group two 16-bit data words into one 32-bit data word. In addition, this type of system can be used in byte-write operations where the other system cannot.

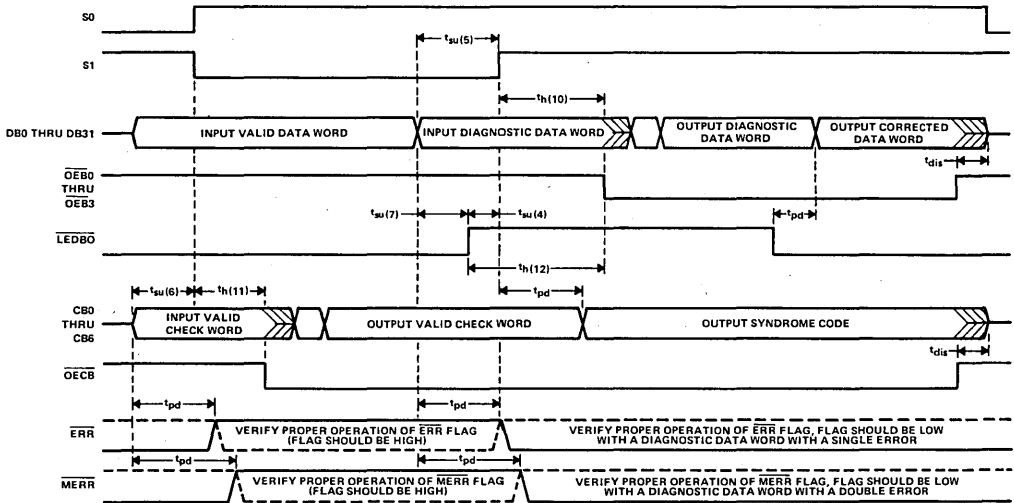


Figure 4. Diagnostic Mode Timing Diagram

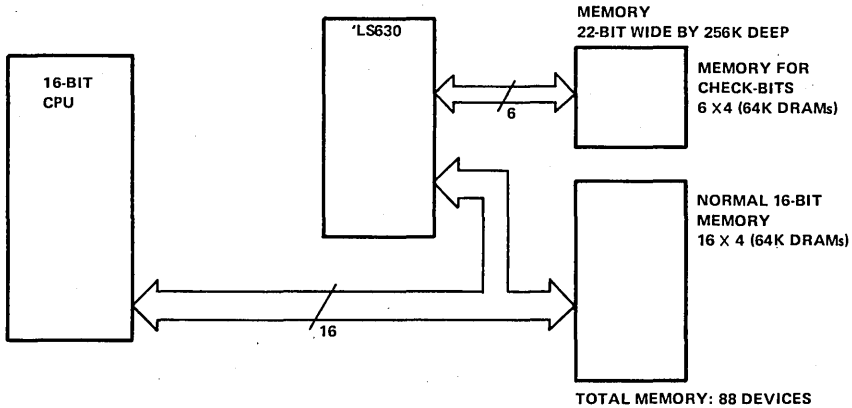


Figure 5. 16-Bit System using Conventional 16-Bit EDAC

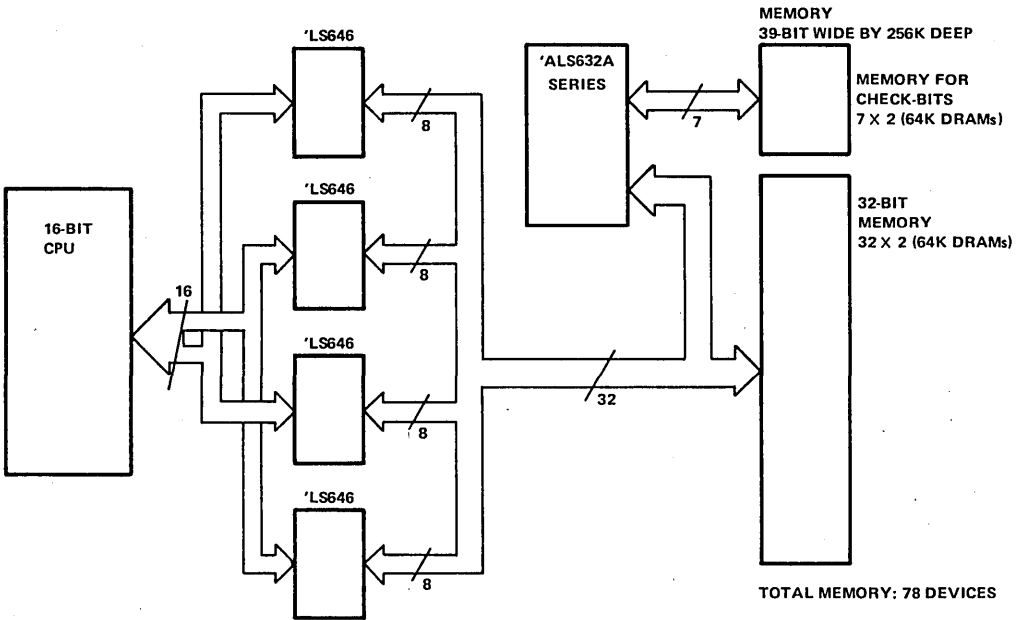


Figure 6. 16-Bit System using 32-Bit EDAC

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MEMORY MAPPING USING SN54/74LS610 THRU SN54/74LS613

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INTRODUCTION

Microprocessors, due to the advent of high density semiconductor memories (i.e., 64K or larger), are being used more and more in systems featuring memory structures larger than 64K bytes. The majority of the microprocessors in use or available today have a 16-bit address bus, with a maximum addressing capability of 64K words. Due to this limitation, some sort of memory mapping is necessary to adapt these microprocessors to applications where large memory structures are required.

The memory mappers (SN54/74LS610 through SN54/74LS613) from TI were designed to alleviate this addressing limitation. These devices employ a paged memory mapping technique in expanding the system memory address bus by 8 bits, thus effectively increasing the system addressing capability by a factor of 2^8 or 256. For microprocessors with a 16-bit address bus (such as the Z-80, the 8085 and the 6800), this results in an increase in the maximum addressing capability from 64K bytes to 16M bytes and for the TMS9900 (which has a 15-bit address bus), the result is an increase from 32K words to 8M words (word = 2 bytes).

In the mapping operation, the four MSBs of the microprocessor address word are used to access one of the sixteen 12-bit registers of the memory mapper's 16×12 -bit RAM array. Each mapper register is capable of holding a 12-bit address which will be termed the page address and will be used as the 12 MSBs of the memory address bus. The remaining 12 bits (11 in the case of the TMS9900) of the microprocessor address bus will be transferred directly to memory from the microprocessor and will be used to address the memory locations within each page. (See Figure 1)

The memory will be organized into 2^x pages (where x equals the number of bits of the page address) with 2^{n-4} words or bytes (where n is the bit length of the microprocessor address bus) per page. Once loaded, the mapper can access only 16 pages or 64K bytes (32K words in the

TMS9900 case). In order to access more pages, the memory mapper RAM array must be reloaded with 16 new page addresses. This is done by the microprocessor via the data bus with the mapper in the WRITE mode. (A more detailed description of the modes of operation will be given later in this report.)

FUNCTIONAL DESCRIPTION

A functional block diagram of the SN54/74LS610 memory mapper, which consists mainly of: a 4-bit 2-to-1 multiplexer, a 16×12 -bit RAM array, a 12-bit 2-to-1 multiplexer, 24 3-state buffers, control logic and in the case of 'LS610 and 'LS611, a 12-bit transparent latch, as shown in Figure 2. Table I lists the functional differences between the 'LS610, 'LS611, 'LS612, and 'LS613. Table II lists the function of each pin.

Depending on the state of the input control signals (i.e., \overline{CS} , R/\overline{W} , \overline{STROBE} , \overline{MM} , and \overline{ME}), the mapper can be operated in three basic modes of operation, I/O (READ or WRITE), MAP and PASS. An explanation of each mode and the control signals necessary to achieve that mode of operation is given below: (Refer to Table III)

Input/Output Mode

In this mode a page address can be loaded either into a mapper register or can be read from a memory mapper register depending on the state of the R/\overline{W} (READ/WRITE) input. This input signal controls either the READ or WRITE function of the I/O Mode.

WRITE Mode

One of the sixteen 12-bit registers is loaded with a page address via the D0-D11 I/O ports from the microprocessor. The address of the selected register is inputted via the RS0-RS3 inputs and is usually the four LSBs of the microprocessor address word. The chip select (\overline{CS}), the strobe (\overline{STROBE}) and R/\overline{W} controls should all be low.

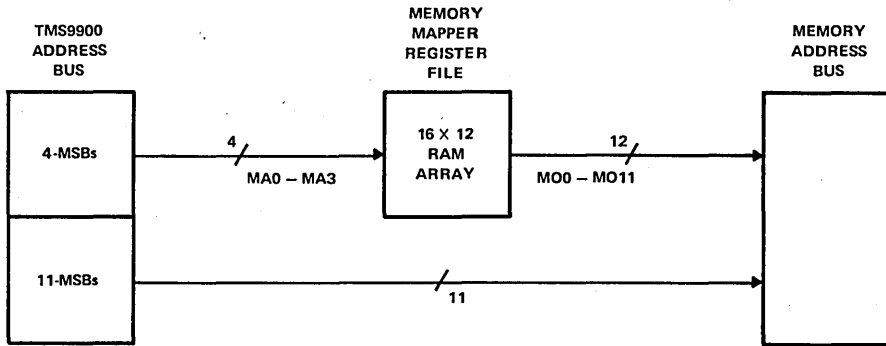


Figure 1. Mapping Operation

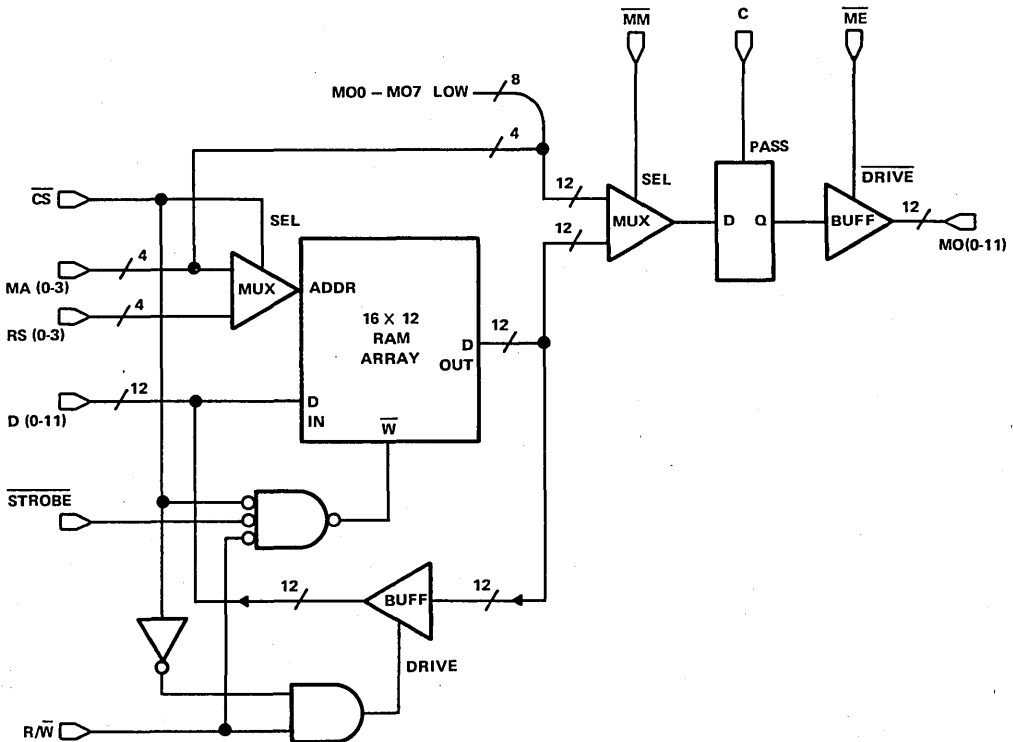


Figure 2. Logic Diagram of the Memory Mapper LS610

Table I. Device Comparison

Device	Map Outputs Latched	Map Output Type
SN54/74LS610	Yes	3-State
SN54/74LS611	Yes	Open-collector
SN54/74LS612	No	3-State
SN54/74LS613	No	Open-collector

READ Mode

The contents of one of the sixteen 12-bit registers is read from the mapper via the D0-D11 I/O ports. As in the WRITE mode, the mapper register is selected by the address on the RS0-RS3 inputs. Again chip select (\overline{CS}) should be low, while the R/W should be kept high.

MAP Mode

The contents of one of the sixteen 12-bit memory mapper registers is outputted to the system address bus via the MO0-MO11 outputs. The address on MA0-MA3 selects the mapper register and is usually the four MSBs of the microprocessor address word. The chip select (\overline{CS}) must be inactive (high), the map mode (\overline{MM}) control and the map enable (\overline{ME}) must both be active (low). The n-4 LSBs, where n equals the microprocessor address bit length, of the microprocessor address bus will be transferred directly to memory from the microprocessor, while the remaining 12 MSBs of the system address bus will be driven onto the bus by the memory mapper.

Table II. Pin Functions

Pin	Pin Name	Functional Description
7-12 29-34	D0 thru D11	I/O connections to data and control bus used for reading from and writing to the map register selected by RS0-RS3 when \overline{CS} is low. Mode controlled by R/W. (D0 corresponds to MO0 and is the most significant bit.)
36, 38, 1, 3	RS0 thru RS3	Register select inputs for I/O operations. (RS3 is the least significant bit.)
6	R/W	Read or write control used in I/O operations to select the condition of the data bus. When high, the data bus outputs are active for reading the map register. When low, the data bus is used to write into the register.
5	\overline{STROBE}	Strobe input used to enter data into the selected map register during I/O operations.
4	\overline{CS}	Chip select input. A low input level selects the memory mapper (assuming more than one used) for an I/O operation.
35, 37, 39, 2	MA0 thru MA3	Map address inputs to select one of 16 map registers when in map mode (\overline{MM} low and \overline{CS} high). (MA3 is the least significant bit.)
14-19 22-27	MO0 thru MO11	Map outputs. Present the map register contents to the system memory address bus in the map mode. In the pass mode, these outputs provide the map address data on MO8-MO11 and low levels on MO0-MO7. (MO11 is the least significant bit.)
13	\overline{MM}	Map mode input. When low, 12 bits of data are transferred from the selected map register to the map outputs. When high (pass mode), the four bits present on the map address inputs are passed to the map outputs.
21	\overline{ME}	Map enable for the map outputs. A low level allows the outputs to be active while a high input level puts the outputs at high impedance.
28	C	Latch enable input for the 'LS610 and 'LS611 (no internal connection for 'LS612 and 'LS613). A high level will transparently pass data to the map outputs. A low level will latch the outputs.
40, 20	V _{CC} , GND	Power supply (5 V) and network ground (substrate) pins.

Table III. Modes of Operation

MAPPER INPUTS	I/O		MAP	PASS
	WRITE (LOAD)	READ (VERIFY)		
\overline{CS}	Active (Low)	Active (Low)	Inactive (High)	Inactive (High)
\overline{STROBE}	Active (Low)	Don't Care	Don't Care	Don't Care
R/\overline{W}	Low	High	Don't Care	Don't Care
\overline{MM}	Don't Care	Don't Care	Active (Low)	Inactive (High)
\overline{ME}	Inactive (High)	Inactive (High)	Active	Active
RS0-RS3	Address of Selected Register	Address of Selected Register	Don't Care	Don't Care
MA0-MA3	Don't Care	Don't Care	Address of Selected Register	Address of Selected Register
MO0-MO11	High Impedance	High Impedance	Valid Address	Valid Address
DO-D11	Register contents to be loaded (input)	Register contents to be read (output)	Input Mode	Input Mode

PASS Mode

The four LSBs (MO8-MO11) of the memory mapper address bus (MO0-MO11) will be the same as the address on the MA0-MA3 input bus, while the remaining eight MSBs of the memory mapper address bus will all be low. The chip select (\overline{CS}) and the map mode (\overline{MM}) should both be inactive (high); map enable (\overline{ME}) should be active. In other words, the address on the system address bus will be the same as the address outputted by the microprocessor, and the memory mapper becomes transparent to the system.

SYSTEMS INTEGRATION

The flexibility of the memory mapper is such that it can be used with microprocessors that have either an 8-bit or a 16-bit data bus. In order to use the memory mapper to its fullest potential (i.e., expand the address bus by eight bits) with an 8-bit microprocessor, the 12-bit page address must be multiplexed into the mapper via the 8-bit data bus. This means that the time it normally takes to load or read the memory mapper will be at least doubled and extra external circuitry will be necessary. If the requirement of the system is such that the address bus needs to be increased by only four bits, then there is no need for multiplexing in the page address. Of course this means that the address bus is expanded to only 20 bits resulting in a 1-megabyte addressing capability. Next in this report, we will look at two 8-bit systems utilizing the 'LS612 memory mapper.

TMS9995-Based System

Figure 3 shows a TMS9995-based system using the 'LS612 to expand the address bus by four bits. The TMS9995 is an 8-bit microprocessor with a 16-bit address bus. This system employs the Programmable System Interface (TMS9901) to control the operation of the mapper. The control of the mapper is software programmable via

the I/O ports of the TMS9901. Since the mapper registers are viewed as part of the logical memory space, an address decode (ADO) of the 12 MSBs is gated with a CRU bit to select the mapper for a READ or WRITE operation. The specific mapper register is then selected by the four LSBs of the microprocessor address bus (A15-A12) via the RS0-RS3 inputs of the mapper. Table IV shows the state of the three control signals P0, P1 and ADO and the corresponding mode of operation of the mapper. When placed in the I/O mode, the READ or WRITE operation is then controlled by memory signals from the microprocessor (i.e., $\overline{WE}/\overline{CRUCLK}$, \overline{MEMEN} , and $\overline{DB IN}$). On POWER-UP and RESET, the I/O ports of the '9901 are put into the input mode. The pull-up resistors R1 and R2 will ensure the mapper is placed in the pass mode during POWER-UP and RESET. The resultant address bus is 20 bits wide, and SA19 is the LSB.

Z-80-Based System

Figure 4 shows another 8-bit (Z-80-based) system using the TI memory mapper. In this case, the control of the mapper is implemented by two flip-flops feeding \overline{MM} and \overline{CS} . These flip-flops are programmed by the Z-80 and are addressed by the data bus, DO-D1. Table V shows the necessary states of DO and D1 to set the mapper in its proper mode of operation. Again during POWER-UP or RESET, the flip-flops are both cleared by RST, which is supplied by the system and which puts the mapper in the pass mode.

Table IV. TMS9900/'LS610 Control Signals

MEMORY MAPPER MODE OF OPERATION	CONTROL SIGNALS		
	P1	P0	ADO
MAP	L	H	L
PASS	H	H	L
I/O	H	L	L

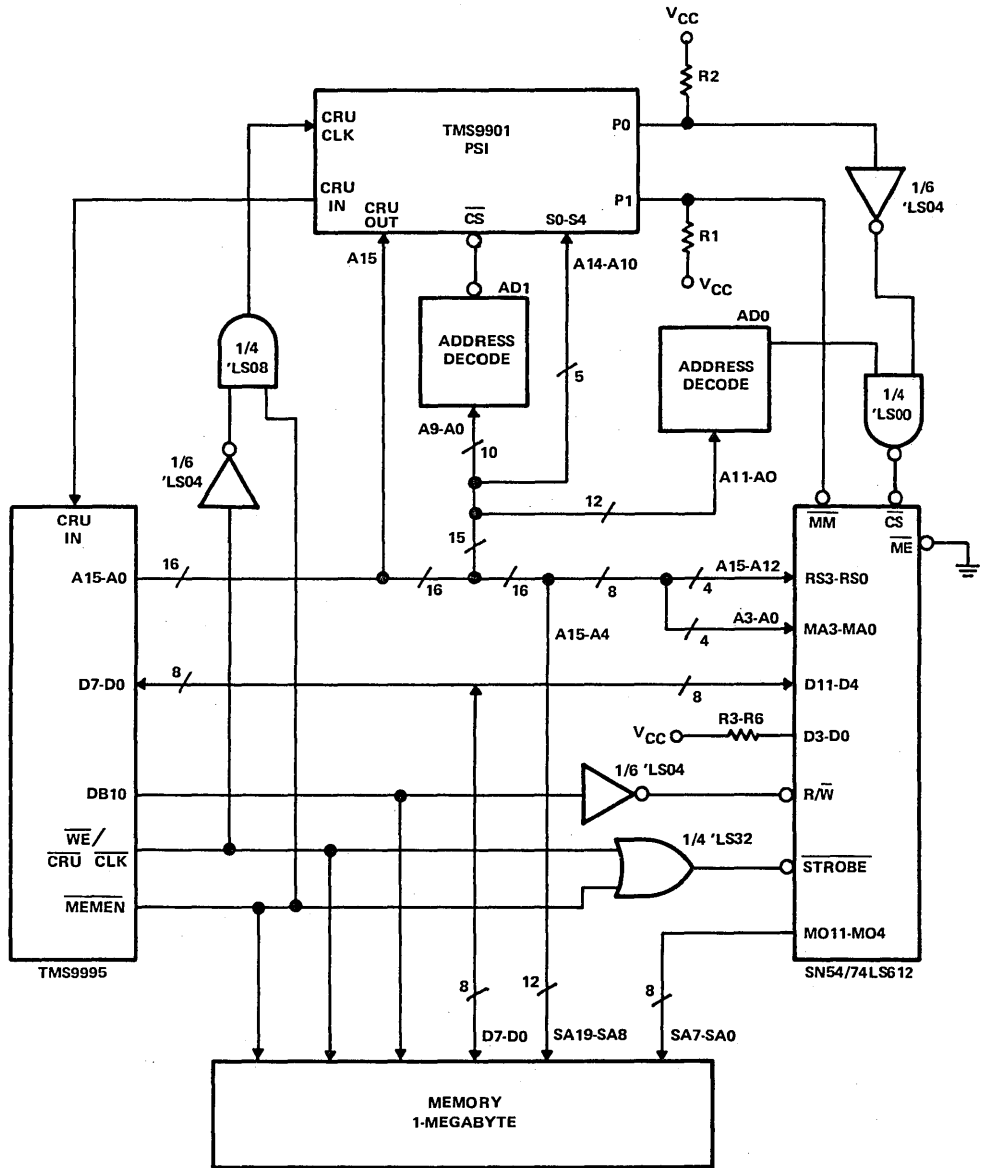


Figure 3. TMS9995 with Memory Mapper



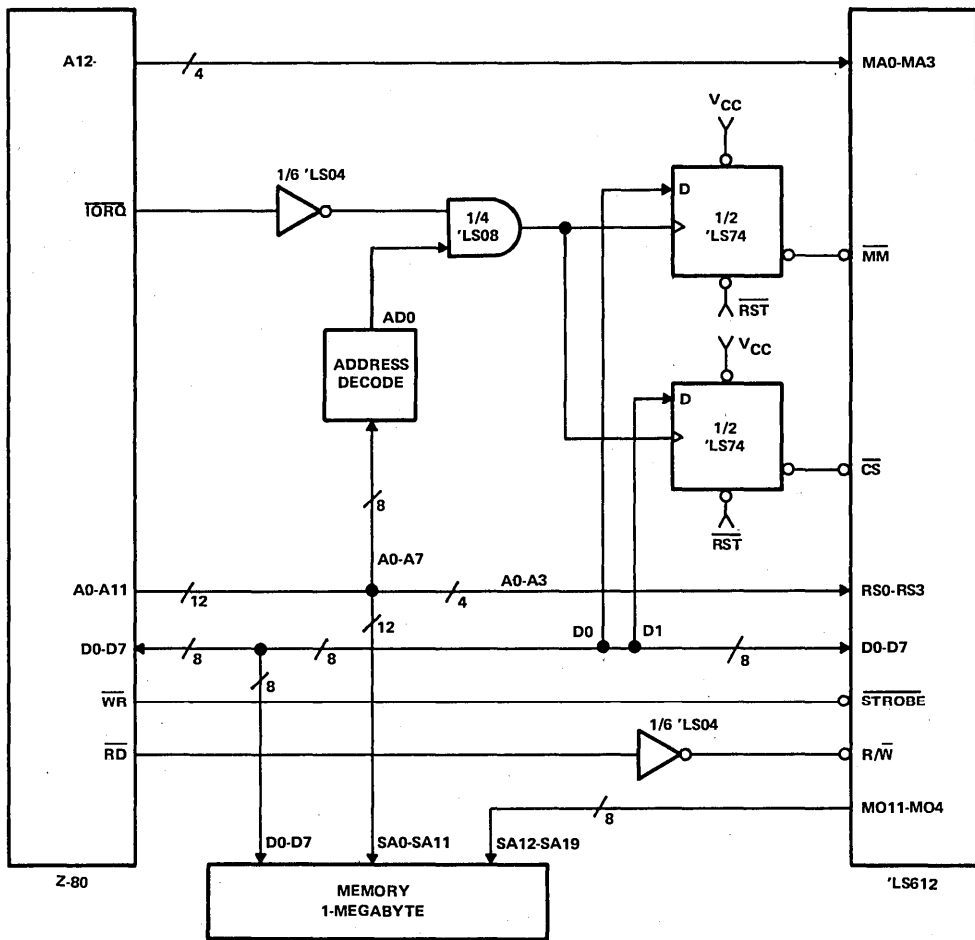


Figure 4. Z-80 with Memory Mapper

Table V. Z-80/LS'610 Control Signals

CONTROL SIGNALS			MEMORY MAPPER
D0	D1	(AD0) $\overline{\text{IORQ}}$	MODE OF OPERATION
L	L	↑	PASS
H	L	↑	MAP
L	H	↑	I/O

TMS9900-Based System

One of the limitations of using an 8-bit microprocessor with the memory mapper, without multiplexing the page address, is that the address bus can only be expanded four bits. In a 16-bit system, one based on a 16-bit microprocessor like the TMS9900, no extra circuitry is necessary to load the mapper with the full 12-bit address. Figure 5

shows a TMS9900 with an SN54/74LS612 for memory mapping. The control of the mapper is implemented in the same fashion as the system using the TMS9995 mentioned previously in the report. The resultant addressing capability is eight megawords. These TI microprocessors have set aside address space for RESET, XOP and INTERRUPT VECTORS, which are addressed when the microprocessor performs a context switch. During a context switch, the microprocessor must be able to address these locations which are part of the logical address (i.e., locations that are capable of being addressed by the microprocessor independently). One method, besides placing the mapper into the pass mode, is to load the memory mapper register whose 4-bit address is O_H with the address of the first page of physical memory. This, like the pass mode, will effectively make the memory mapper appear to be transparent.

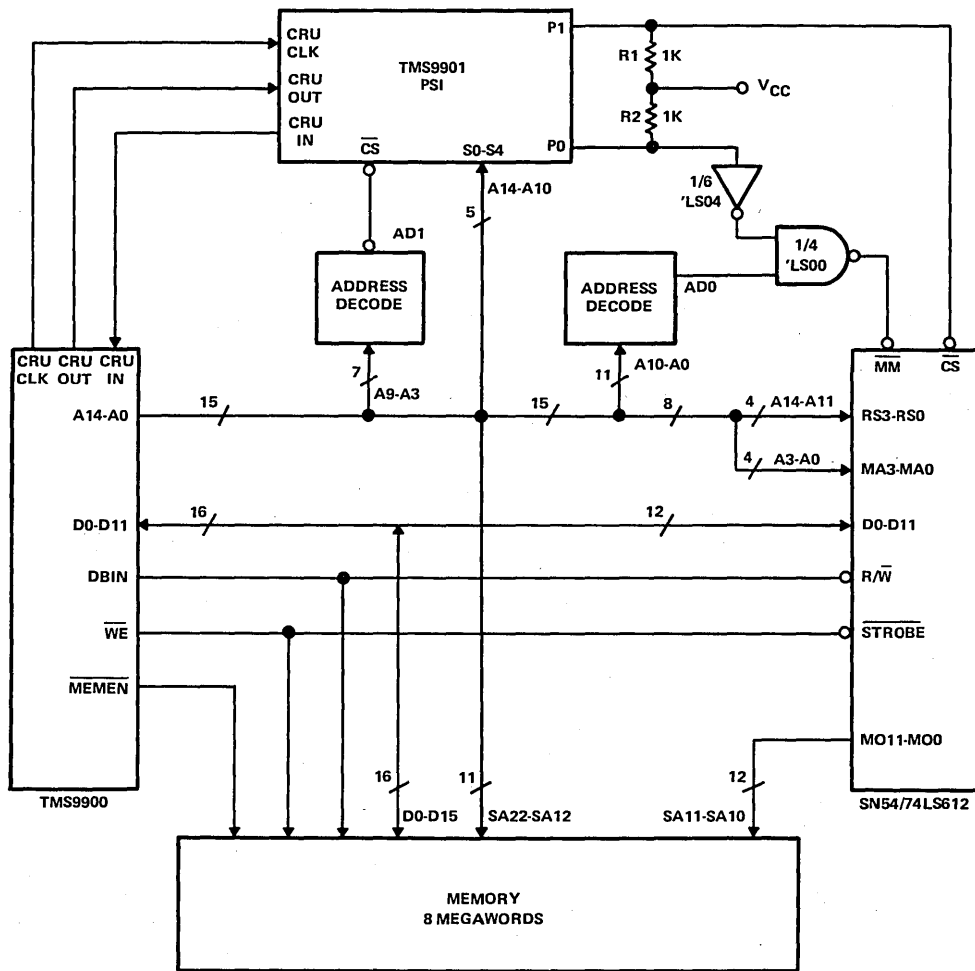


Figure 5. TMS9900 with Memory Mapper

Another point worth noting is that in all three of the previously mentioned systems, the \overline{ME} input was always connected to ground. This caused the mapper address buffers to be enabled during all modes of operation of the mapper. This is only a problem during the I/O mode where, when loading the mapper register, other memory locations are also being written into. The method used to avoid destroying data already in memory was to put the mapper into the pass mode during the I/O operation. This was accomplished simply by pulling MM input high, thus making the system address equal to the microprocessor address.

Multimapper Systems

In a system employing a single memory mapper, the maximum active addressing capability is only 16 pages, if increased addressing capabilities are needed, the mapper must be reloaded. To avoid this procedure, another mapper may be added to the system. This will not increase the overall addressing capability of the system, but it will double the amount of active pages and will also afford twice the active addressing capability. Even though the control of two mappers is a little more detailed than the control of one, the same basic methods employed in the systems with one mapper can be used here.

TIMING

The subject of how the mapper affects the critical timing parameters of the memory READ/WRITE cycles and what changes, if any, are needed to accommodate the mapper, have not been discussed in this report. First, looking at the I/O mode of operation where the mapper registers are either loaded or read from, it is seen that the mapper registers can be regarded as standard common I/O, static RAMs, with maximum access times (RS to valid MO, $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, $V_{CC} = 5\text{ V}$) of 75 ns. Once the I/O mode is set ($\overline{CS} = \text{low}$), the only two signals necessary to read or write into the mapper are \overline{STROBE} and R/\overline{W} . As shown in the previously mentioned system, these signals were supplied directly from the microprocessor with no wait states necessary to perform either function. This will be the case with most microprocessors.

In the MAP and PASS mode, the main concern is the maximum access time (MA to MO). This access time is specified at a maximum of 70 ns, which, depending on the timing of the microprocessor and the memory used, may or may not cause any problems. In the Z-80-based system, no wait states were introduced by the mapper because the memory control signals become active 95 ns after the microprocessor address bus became valid. This gives the address bus sufficient time to settle down.

In conclusion, it can be said that for most microprocessors and memory available at the time of this writing, the operation of the mapper does not adversely affect the memory cycle timing and is flexible enough to be used with almost all microprocessors.

SUMMARY

The possible uses of the memory mapper and the various techniques that can be employed to control its operation are numerous and only some examples were shown in this report. Some of the other possible applications of the mapper include: (1) achieving system addressing capability greater than 16 megabytes is accomplished by reducing the number of mapper registers used by a factor of 2, thus increasing the size of each page by the same factor of 2 without affecting the total amount of pages; (2) being used in systems employing DMA; (3) memory protection which can be accomplished by sacrificing one or two bits of the page address, and gating these bits with the memory control signals.

Another technique that may be employed in controlling the modes of operation of the mapper is to use PROMs.

Bit-Slice Processor Applications

8-Bit Family

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214/995-4720



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Contents

	<i>Page</i>
Title	
Section 1	
Introduction	
INTRODUCTION	3-73
Section 2	
2910 Microprogram Controller Emulation Using the 'AS890 Microsequencer	
2910 MICROPROGRAM CONTROLLER EMULATION USING THE 'AS890 MICROSEQUENCER	3-75
Emulator Configuration	3-75
Microinstruction Conversion	3-75
2910 Emulation Differences	3-75
Loop Counts	3-75
Register Loading	3-76
Stack Full Indication	3-76
Data Path Widths	3-76
Section 3	
Minimum Cycle Time Delay Calculations for a 16-Bit System	
MINIMUM CYCLE TIME DELAY CALCULATIONS FOR A 16-BIT SYSTEM	3-93
16-Bit Computer System Design	3-93
Benchmark I: Comparison of Am2903A/2910A with 'AS888-1/'AS890-1	3-94
Benchmark II: Comparison of Am2901C/2910A with 'AS888-1/'AS890-1	3-94
Summary of Results	3-94
Section 4	
32-Bit CPU Design with the 'AS888/'AS890	
32-BIT CPU DESIGN WITH THE 'AS888/'AS890	3-101
Designing a 32-Bit System	3-101
Construction of the ALU	3-101
Construction of the CCU	3-103
Tracing Through a 32-Bit Computer	3-104
Defining the Macrocode Instruction Format	3-107
Tracing a Macrocode Instruction	3-107
System Enhancements	3-109
Timing and System Throughput	3-111
Fetch Analysis	3-111
Multiplication Analysis	3-111
Section 5	
An Adaptive Clock Generator to Increase 'AS888 System Speed	
AN ADAPTIVE CLOCK GENERATOR TO INCREASE 'AS888 SYSTEM SPEED	3-113
Circuit Description	3-113
PROM Program	3-113

Section 6 Floating-Point System Design Using the 'AS888/'AS890

FLOATING-POINT SYSTEM DESIGN USING THE 'AS888/'AS890	3-125
Step 1: Choose a Floating-Point Number System	3-125
Step 2: Choose an Algorithm for Sin(x)	3-126
Step 3: Make 'AS888 Register Assignments	3-126
Step 4: Substitute Registers for Variables in the Algorithm	3-127
Step 5: Decompose Steps in the Algorithm into Simple Operations	3-127
Step 6: Translate into 'AS888/890 Instructions; Identify Subroutines	3-128
Step 7: Expand Subroutines into 'AS888/890 Operations	3-129
Floating-Point Multiplication	3-129
Floating-Point Addition	3-131
Step 8: Evaluate Trade-Offs and Block Diagram the Hardware	3-133
Step 9: Define Microinstruction Fields During Detailed Hardware Design	3-134
Step 10: Assemble the Microprogram	3-134

List of Illustrations

<i>Figure</i>	<i>Title</i>	<i>Page</i>
2-1	2910 Emulator Block Diagram	3-76
3-1	16-Bit Computer System	3-93
3-2	Am2903-Based 16-Bit Computer System	3-97
3-3	'AS888-Based 16-Bit Computer System	3-98
3-4	ALU Path for Multiplication and Division in the Am2903A System	3-98
3-5	ALU Path for Multiplication and Division in the 'AS888 System	3-99
3-6	Am2901C-Based 16-Bit Computer System	3-99
3-7	Modified Design of Am2901C-Based System	3-100
4-1	System Design Approach	3-101
4-2	CCU Block Diagram	3-102
4-3	ALU Block Diagram	3-102
4-4	Cascaded 'AS888 Packages	3-103
5-1	Adaptive Clock Generator Circuit	3-114
5-2	Adaptive Clock Generator Timing Diagram	3-115
5-3	Propagation Delay Without Carry and Without Shift	3-118
5-4	Propagation Delay Without Carry and With Shift	3-119
5-5	Propagation Delay With Carry and Without Shift	3-120
5-6	Propagation Delay With Carry and With Shift	3-121
5-7	PROM Data	3-124
6-1	Block Diagram of Floating-Point Processor	3-134

List of Programs

<i>Program</i>	<i>Title</i>	<i>Page</i>
2-1	Logic Equations Used to Generate Emulator PAL 1	3-78
2-2	Expanded Product Terms, Symbol Table and Fuse Plot for Emulator PAL 1	3-79
2-3	Simulation Results for Emulator PAL 1	3-82
2-4	JEDEC Printout for Emulator PAL 1	3-83
2-5	Logic Equations Used to Generate Emulator PAL 2	3-84
2-6	Expanded Product Terms, Symbol Table and Fuse Plot for Emulator PAL 2	3-85
2-7	Simulation Results for Emulator PAL 2	3-88
2-8	JEDEC Printout for Emulator PAL 2	3-91
5-1	BASIC Program to Generate PROM Data	3-122

List of Tables

<i>Table</i>	<i>Title</i>	<i>Page</i>
2-1	Typical Switching Characteristics	3-75
2-2	'AS890 Encodings for Am2910 Instructions	3-77
2-3	Effect of Table 2-2 Encodings on 'AS890 Control Signals	3-77
3-1	Am2903A/Am2910A Timings for Addition	3-94
3-2	'AS888-1/'AS890-1 Timings for Addition	3-94
3-3	Am2903A/Am2910A Timings for Addition with Shift	3-95
3-4	'AS888-1/'AS890-1 Timings for Addition with Shift	3-95
3-5	Am2903A/Am2910A Timings for Multiplication	3-95
3-6	Am2903A/Am2910A Timings for Division	3-95
3-7	'AS888-1/'AS890-1 Timings for Multiplication and Division	3-96
3-8	Am2901C/Am2910A Timings for Addition	3-96
3-9	Am2901C/Am2910A Timings for Addition with Shift	3-96
3-10	Summary of Results	3-96
4-1	Microcode Definition	3-105
4-2	Functional Listing of Fetch	3-106
4-3	Assembler Listing of Fetch	3-106
4-4	Microcode Listing of Fetch	3-107
4-5	Possible Instruction Formats	3-107
4-6	Functional Listing of Multiply	3-107
4-7	Assembler Code of Multiply	3-108
4-8	Microcode Listing of Multiply	3-109
4-9	Critical Delay Path Analysis	3-110
4-10	Fetch Timing Comparison	3-110
4-11	Multiply Timing Comparison	3-110
5-1	'AS888-1 Timing Characteristics	3-115
5-2	Shift and Carry as a Function of I7-I0	3-116
5-7	PROM Data	3-123
6-1	Floating Point Sin(x) Microprogram	3-135



Section 1

Introduction

Bit-slice technology has gained widespread acceptance among CPU designers over the past several years as a means of increasing system speed and reducing the discrete logic needed for CPU construction. TI's recent entries on the market, the SN74AS888 8-bit processor slice and its companion microsequencer, the SN74AS890, increase processing throughput per unit area to an extent never before realized in bit-slice systems, making them well suited to the construction of high-speed systems with flexible instruction sets.

This is the first in a series of application books addressed to users of TI's bit-slice products. It discusses ways to take advantage of the 'AS888/'AS890's increased speed in the areas of CPU design and floating point processing, compares their performance with similar products, and presents a means of achieving optimum speed by adding an adaptive clock circuit to an 'AS888/'AS890 system. Also included is a 2910 emulator, which allows users to take advantage of the 'AS890's increased speed and greatly expanded addressing range, while still retaining existing 2910 software. Brief abstracts of the papers in this volume are given below.

Section 2, "2910 Microprogram Controller Emulation using the 'AS890 Microsequencer," converts the 16 instructions of the 2910 into 'AS890 commands, using programmable array logic (PALs) for fast emulation. By using the emulator, accessible microcode store can be quadrupled from 4,096 to 16,384 memory locations, and advantage can be taken of the 'AS890's deeper stack.

Section 3, "Minimum Cycle Time Delay Calculations for a 16-Bit System," examines some timings for systems using TI's 'AS888-1/'AS890-1, AMD's Am2901C/2910A,

and AMD's Am2903A/2910A. Four cases are considered: addition, addition followed by a shift of the result, unsigned integer multiplication and unsigned integer division.

Section 4, "32-Bit CPU Design with the 'AS888/'AS890," takes a look at constructing a central processing unit by cascading four 'AS888s to form a 32-bit ALU and the 'AS890 sequencer to address a control store containing the system microcode. Microcode and assembly code are given for an instruction fetch routine and for unsigned multiplications.

Section 5, "An Adaptive Clock Generator to Increase 'AS888 System Speed," uses an adaptive circuit to generate clock pulses for an 'AS888-based system. The clock cycle length is optimally matched to the propagation delay of the 'AS888 for each individual instruction, further increasing the speed of the system. The circuit is linked to the 'AS888 with a PROM that decodes 888 instructions into cycle lengths. A BASIC program calculates instruction lengths and generates a file that can be transmitted to a Data I/O PROM programmer.

Section 6, "Floating Point Design using the 'AS888/'AS890," provides a model for floating point system design, illustrating the step by step development of a utility to compute $\sin(x)$. By developing a $\sin(x)$ algorithm, a microprogram is generated and hardware requirements are identified in an interactive manner.

The application notes in this volume were prepared by the following members of VLSI Systems Engineering:

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3

Application Reports

Section 2

2910 Microprogram Controller Emulation using the 'AS890 Microsequencer

The 'AS890 microsequencer, with its powerful instruction set, can be microprogrammed to emulate the popular 2910 microprogram controller. By converting the 16 instructions of the 2910 into the appropriate 'AS890 commands, 2910 users can both quadruple accessible microcode store from 4,096 to 16,384 memory locations and take advantage of the 'AS890's deeper stack, while retaining existing microprograms and preserving prior investments in software without loss of system performance. Programmable Read Only Memory (PROM) can be used to implement the system, or TI's Programmable Array Logic PAL® can be selected for faster emulation.

EMULATOR CONFIGURATION

The DRB inputs of the 'AS890 are used as the 2910 emulator's D (direct data) inputs. JSRP and JRP (2910 instructions 5 and 7) conditionally select the counter/register, requiring the counter/register contents to be available through the Y-output multiplexer. The 'AS890 does not directly support this function, but it can be accomplished by enabling either the DRA or DRB ports as an output and selecting the appropriate path through the Y-multiplexer.

JSRP and JRP also require that direct data input and existing register/counter contents be available at the Y-multiplexer concurrently. The emulator uses direct data port DRA and register/counter A for this purpose. Two '74AS244 buffers are used to isolate DRA from DRB so that register/counter A can be loaded from the Direct Data input and DRA can be used to send the register/counter's contents to the Y-multiplexer.

Figure 2-1 shows the configuration of the 2910 emulator. To provide fast propagation delays, two TIBPAL16L8-15s, with a maximum propagation delay of 15 ns, are used for the control PALs. Because the TIBPAL16L8-15 will only accommodate seven product

terms and eight were required for the condition code input to the 'AS890, it is driven by two outputs of the control PAL. These outputs are selectively enabled using the $\overline{\text{CCEN}}$ input (see Programs 2-1 and 2-5 for detailed PAL equations).

Typical switching delays for the 2910 emulator are summarized in Table 2-1.

MICROINSTRUCTION CONVERSION

Table 2-2 lists Y-multiplexer, stack and register control encodings that can be used to convert the 2910 instruction set into 'AS890 microinstructions. The effect of these encodings on the Y-multiplexer, stack and register controls is shown in Table 2-3. Data from Table 2-2 was used as input to a universal program logic compiler to produce the emulator's two control PALs. Files generated for each PAL by the compiler include:

1. a logic description file
2. a listing of expanded product terms and fuse map
3. simulation results
4. a JEDEC file.

These are reproduced at the end of this application note. The CUPL™ software used to develop the PALs is available from Texas Instruments or from Assisted Technology, Inc., San Jose, CA.

2910 EMULATION DIFFERENCES

The architecture of the 'AS890 does not lend itself to a complete emulation of the 2910 controller. Differences are noted below.

Loop Counts

The 2910 register/counter is tested for a zero value prior to decrementing and branching on conditional loops. The counter is usually loaded with a value that is one less

Table 2-1. Typical Switching Characteristics

SET-UP AND HOLD TIMES			COMBINATIONAL DELAYS			
INPUT	Ts	Th	FROM	TO		
				Y	PL,MAP VECT	FULL
D → R (Inst. = 5,7)	15	0	DO-D13 (Inst. = 5,7)	15		
D → R (Inst. ≠ 5,7)	8	0	DO-D13 (Inst. ≠ 5,7)	8		
D → Pc (Inst. = 5,7)	28	0	I0-I3 (Inst. = 5,7,9)	27	10	
D → Pc (Inst. ≠ 5,7)	20	0	I0-I3 (Inst. ≠ 5,7,9)	22	10	
I3-I0	36	0	CC	22		
CC	36	0	CCEN	22		
CCEN	36	0	CP	18		25
CI	12	0	CP (I = 8,9,F & CNTR = 2)	24		25
RLD	36	0	OE	8		

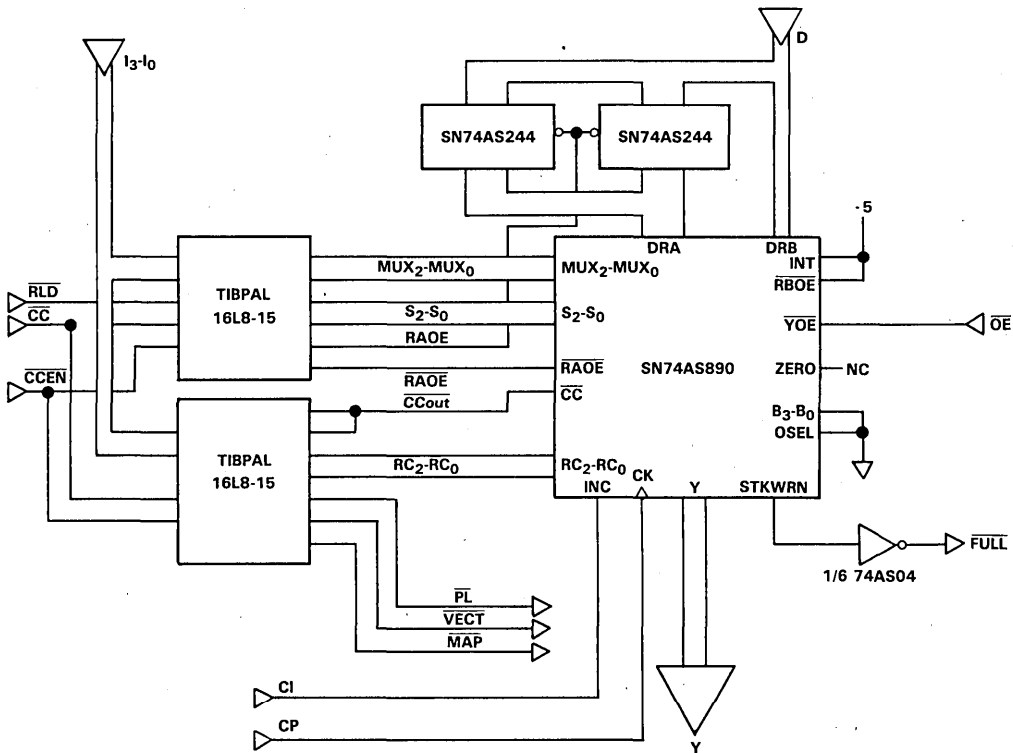


Figure 2-1. 2910 Emulator Block Diagram

than the desired loop count. The 'AS890 tests for a one prior to decrementing. Therefore, the 2910 emulator requires that the actual loop count, rather than loop count minus one, be loaded into the register/counter.

Three of the 2910 instructions (RFCT, RPCT, and TWB) execute once and terminate the counter decrement when a zero is found in the register/counter. The emulator requires a one in the register/counter to execute these instructions and terminate the counter decrement. Loading a zero into the register/counter before decrementing will cause the emulator to loop 16,384 times.

Register Loading

Using the 2910's register load (RLD) input during a JSRP or JRP instruction allows external data to be input to the register/counter while the current value in the register/counter is output on the Y-bus. This is not the case with the 'AS890, where an external value placed on DRA for input to the register/counter will also be sent to the Y-

multiplexer outputs. A register load using the emulator must therefore be implemented independently of the JSRP or JRP instructions.

Stack Full Indication

The 'AS890 stack is nine levels deep, compared to the 2910's five-level stack. The 2910 signals that all five levels of the stack are used by setting FULL low. The emulator's FULL signal is set to zero when its eighth stack location is used, indicating that only one location remains available. A low value will also appear at the FULL output when a stack POP is to be executed and the stack is empty.

Data Path Widths

Because the 'AS890 supports 14-bit data paths instead of the 2910's 12-bit paths, the number of address locations that can be accessed by the emulator can be expanded from 4,096 to 16,634 locations.

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Table 2-2. 'AS890 Encodings for Am2910 Instructions

13-10	MNEMONIC	NAME	$\overline{CCEN} = \text{LOW}$ and $\overline{CC} = \text{HIGH}$				$\overline{CCEN} = \text{HIGH}$ or $\overline{CC} = \text{LOW}$				ENABLE
			CCOUT	RC	S	MUX	CCOUT	RC	S	MUX	
0	JZ	JUMP ZERO	H	LLL	LLL	HHH	H	LLL	LLL	HHH	PL
1	CJS	COND JSB PL	H	LLL	HLH	HHH	L	LLL	HLH	HHH	PL
2	JMAP	JUMP MAP	H	LLL	HHH	HLL	H	LLL	HHH	HLL	MAP
3	CJP	COND JUMP PL	H	LLL	HHH	HHH	L	LLL	HHH	HHH	PL
4	PUSH	PUSH/COND LD CNTR	H	LLL	HHL	HHH	H	LHL	HHL	HHH	PL
5	JSRP	COND JSB R/PL	L	LLL	HHL	HLL	H	LLL	HHL	HLL	PL
6	CJV	COND JUMP VECTOR	H	LLL	HHH	HHH	L	LLL	HHH	HHH	VECT
7	JRP	COND JUMP R/PL	L	LLL	HHH	HLL	H	LLL	HHH	HLL	PL
8	RFCT	RPT LOOP, CNTR ≠ 0	L	LLH	LHL	LLH	L	LLH	LHL	LLH	PL
9	RPCT	RPT LOOP, CNTR ≠ 0	L	LLH	HHH	HLL	L	LLH	HHH	HLL	PL
A	CRTN	COND RTN	H	LLL	LHH	LHH	L	LLL	LHH	LHH	PL
B	CJPP	COND JUMP PL & POP	H	LLL	LHH	HHH	L	LLL	LHH	HHH	PL
C	LDCT	LD CNTR 7 CONTINUE	H	LHL	HHH	HHH	H	LHL	HHH	HHH	PL
D	LOOP	TEST END LOOP	L	LLL	LHL	LHH	H	LLL	LHL	LHH	PL
E	CONT	CONTINUE	H	LLL	HHH	HHH	H	LLL	HHH	HHH	PL
F	TWB	THREE-WAY BRANCH	L	LLH	LHL	LHH	H	LLH	LHL	LHH	PL

Table 2-3. Effect of Table 2-2 Encodings on 'AS890 Control Signals

13-10	MNEMONIC	NAME	ZERO	$\overline{CCEN} = \text{LOW}$ and $\overline{CC} = \text{HIGH}$				$\overline{CCEN} = \text{HIGH}$ or $\overline{CC} = \text{LOW}$				ENABLE
				CCOUT	RC	S	MUX	CCOUT	RC	S	MUX	
0	JZ	JUMP ZERO		H	Hold	Reset	0	H	Hold	Reset	0	PL
1	CJS	COND JSB PL		H	Hold	Hold	MPC	L	Hold	Push	DRB	PL
2	JMAP	JUMP MAP		H	Hold	Hold	DRB	H	Hold	Hold	DRB	MAP
3	CJP	COND JUMP PL		H	Hold	Hold	MPC	L	Hold	Hold	DRB	PL
4	PUSH	PUSH/COND LD CNTR		H	Hold	Push	MPC	H	LoadA	Push	MPC	PL
5	JSRP	COND JSB R/PL		L	Hold	Push	DRA	H	Hold	Push	DRB	PL
6	CJV	COND JUMP VECTOR		H	Hold	Hold	MPC	L	Hold	Hold	DRB	VECT
7	JRP	COND JUMP R/PL		L	Hold	Hold	DRA	H	Hold	Hold	DRB	PL
8	RFCT	RPT LOOP, CNTR ≠ 0	L	L	DecA	Hold	STK	L	DecA	Hold	STK	PL
			H	L	DecA	Pop	MPC	L	DecA	Pop	MPC	PL
9	RPCT	RPT LOOP, CNTR ≠ 0	L	L	DecA	Hold	DRA	L	DecA	Hold	DRA	PL
			H	L	DecA	Hold	MPC	L	DecA	Hold	MPC	PL
A	CRTN	COND RTN		H	Hold	Hold	MPC	L	Hold	Pop	STK	PL
B	CJPP	COND JUMP PL & POP		H	Hold	Hold	MPC	L	Hold	Pop	DRB	PL
C	LDCT	LD CNTR 7 CONTINUE		H	LoadA	Hold	MPC	H	LoadA	Hold	MPC	PL
D	LOOP	TEST END LOOP		L	Hold	Hold	STK	H	Hold	Pop	MPC	PL
E	CONT	CONTINUE		H	Hold	Hold	MPC	H	Hold	Hold	MPC	PL
F	TWB	THREE-WAY BRANCH	L	L	DecA	Hold	STK	H	DecA	Pop	MPC	PL
			H	L	DecA	Pop	DRB	H	Hold	Pop	MPC	PL

Program 2-1. Logic Equations Used to Generate Emulator PAL 1

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SOURCE FILE: B:2910EM DEVICE: P16L8

```

1:
2:          PARTNO    2910EM ;
3:          NAME      '74AS890/2910 EMULATOR PAL 1 ;
4:          DATE      04/04/85 ;
5:          REV        01 ;
6:          DESIGNER  RICHARD D. NAWROCKI ;
7:          COMPANY   TEXAS INSTRUMENTS ;
8:          ASSEMBLY  00001 ;
9:          LOCATION  U100 ;
10:
11: /******
12: /*
13: /* THIS DEVICE GENERATES CONTROL SIGNALS FOR THE '74AS890
14: /* EMULATION OF THE 2910 MICROPROGRAM CONTROLLER.
15: /*
16: /* ALLOWABLE TARGET DEVICE TYPES: PAL16L8A
17: /******
18:
19: /** INPUTS **/
20:
21: PIN [1..4] = [I0..3] ; /* 2910 INSTRUCTION CODE */
22: PIN 5 = RLD ; /* 2910 REGISTER LOAD */
23:
24: /** OUTPUTS **/
25:
26: PIN 19 = RAOE ; /* 74AS890 DRA OUTPUT ENABLE */
27: PIN [18..16] = [MUX0..2] ; /* 74AS890 MUX_Y CONTROL */
28: PIN [15..13] = [S0..2] ; /* 74AS890 STACK CONTROL */
29: PIN 12 = EN_244 ; /* 74AS244 OUTPUT ENABLES */
30:
31: /** DECLARATIONS AND INTERMEDIATE VARIABLE DEFINITIONS **/
32:
33: FIELD INSTRUCTION = [I3..0] ;
34: FIELD STACK = [S2..0] ;
35: FIELD Y_MUX = [MUX2..0] ;
36:
37:
38: /** LOGIC EQUATIONS **/
39:
40: !RAOE = INSTRUCTION:[5,7] & RLD ;
41:
42: !EN_244 = INSTRUCTION:[0..4,6,8..F] # (INSTRUCTION:[5,7] & !RLD) ;
43:
44: STACK = INSTRUCTION:1 & 'H'5
45: # INSTRUCTION:[2,3,6,7,9,C,E] & 'H'7
46: # INSTRUCTION:[4,5] & 'H'6
47: # INSTRUCTION:[8,D,F] & 'H'2
48: # INSTRUCTION:[A,B] & 'H'3 ;
49:
50: Y_MUX = INSTRUCTION:[0,1,3,4,6,B,C,E] & 'H'7
51: # INSTRUCTION:[2,5,7,9] & 'H'4
52: # INSTRUCTION:8 & 'H'1
53: # INSTRUCTION:[A,D,F] & 'H'3 ;
54:
55:
56:

```

JEDEC FUSE CHECKSUM (7103)
 JEDEC TRANSMIT CHECKSUM (259E)

Program 2-2. Expanded Product Terms, Symbol Table and Fuse Plot for Emulator PAL 1

```

CUPL          2.02A
DEVICE        P16L8 DL1B-c-18-5
PARTNO        2910EM
NAME          '74AS890/2910 EMULATOR PAL 1
REVISION      01
DATE          04/04/85
DESIGNER      RICHARD D. NAWROCKI
COMPANY       TEXAS INSTRUMENTS
ASSEMBLY      00001
LOCATION       U100
    
```

=====

EXPANDED PRODUCT TERMS

=====

```

EN_244 ->
  I3
  # !I2 & !I3
  # !I0 & !I2 & !I3
  # I0 & !I2 & !I3 & !RLD
                                RAOE_0E ->
                                    1
                                S0_0E ->
                                    1
INSTRUCTION ->
  I3 , I2 , I1 , I0
                                S1_0E ->
                                    1
MUX0 ->
  I0 & !I2 & !I3
  # !I0 & !I1 & !I2 & !I3
  # I0 & !I1 & !I2 & !I3
                                S2_0E ->
                                    1
MUX1 ->
  I0 & !I2 & !I3
  # !I1 & !I2 & !I3
  # !I0 & !I1 & !I2 & !I3
MUX2 ->
  !I0 & !I2 & !I3
  # I0 & !I2 & !I3
RAOE ->
  I0 & !I2 & !I3 & RLD
S0 ->
  I0 & !I1 & !I2
  # !I0 & !I1 & !I3
  # I0 & !I2 & !I3
  # !I0 & !I1 & !I2
S1 ->
  !I1 & !I2 & !I3
S2 ->
  I1 & !I2 & !I3
  # !I0 & !I1 & !I2
  # I0 & !I2 & !I3
STACK ->
  S2 , S1 , S0
Y_MUX ->
  MUX2 , MUX1 , MUX0
EN_244_0E ->
  1
MUX0_0E ->
  1
MUX1_0E ->
  1
MUX2_0E ->
  1
    
```

Program 2-2. Expanded Product Terms, Symbol Table and Fuse Plot for Emulator PAL 1 (Continued)

SYMBOL TABLE

POL	NAME	EXT	PIN	TYPE	USED	MAX
	EN_244		12	V	4	7
	I0		1	V	-	-
	I1		2	V	-	-
	I2		3	V	-	-
	I3		4	V	-	-
	INSTRUCTION		0	F	-	-
	MUX0		18	V	3	7
	MUX1		17	V	3	7
	MUX2		16	V	2	7
	RAOE		19	V	1	7
	RLD		5	V	-	-
	S0		15	V	4	7
	S1		14	V	1	7
	S2		13	V	3	7
	STACK		0	F	-	-
	Y_MUX		0	F	-	-
	EN_244	OE	12	D	1	1
	MUX0	OE	18	D	1	1
	MUX1	OE	17	D	1	1
	MUX2	OE	16	D	1	1
	RAOE	OE	19	D	1	1
	S0	OE	15	D	1	1
	S1	OE	14	D	1	1
	S2	OE	13	D	1	1

LEGEND D : DEFAULT VAR F : FIELD I : INTERMEDIATE VAR
 U : UNDEFINED V : VAR X : EXTENDED VAR
 N : NODE M : EXTENDED NODE

FUSE PLOT

PIN #19		PIN #17	
0000	-----	0512	-----
0032	--x-x--x-x-----	0544	--x-x--x-----
0064	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0576	-x--x--x-----
0096	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0608	x--x-x--x-----
0128	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0640	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0160	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0672	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0192	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0704	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0224	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0736	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
PIN #18		PIN #16	
0256	-----	0768	-----
0288	--x-x--x-----	0800	--x-x--x-----
0320	x--x-x--x-----	0832	-x--x--x-----
0352	--xx--x--x-----	0864	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0384	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0896	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0416	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0928	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0448	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0960	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0480	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0992	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

Program 2-2. Expanded Product Terms, Symbol Table and Fuse Plot for Emulator PAL 1 (Continued)

```

PIN #15
1024 -----
1056 -xx-x-----
1088 -x-x--x-----
1120 --x-x--x-----
1152 -x-x-x-----
1184 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
1216 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
1248 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
PIN #14
1280 -----
1312 -x--x--x-----
1344 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
1376 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
1408 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
1440 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
1472 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
1504 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
    
```

```

PIN #13
1536 -----
1568 x---x-x-----
1600 -x-x-x-----
1632 --x-x--x-----
1664 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
1696 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
1728 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
1760 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
PIN #12
1792 -----
1824 -----x-----
1856 -----x-x-----
1888 ---xx---x-----
1920 --x-x---x---x-----
1952 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
1984 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
2016 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
    
```

LEGEND X : FUSE NOT BLOWN
 - : FUSE BLOWN

Program 2-3. Simulation Results for Emulator PAL 1

```

1:      NAME      '74AS890/2910 EMULATOR PAL 1;
2:      DATE      04/04/85;
3:      REV       01 ;
4:      DESIGNER  RICHARD D. NAWROCKI ;
5:      COMPANY   TEXAS INSTRUMENTS ;
6:      ASSEMBLY  00001 ;
7:      LOCATION  U100 ;
8:
9:  /******
10: /* THIS DEVICE GENERATES CONTROL SIGNALS FOR THE */
11: /* '74AS890 EMULATOR OF THE 2910 MICROPROGRAM SEQUENCER. */
12: /******
13:
14: ORDER:
15:      I3, Z2, I2, Z2, I1, Z2, I0, Z2,
16:      RLD, Z2, RAOE, Z2, EN, Z44, Z2,
17:      MUX2, Z2, MUX1, Z2, MUX0, Z2,
18:      S2, Z2, S1, Z2, S0 ;
19:

```

=====

SIMULATION RESULTS

=====

													E N																		
				R	A	Z		M	M	M	S	S	S					R	A	Z		M	M	M	S	S	S				
I	I	I	I	L	R	O	4	X	X	X	2	1	0	D	E	4	2	1	0	D	E	4	2	1	0	D	E	4	2	1	0
INSTRUCTION 0													INSTRUCTION E																		
0001:	0	0	0	0	1	H	L	H	H	H	L	L	L		0029:	1	1	1	0	1	H	L	H	H	H	H	H	H			
0002:	0	0	0	0	0	H	L	H	H	H	L	L	L		0030:	1	1	1	0	0	H	L	H	H	H	H	H	H			
INSTRUCTION 1													INSTRUCTION F																		
0003:	0	0	0	1	1	H	L	H	H	H	H	L	H		0031:	1	1	1	1	1	H	L	L	H	H	L	H	L			
0004:	0	0	0	1	0	H	L	H	H	H	H	L	H		0032:	1	1	1	1	0	H	L	L	H	H	L	H	L			
INSTRUCTION 2																															
0005:	0	0	1	0	1	H	L	H	L	L	H	H	H																		
0006:	0	0	1	0	0	H	L	H	L	L	H	H	H																		
INSTRUCTION 3																															
0007:	0	0	1	1	1	H	L	H	H	H	H	H	H																		
0008:	0	0	1	1	0	H	L	H	H	H	H	H	H																		
INSTRUCTION 4																															
0009:	0	1	0	0	1	H	L	H	H	H	H	H	L																		
0010:	0	1	0	0	0	H	L	H	H	H	H	H	L																		
INSTRUCTION 5																															
0011:	0	1	0	1	1	L	H	H	L	L	H	H	L																		
0012:	0	1	0	1	0	H	L	H	L	L	H	H	L																		
INSTRUCTION 6																															
0013:	0	1	1	0	1	H	L	H	H	H	H	H	H																		
0014:	0	1	1	0	0	H	L	H	H	H	H	H	H																		
INSTRUCTION 7																															
0015:	0	1	1	1	1	L	H	H	L	L	H	H	H																		
0016:	0	1	1	1	0	H	L	H	L	L	H	H	H																		
INSTRUCTION 8																															
0017:	1	0	0	0	1	H	L	L	L	H	L	H	L																		
0018:	1	0	0	0	0	H	L	L	L	H	L	H	L																		
INSTRUCTION 9																															
0019:	1	0	0	1	1	H	L	H	L	L	H	H	H																		
0020:	1	0	0	1	0	H	L	H	L	L	H	H	H																		
INSTRUCTION A																															
0021:	1	0	1	0	1	H	L	L	H	H	L	H	H																		
0022:	1	0	1	0	0	H	L	L	H	H	L	H	H																		
INSTRUCTION B																															
0023:	1	0	1	1	1	H	L	H	H	H	L	H	H																		
0024:	1	0	1	1	0	H	L	H	H	H	L	H	H																		
INSTRUCTION C																															
0025:	1	1	0	0	1	H	L	H	H	H	H	H	H																		
0026:	1	1	0	0	0	H	L	H	H	H	H	H	H																		
INSTRUCTION D																															
0027:	1	1	0	1	1	H	L	L	H	H	L	H	L																		
0028:	1	1	0	1	0	H	L	L	H	H	L	H	L																		

3 Application Reports

Program 2-4. JEDEC Printout for Emulator PAL 1

CUPL 2.02A
 DEVICE P16L8 DLIB-c-18-5
 PARTNO 2910EM
 NAME '74AS890/2910 EMULATOR PAL 1
 REVISION 01
 DATE 04/04/85
 DESIGNER RICHARD D. NAWROCKI
 COMPANY TEXAS INSTRUMENTS
 ASSEMBLY 00001
 LOCATION U100

*V0030 01110XXXXNXLHHHHHHN
 *V0031 11111XXXXNXLLHLLHHHN
 *V0032 11110XXXXNXLLHLLHHHN
 *0757

*QP20
 *QF2048
 *G0
 *F0
 *L0000 11111111111111111111111111111111
 *L0032 11010111011011111111111111111111
 *L0256 11111111111111111111111111111111
 *L0288 11010111011111111111111111111111
 *L0320 01101011101111111111111111111111
 *L0352 10011011011111111111111111111111
 *L0512 11111111111111111111111111111111
 *L0544 11010111011111111111111111111111
 *L0576 10111011011111111111111111111111
 *L0608 01101011101111111111111111111111
 *L0768 11111111111111111111111111111111
 *L0800 11101011011111111111111111111111
 *L0832 11010111011111111111111111111111
 *L1024 11111111111111111111111111111111
 *L1056 10010111111111111111111111111111
 *L1088 10101111011111111111111111111111
 *L1120 11010111011111111111111111111111
 *L1152 10101011111111111111111111111111
 *L1280 11111111111111111111111111111111
 *L1312 10111011101111111111111111111111
 *L1536 11111111111111111111111111111111
 *L1568 01111011011111111111111111111111
 *L1600 10101011111111111111111111111111
 *L1632 11010111011111111111111111111111
 *L1792 11111111111111111111111111111111
 *L1824 11111111101111111111111111111111
 *L1856 11111011101111111111111111111111
 *L1888 11100111101111111111111111111111
 *L1920 11010111011101111111111111111111

*C7103
 *V0001 00001XXXXNXLLLLHHHHN
 *V0002 00000XXXXNXLLLLHHHHN
 *V0003 10001XXXXNXLHLLHHHHN
 *V0004 10000XXXXNXLHLLHHHHN
 *V0005 01001XXXXNXLHHHLLHN
 *V0006 01000XXXXNXLHHHLLHN
 *V0007 11001XXXXNXLHHHHHHN
 *V0008 11000XXXXNXLHHHHHHN
 *V0009 00101XXXXNXLHHLHHHHN
 *V0010 00100XXXXNXLHHLHHHHN
 *V0011 10101XXXXNXHHLHLLLN
 *V0012 10100XXXXNXLHHLHLLHN
 *V0013 01101XXXXNXLHHHHHHN
 *V0014 01100XXXXNXLHHHHHHN
 *V0015 11101XXXXNXHHLHLLLN
 *V0016 11100XXXXNXLHHHLLHN
 *V0017 00011XXXXNXLLHLLHHN
 *V0018 00010XXXXNXLLHLLHHN
 *V0019 10011XXXXNXLHHHLLHN
 *V0020 10010XXXXNXLHHHLLHN
 *V0021 01011XXXXNXLHHLHHHN
 *V0022 01010XXXXNXLLHHLHHHN
 *V0023 11011XXXXNXLLHHHHHHN
 *V0024 11010XXXXNXLLHHHHHHN
 *V0025 00111XXXXNXLHHHHHHN
 *V0026 00110XXXXNXLHHHHHHN
 *V0027 10111XXXXNXLLHLLHHN
 *V0028 10110XXXXNXLLHLLHHN
 *V0029 01111XXXXNXLHHHHHHN

Program 2-5. Logic Equations Used to Generate Emulator PAL 2

CUPL VERSION 2.02A COPYRIGHT (C) 1983,84,85 ASSISTED TECHNOLOGY, INC. -- LISTING

SOURCE FILE: B:2910EM1

DEVICE: PL6L8

```

1:          PARTNO      2910EM1 ;
2:          NAME        '74AS890/2910 EMULATOR PAL 2 ;
3:          DATE        04/04/85 ;
4:          REV         01 ;
5:          DESIGNER    RICHARD D. NAWROCKI ;
6:          COMPANY     TEXAS INSTRUMENTS ;
7:          ASSEMBLY    00001 ;
8:          LOCATION    U101 ;
9:
10: /******
11: /* THIS DEVICE GENERATES CONTROL SIGNALS FOR THE '74AS890      */
12: /* EMULATION OF THE 2910 MICROPROGRAM CONTROLLER.             */
13: /*
14: /* ALLOWABLE TARGET DEVICE TYPES: PAL16L8                      */
15: /******
16:
17: /** INPUTS **/
18:
19: PIN [1..4] = [I0..3] ; /* 2910 INSTRUCTION CODE */
20: PIN 5 = RLD ; /* 2910 REGISTER LOAD */
21: PIN 6 = CC ; /* 2910 CONDITION CODE */
22: PIN 7 = CCEN ; /* 2910 CONDITION CODE ENABLE */
23:
24: /** OUTPUTS **/
25:
26: PIN 19 = CC_OUT0 ; /* 74AS890 CONDITION CODE (1 OF 2) */
27: PIN 18 = CC_OUT1 ; /* 74AS890 CONDITION CODE (2 OF 2) */
28: PIN [17..15] = [RC2..0] ; /* 74AS890 REGISTER/COUNTER CONTROL */
29: PIN 14 = PL ; /* 2910 PIPELINE MAP OUTPUT */
30: PIN 13 = MAP ; /* 2910 PROM MAP OUTPUT */
31: PIN 12 = VECT ; /* 2910 VECTOR MAP OUTPUT */
32:
33: /** DECLARATIONS AND INTERMEDIATE VARIABLE DEFINITIONS **/
34:
35: FIELD INSTRUCTION = [I3..0] ;
36: FIELD COUNTER = [RC2..0] ;
37:
38: /** LOGIC EQUATIONS **/
39:
40: !PL = INSTRUCTION:[0,1,3..5,7..F] ;
41:
42: !MAP = INSTRUCTION:2 ;
43:
44: !VECT = INSTRUCTION:6 ;
45:
46: COUNTER = 'H'2 & INSTRUCTION:C
47:          # ('H'2 & INSTRUCTION:4 & (CCEN # !CC))
48:          # 'H'2 & !RLD
49:          # 'H'1 & RLD & INSTRUCTION:[8,9,F] ;
50:
51: CC_OUT0.OE = CCEN ;
52:
53: CC_OUT1.OE = !CCEN ;
54:
55: !CC_OUT0 = INSTRUCTION:[1,3,6,8..B] ;
56:
57: !CC_OUT1 = INSTRUCTION:[1,3,6,8..B] & !CC
58:          # INSTRUCTION:[5,7,D,F] & CC
59:          # INSTRUCTION:[8,9] ;
60:
61:

```

JEDEC FUSE CHECKSUM (791A)
 JEDEC TRANSMIT CHECKSUM (3521)

Program 2-6. Expanded Product Terms, Symbol Table and Fuse Plot for Emulator PAL 2

```

CUPL          2.02A
DEVICE        P16L8 DLIB-c-18-5
PARTNO        2910EM1
NAME          '74AS890/2910 EMULATOR PAL 2
REVISION      01
DATE          04/04/85
DESIGNER      RICHARD D. NAWROCKI
COMPANY       TEXAS INSTRUMENTS
ASSEMBLY      00001
LOCATION       U101
    
```

=====

EXPANDED PRODUCT TERMS

=====

```

CC_OUT0 ->          RC0.OE ->
  !I2 & !I3          1
# !I0 & !I2 & !I3
# !I0 & !I1 & !I2 & !I3          RC1.OE ->
                                1
CC_OUT0.OE ->          RC2.OE ->
  CCEN              1
CC_OUT1 ->          VECT.OE ->
  !CC & !I2 & !I3          1
# !I1 & !I2 & !I3
# CC & !I0 & !I2
# !CC & !I0 & !I2 & !I3
# !CC & !I0 & !I1 & !I2 & !I3
CC_OUT1.OE ->
  !CCEN
COUNTER ->
  RC2 , RC1 , RC0
INSTRUCTION ->
  I3 , I2 , I1 , I0
MAP ->
  !I0 & !I1 & !I2 & !I3
PL ->
  I3
# !I1 & !I3
# !I0 & !I1 & !I3
RC0 ->
  !I0 & !I1
# !I1 & !I2
# !I1 & !I2
# !I3
# !RLD
RC1 ->
  !I0 & RLD
# !I2 & RLD
# !I1 & RLD
# !CCEN & CC & !I3 & RLD
RC2 ->
  1
VECT ->
  !I0 & !I1 & !I2 & !I3
MAP.OE ->
  1
PL.OE ->
  1
    
```


Program 2-6. Expanded Product Terms, Symbol Table and Fuse Plot for Emulator PAL 2 (Continued)

=====

SYMBOL TABLE

=====

POL	NAME	EXT	PIN	TYPE	USED	Max
	CCEN		7	V	-	-
	CC		6	V	-	-
	CC_OUT0		19	V	3	7
	CC_OUT0	OE	19	X	1	1
	CC_OUT1		18	V	5	7
	CC_OUT1	OE	18	X	1	1
	COUNTER		0	F	-	-
	IO		1	V	-	-
	I1		2	V	-	-
	I2		3	V	-	-
	I3		4	V	-	-
	INSTRUCTION		0	F	-	-
	MAP		13	V	1	7
	PL		14	V	3	7
	RC0		15	V	5	7
	RC1		16	V	4	7
	RC2		17	V	1	7
	RLD		5	V	-	-
	VECT		12	V	1	7
	MAP	OE	13	D	1	1
	PL	OE	14	D	1	1
	RC0	OE	15	D	1	1
	RC1	OE	16	D	1	1
	RC2	OE	17	D	1	1
	VECT	OE	12	D	1	1

LEGEND D : DEFAULT VAR F : FIELD I : INTERMEDIATE VAR
 U : UNDEFINED V : VAR X : EXTENDED VAR
 N : NODE M : EXTENDED NODE

=====

FUSE PLOT

=====

PIN #19

```

0000 -----x-----
0032 -----x-x-----
0064 --x-x-x-----
0096 x-xx-x-----
0128 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0160 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0192 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0224 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
PIN #18
0256 -----x-----
0288 -----x-x-----x
0320 -x-x-x-----
0352 --x-x-----x
0384 -x-x-x-----x
0416 x-xx-x-----x
0448 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0480 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
PIN #17
0512 -----
0544 -----
0576 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0608 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0640 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0672 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0704 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0736 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
    
```

PIN #16

```

0768 -----
0800 --x-----x
0832 --x-x-----x
0864 x-----x-----
0896 -----x-x-x-x-----
0928 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0960 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0992 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
PIN #15
1024 -----
1056 x-x-----
1088 -x-x-----
1120 x--x-----
1152 -----x-----
1184 -----x-----
1216 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
1248 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
PIN #14
1280 -----
1312 -----x-----
1344 -x-----x-----
1376 x-x-----x-----
1408 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
1440 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
1472 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
1504 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
    
```

Program 2-6. Expanded Product Terms, Symbol Table and Fuse Plot for Emulator PAL 2 (Continued)

```
PIN #13
1536 -----
1568 x--x-x---x-----
1600 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
1632 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
1664 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
1696 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
1728 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
1760 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
PIN #12
1792 -----
1824 x--xx----x-----
1856 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
1888 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
1920 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
1952 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
1984 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
2016 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

LEGEND x : FUSE NOT BLOWN
 - : FUSE BLOWN

Program 2-7. Simulation Results for Emulator PAL 2

```

1:      NAME      '74AS890/2910 EMULATOR PAL 2 ;
2:      DATE      04/04/85 ;
3:      REV       01 ;
4:      DESIGNER  RICHARD D. NAWROCKI ;
5:      COMPANY   TEXAS INSTRUMENTS ;
6:      ASSEMBLY  00001 ;
7:      LOCATION  U101 ;
8:
9:  /*****
10: /* THIS DEVICE GENERATES CONTROL SIGNALS FOR THE */
11: /* '74AS890 EMULATOR OF THE 2910 MICROPROGRAM SEQUENCER. */
12: *****/
13:
14: ORDER:
15:  I3, Z2, I2, Z2, I1, Z2, I0, Z2,
16:  CC, Z2, CCEN, Z2, RLD, Z2,
17:  PL, Z2, MAP, Z2, VECT, Z2,
18:  CC_OUT1, Z2, CC_OUT0, Z2,
19:  RC2, Z2, RC1, Z2, RC0 ;
20:

```

=====

SIMULATION RESULTS

=====

	I	I	I	I	C	C	R	P	M	V	C	U	U	R	R	R
	3	2	1	0	C	C	L	P	A	E	T	1	0	2	1	0
INSTRUCTION 0																
0001:	0	0	0	0	1	0	1	L	H	H	H	Z	L	L	L	L
0002:	0	0	0	0	1	0	0	L	H	H	H	Z	L	L	L	L
0003:	0	0	0	0	0	0	1	L	H	H	H	Z	L	L	L	L
0004:	0	0	0	0	0	0	0	L	H	H	H	Z	L	L	L	L
0005:	0	0	0	0	1	1	1	L	H	H	H	Z	L	L	L	L
0006:	0	0	0	0	1	1	0	L	H	H	H	Z	L	L	L	L
0007:	0	0	0	0	0	1	1	L	H	H	H	Z	L	L	L	L
0008:	0	0	0	0	0	1	0	L	H	H	H	Z	L	L	L	L
INSTRUCTION 1																
0009:	0	0	0	1	1	0	1	L	H	H	H	Z	L	L	L	L
0010:	0	0	0	1	1	0	0	L	H	H	H	Z	L	L	L	L
0011:	0	0	0	1	0	0	1	L	H	H	H	Z	L	L	L	L
0012:	0	0	0	1	0	0	0	L	H	H	H	Z	L	L	L	L
0013:	0	0	0	1	1	1	1	L	H	H	H	Z	L	L	L	L
0014:	0	0	0	1	1	1	0	L	H	H	H	Z	L	L	L	L
0015:	0	0	0	1	0	1	1	L	H	H	H	Z	L	L	L	L
0016:	0	0	0	1	0	1	0	L	H	H	H	Z	L	L	L	L
INSTRUCTION 2																
0017:	0	0	1	0	1	0	1	H	L	H	H	Z	L	L	L	L
0018:	0	0	1	0	1	0	0	H	L	H	H	Z	L	L	L	L
0019:	0	0	1	0	0	0	1	H	L	H	H	Z	L	L	L	L
0020:	0	0	1	0	0	0	0	H	L	H	H	Z	L	L	L	L
0021:	0	0	1	0	1	1	1	H	L	H	H	Z	L	L	L	L
0022:	0	0	1	0	1	1	0	H	L	H	H	Z	L	L	L	L
0023:	0	0	1	0	0	1	1	H	L	H	H	Z	L	L	L	L
0024:	0	0	1	0	0	1	0	H	L	H	H	Z	L	L	L	L
INSTRUCTION 3																
0025:	0	0	1	1	1	0	1	L	H	H	H	Z	L	L	L	L
0026:	0	0	1	1	1	0	0	L	H	H	H	Z	L	L	L	L
0027:	0	0	1	1	0	0	1	L	H	H	H	Z	L	L	L	L
0028:	0	0	1	1	0	0	0	L	H	H	H	Z	L	L	L	L
0029:	0	0	1	1	1	1	1	L	H	H	H	Z	L	L	L	L
0030:	0	0	1	1	1	1	0	L	H	H	H	Z	L	L	L	L
0031:	0	0	1	1	0	1	1	L	H	H	H	Z	L	L	L	L
0032:	0	0	1	1	0	1	0	L	H	H	H	Z	L	L	L	L

Program 2-7. Simulation Results for Emulator PAL 2 (Continued)

	I 3	I 2	I 1	I 0	C C	C E N	R L D	P L	M A P	V E C T	C C - O U T 1	C C - O U T 0	R C 2	R C 1	R C 0
INSTRUCTION 4															
0033:	0	1	0	0	1	0	1	L	H	H	H	Z	L	L	L
0034:	0	1	0	0	1	0	0	L	H	H	H	Z	L	L	L
0035:	0	1	0	0	0	0	1	L	H	H	H	Z	L	L	L
0036:	0	1	0	0	0	0	0	L	H	H	H	Z	L	L	L
0037:	0	1	0	0	1	1	1	L	H	H	H	Z	L	L	L
0038:	0	1	0	0	1	1	0	L	H	H	H	Z	L	L	L
0039:	0	1	0	0	0	1	1	L	H	H	H	Z	L	L	L
0040:	0	1	0	0	0	1	0	L	H	H	H	Z	L	L	L
INSTRUCTION 5															
0041:	0	1	0	1	1	0	1	L	H	H	L	Z	L	L	L
0042:	0	1	0	1	1	0	0	L	H	H	L	Z	L	L	L
0043:	0	1	0	1	0	0	1	L	H	H	H	Z	L	L	L
0044:	0	1	0	1	0	0	0	L	H	H	H	Z	L	L	L
0045:	0	1	0	1	1	1	1	L	H	H	H	Z	L	L	L
0046:	0	1	0	1	1	1	0	L	H	H	H	Z	L	L	L
0047:	0	1	0	1	0	1	1	L	H	H	H	Z	L	L	L
0048:	0	1	0	1	0	1	0	L	H	H	H	Z	L	L	L
INSTRUCTION 6															
0049:	0	1	1	0	1	0	1	H	H	L	H	Z	L	L	L
0050:	0	1	1	0	1	0	0	H	H	L	H	Z	L	L	L
0051:	0	1	1	0	0	0	1	H	H	L	L	Z	L	L	L
0052:	0	1	1	0	0	0	0	H	H	L	L	Z	L	L	L
0053:	0	1	1	0	1	1	1	H	H	L	L	Z	L	L	L
0054:	0	1	1	0	1	1	0	H	H	L	L	Z	L	L	L
0055:	0	1	1	0	0	1	1	H	H	L	L	Z	L	L	L
0056:	0	1	1	0	0	1	0	H	H	L	L	Z	L	L	L
INSTRUCTION 7															
0057:	0	1	1	1	1	0	1	L	H	H	L	Z	L	L	L
0058:	0	1	1	1	1	0	0	L	H	H	L	Z	L	L	L
0059:	0	1	1	1	0	0	1	L	H	H	H	Z	L	L	L
0060:	0	1	1	1	0	0	0	L	H	H	H	Z	L	L	L
0061:	0	1	1	1	1	1	1	L	H	H	H	Z	L	L	L
0062:	0	1	1	1	1	1	0	L	H	H	H	Z	L	L	L
0063:	0	1	1	1	0	1	1	L	H	H	H	Z	L	L	L
0064:	0	1	1	1	0	1	0	L	H	H	H	Z	L	L	L
INSTRUCTION 8															
0065:	1	0	0	0	1	0	1	L	H	H	L	Z	L	L	H
0066:	1	0	0	0	1	0	0	L	H	H	L	Z	L	L	H
0067:	1	0	0	0	0	0	1	L	H	H	L	Z	L	L	H
0068:	1	0	0	0	0	0	0	L	H	H	L	Z	L	L	H
0069:	1	0	0	0	1	1	1	L	H	H	H	Z	L	L	H
0070:	1	0	0	0	1	1	0	L	H	H	H	Z	L	L	H
0071:	1	0	0	0	0	1	1	L	H	H	H	Z	L	L	H
0072:	1	0	0	0	0	1	0	L	H	H	H	Z	L	L	H
INSTRUCTION 9															
0073:	1	0	0	1	1	0	1	L	H	H	L	Z	L	L	H
0074:	1	0	0	1	1	0	0	L	H	H	L	Z	L	L	H
0075:	1	0	0	1	0	0	1	L	H	H	L	Z	L	L	H
0076:	1	0	0	1	0	0	0	L	H	H	L	Z	L	L	H
0077:	1	0	0	1	1	1	1	L	H	H	H	Z	L	L	H
0078:	1	0	0	1	1	1	0	L	H	H	H	Z	L	L	H
0079:	1	0	0	1	0	1	1	L	H	H	H	Z	L	L	H
0080:	1	0	0	1	0	1	0	L	H	H	H	Z	L	L	H
INSTRUCTION A															
0081:	1	0	1	0	1	0	1	L	H	H	H	Z	L	L	L
0082:	1	0	1	0	1	0	0	L	H	H	H	Z	L	L	L
0083:	1	0	1	0	0	0	1	L	H	H	L	Z	L	L	L
0084:	1	0	1	0	0	0	0	L	H	H	L	Z	L	L	L
0085:	1	0	1	0	1	1	1	L	H	H	H	Z	L	L	L
0086:	1	0	1	0	1	1	0	L	H	H	H	Z	L	L	L
0087:	1	0	1	0	0	1	1	L	H	H	H	Z	L	L	L
0088:	1	0	1	0	0	1	0	L	H	H	H	Z	L	L	L

Program 2-7. Simulation Results for Emulator PAL 2 (Continued)

	I 3	I 2	I 1	I 0	C C	C E N	R L D	P L	M A P	V E C T	C C - O U T 1	C C - O U T 0	R C 2	R C 1	R C 0
INSTRUCTION B															
0089:	1	0	1	1	1	1	0	1	L	H	H	Z	L	L	L
0090:	1	0	1	1	1	0	0	1	L	H	H	Z	L	L	L
0091:	1	0	1	1	0	0	0	1	L	H	H	Z	L	L	L
0092:	1	0	1	1	0	0	0	0	L	H	H	Z	L	L	L
0093:	1	0	1	1	1	1	1	1	L	H	H	Z	L	L	L
0094:	1	0	1	1	1	1	0	1	L	H	H	Z	L	L	L
0095:	1	0	1	1	0	1	1	1	L	H	H	Z	L	L	L
0096:	1	0	1	1	0	1	0	1	L	H	H	Z	L	L	L
INSTRUCTION C															
0097:	1	1	0	0	1	0	1	L	H	H	Z	L	H	L	L
0098:	1	1	0	0	1	0	0	1	L	H	H	Z	L	L	L
0099:	1	1	0	0	0	0	0	1	L	H	H	Z	L	L	L
0100:	1	1	0	0	0	0	0	0	L	H	H	Z	L	L	L
0101:	1	1	0	0	1	1	1	1	L	H	H	Z	H	L	L
0102:	1	1	0	0	1	1	0	1	L	H	H	Z	H	L	L
0103:	1	1	0	0	0	1	1	1	L	H	H	Z	H	L	L
0104:	1	1	0	0	0	1	0	L	H	H	Z	H	L	L	L
INSTRUCTION D															
0105:	1	1	0	1	1	0	1	L	H	H	L	Z	L	L	L
0106:	1	1	0	1	1	0	0	1	L	H	H	Z	L	L	L
0107:	1	1	0	1	0	0	0	1	L	H	H	Z	L	L	L
0108:	1	1	0	1	0	0	0	0	L	H	H	Z	L	L	L
0109:	1	1	0	1	1	1	1	1	L	H	H	Z	H	L	L
0110:	1	1	0	1	1	1	0	1	L	H	H	Z	H	L	L
0111:	1	1	0	1	0	1	1	1	L	H	H	Z	H	L	L
0112:	1	1	0	1	0	1	0	L	H	H	Z	H	L	L	L
INSTRUCTION E															
0113:	1	1	1	0	1	0	1	L	H	H	H	Z	L	L	L
0114:	1	1	1	0	1	0	0	1	L	H	H	Z	L	L	L
0115:	1	1	1	0	0	0	0	1	L	H	H	Z	L	L	L
0116:	1	1	1	0	0	0	0	0	L	H	H	Z	L	L	L
0117:	1	1	1	0	1	1	1	1	L	H	H	Z	H	L	L
0118:	1	1	1	0	1	1	0	1	L	H	H	Z	H	L	L
0119:	1	1	1	0	0	1	1	1	L	H	H	Z	H	L	L
0120:	1	1	1	0	0	1	0	L	H	H	Z	H	L	L	L
INSTRUCTION F															
0121:	1	1	1	1	1	0	1	L	H	H	L	Z	L	L	H
0122:	1	1	1	1	1	0	0	1	L	H	H	Z	L	L	L
0123:	1	1	1	1	0	0	0	1	L	H	H	Z	L	L	L
0124:	1	1	1	1	0	0	0	0	L	H	H	Z	L	L	L
0125:	1	1	1	1	1	1	1	1	L	H	H	Z	H	L	L
0126:	1	1	1	1	1	1	0	1	L	H	H	Z	H	L	L
0127:	1	1	1	1	1	0	1	1	L	H	H	Z	H	L	L
0128:	1	1	1	1	0	1	0	L	H	H	Z	H	L	L	L

Program 2-8. JEDEC Printout for Emulator PAL 2

CUPL 2.02A
 DEVICE P16L8 DLIB-c-18-5
 PARTNO 2910EM1
 NAME 74AS890/2910 EMULATOR PAL 2
 REVISION 01
 DATE 04/04/85
 DESIGNER RICHARD D. NAWROCKI
 COMPANY TEXAS INSTRUMENTS
 ASSEMBLY 00001
 LOCATION U101

*QP20
 *QF2048
 *G0
 *F0
 *L0000 11111111111111111111111111111111
 *L0032 11111011011111111111111111111111
 *L0064 11011011101111111111111111111111
 *L0096 01100111101111111111111111111111
 *L0256 1111111111111111111111101111111111
 *L0288 1111101101111111111110111111111111
 *L0320 10111011011111111111111111111111
 *L0352 1101011111111111111011111111111111
 *L0384 1101101110111111111110111111111111
 *L0416 0110011110111111111110111111111111
 *L0512 11111111111111111111111111111111
 *L0544 11111111111111111111111111111111
 *L0768 11111111111111111111111111111111
 *L0800 11011111111101111111111111111111
 *L0832 11111011111110111111111111111111
 *L0864 01111111111101111111111111111111
 *L0896 1111111110110111011110111111111111
 *L1024 11111111111111111111111111111111
 *L1056 01101111111111111111111111111111
 *L1088 10110111111111111111111111111111
 *L1120 01111011111111111111111111111111
 *L1152 11111111101111111111111111111111
 *L1184 11111111111101111111111111111111
 *L1280 11111111111111111111111111111111
 *L1312 11111111101111111111111111111111
 *L1344 10111111101111111111111111111111
 *L1376 01011111101111111111111111111111
 *L1536 11111111111111111111111111111111
 *L1568 01101011101111111111111111111111
 *L1792 11111111111111111111111111111111
 *L1824 01100111101111111111111111111111

*C791A
 *V0001 0000110XXNXHLLHLLHZN
 *V0002 0000010XXNXHLLHLHZN
 *V0003 0000100XXNXHLLHLLHZN
 *V0004 0000000XXNXHLLHLHZN
 *V0005 0000111XXNXHLLHLLHZN
 *V0006 0000011XXNXHLLHLHZN
 *V0007 0000101XXNXHLLHLLHZN
 *V0008 0000001XXNXHLLHLHZN
 *V0009 1000110XXNXHLLHLLHZN
 *V0010 1000010XXNXHLLHLHZN
 *V0011 1000100XXNXHLLHLLHZN
 *V0012 1000000XXNXHLLHLLHZN
 *V0013 1000111XXNXHLLHLLHZN
 *V0014 1000011XXNXHLLHLHZN
 *V0015 1000101XXNXHLLHLLHZN
 *V0016 1000001XXNXHLLHLHZN
 *V0017 0100110XXNXHLHLLHZN
 *V0018 0100010XXNXHLHLHZN
 *V0019 0100100XXNXHLHLLHZN
 *V0020 0100000XXNXHLHLHZN
 *V0021 0100111XXNXHLHLLHZN
 *V0022 0100011XXNXHLHLHZN
 *V0023 0100101XXNXHLHLLHZN
 *V0024 0100001XXNXHLHLHZN
 *V0025 1100110XXNXHLLHLLHZN
 *V0026 1100010XXNXHLLHLHZN
 *V0027 1100100XXNXHLLHLLHZN

Program 2-8. JEDEC Printout for Emulator PAL 2 (Continued)

```

*V0028 1100000XXNXHHLLHLLZN
*V0029 1100111XXNXHHLLLZLN
*V0030 1100011XXNXHHLLHLZLN
*V0031 1100101XXNXHHLLLZLN
*V0032 1100001XXNXHHLLHLZLN
*V0033 0010110XXNXHHLLLHZN
*V0034 0010010XXNXHHLLHLHZN
*V0035 0010100XXNXHHLLHLHZN
*V0036 0010000XXNXHHLLHLHZN
*V0037 0010111XXNXHHLLHLZHN
*V0038 0010011XXNXHHLLHLZHN
*V0039 0010101XXNXHHLLHLZHN
*V0040 0010001XXNXHHLLHLZHN
*V0041 1010110XXNXHHLLLZLN
*V0042 1010010XXNXHHLLHLZLN
*V0043 1010100XXNXHHLLHLHZN
*V0044 1010000XXNXHHLLHLHZN
*V0045 1010111XXNXHHLLLZHN
*V0046 1010011XXNXHHLLHLZHN
*V0047 1010101XXNXHHLLLZHN
*V0048 1010001XXNXHHLLHLZHN
*V0049 0110110XXNXHLLHLLHZN
*V0050 0110010XXNXHLLHLLHZN
*V0051 0110100XXNXHLLHLLZLN
*V0052 0110000XXNXHLLHLLZLN
*V0053 0110111XXNXHLLHLLZLN
*V0054 0110011XXNXHLLHLLZLN
*V0055 0110101XXNXHLLHLLZLN
*V0056 0110001XXNXHLLHLLZLN
*V0057 1110110XXNXHHLLLZLN
*V0058 1110010XXNXHHLLHLZLN
*V0059 1110100XXNXHHLLLHZN
*V0060 1110000XXNXHHLLHLHZN
*V0061 1110111XXNXHHLLLZHN
*V0062 1110011XXNXHHLLHLZHN
*V0063 1110101XXNXHHLLHLZHN
*V0064 1110001XXNXHHLLHLZHN
*V0065 0001110XXNXHHLLHLLZLN
*V0066 0001010XXNXHHLLHLLZLN
*V0067 0001100XXNXHHLLHLLZLN
*V0068 0001000XXNXHHLLHLLZLN
*V0069 0001111XXNXHHLLHLLZLN
*V0070 0001011XXNXHHLLHLZLN
*V0071 0001101XXNXHHLLHLZLN
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*V0074 1001010XXNXHHLLHLLZLN
*V0075 1001100XXNXHHLLHLLZLN
*V0076 1001000XXNXHHLLHLLZLN
*V0077 1001111XXNXHHLLHLZLN
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*V0080 1001001XXNXHHLLHLZLN
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*V0082 0101010XXNXHHLLHLHZN
*V0083 0101100XXNXHHLLLHZN
*V0084 0101000XXNXHHLLHLLZLN
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*V0090 1101010XXNXHHLLHLHZN
*V0091 1101100XXNXHHLLLZLN
*V0092 1101000XXNXHHLLHLZLN
*V0093 1101111XXNXHHLLLZLN
*V0094 1101011XXNXHHLLHLZLN
*V0095 1101101XXNXHHLLLZLN
*V0096 1101001XXNXHHLLHLZLN
*V0097 0011110XXNXHHLLHLHZN
*V0098 0011010XXNXHHLLHLHZN
*V0099 0011100XXNXHHLLHLHZN
*V0100 0011000XXNXHHLLHLHZN
*V0101 0011111XXNXHHLLHLZHN
*V0102 0011011XXNXHHLLHLZHN
*V0103 0011101XXNXHHLLHLZHN
*V0104 0011001XXNXHHLLHLZHN
*V0105 1011110XXNXHHLLLZLN
*V0106 1011010XXNXHHLLHLZLN
*V0107 1011000XXNXHHLLLHZN
*V0108 1011000XXNXHHLLHLHZN
*V0109 1011111XXNXHHLLLZHN
*V0110 1011011XXNXHHLLHLZHN
*V0111 1011101XXNXHHLLLZHN
*V0112 1011001XXNXHHLLHLZHN
*V0113 0111101XXNXHHLLHLHZN
*V0114 0111010XXNXHHLLHLHZN
*V0115 0111000XXNXHHLLLHZN
*V0116 0111000XXNXHHLLHLHZN
*V0117 0111111XXNXHHLLLZHN
*V0118 0111011XXNXHHLLHLZHN
*V0119 0111010XXNXHHLLLZHN
*V0120 0111001XXNXHHLLHLZHN
*V0121 1111110XXNXHHLLLZLN
*V0122 1111010XXNXHHLLHLZLN
*V0123 1111000XXNXHHLLHLHZN
*V0124 1111000XXNXHHLLHLHZN
*V0125 1111111XXNXHHLLHLZHN
*V0126 1111011XXNXHHLLHLZHN
*V0127 1111101XXNXHHLLHLZHN
*V0128 1111001XXNXHHLLHLZHN
*A128

```

Section 3

Minimum Cycle Time Delay Calculations for a 16-Bit System

This article examines some timings for a typical 16-bit computer system using a bit-slice processor and microsequencer. Comparative data for systems using TI's 'AS888-1/'AS890-1, AMD's Am2901C/2910A, and AMD's Am2903A/2910A are presented. Timing calculations are based on data from TI SN74AS888/890 family data sheets and from the *AMD2900 Family Bipolar Microprocessor Logic and Interface 1985 Data Book*.

16-BIT COMPUTER SYSTEM DESIGN

Figure 3-1 shows a basic design for a 16-bit computer system. The computer control unit (CCU), shown on the left side of the dotted line, executes microcode from the microprogram memory (also known as the control store). A one-level pipeline design is used to speed data processing,

allowing the address and contents of the next instruction to be fetched while the current instruction is being executed. The arithmetic logic unit, consisting of the bit-slice processor chips and any other logic needed to process the data, is shown on the right side of the figure.

This section compares the time required to perform the following functions, using TI's SN74AS888-1/890-1, AMD's Am2901C/2910A and AMD's Am2903A/2910A bit-slice products:

1. addition
2. addition with a shift
3. unsigned integer multiplication
4. unsigned integer division.

Cases 3 and 4 are not included in the Am2901C/Am2910A discussion, since the Am2901C does not incorporate internal multiplication or division algorithms.

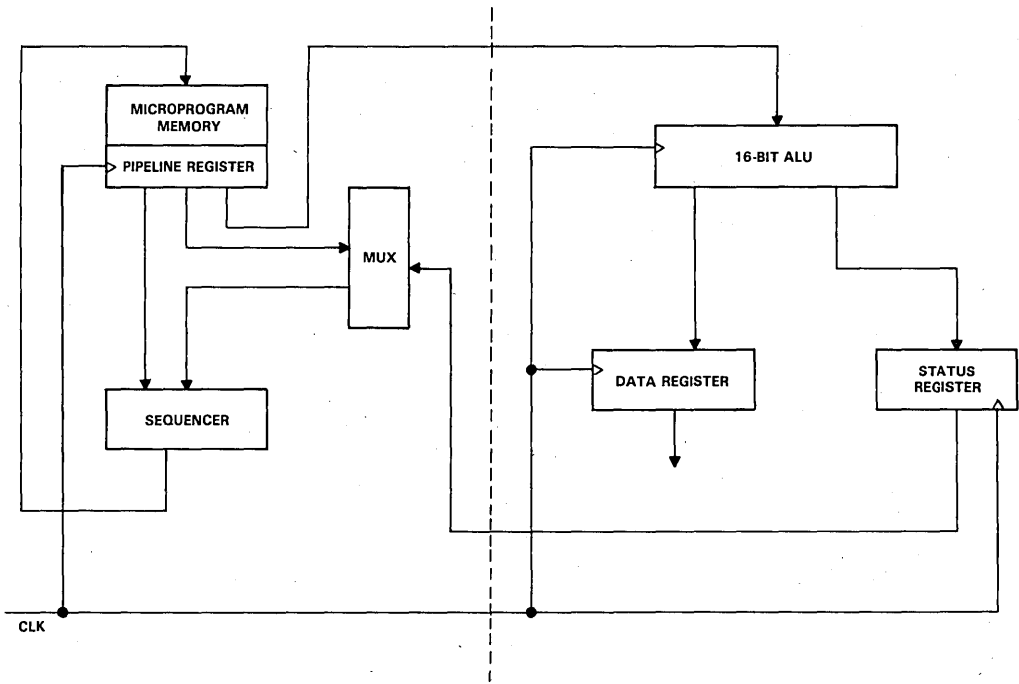


Figure 3-1. 16-Bit Computer System

Benchmark I: Comparison of Am2903A/2910A with 'AS888-1/'AS890-1

Design of a 16-bit system that is Am2903A-based is presented in Figure 3-2. The same system implemented with the 'AS888-1 and 'AS890-1 is shown in Figure 3-3. These systems are used to calculate timings for the four cases discussed in this section. Timings for the control path are given in the first test case and remain constant for the remaining three cases.

Tables 3-1 and 3-2 contain timing results for addition using the two chip sets; Tables 3-3 and 3-4 analyze the add with shift combination. It can be seen that the TI system runs 36% faster for addition and 32% faster for addition followed by a shift of the result.

Figures 3-4 and 3-5 show the ALU data paths used for multiplication and division by the two systems. Tables 3-5, 3-6 and 3-7 display timings for the critical path calculations for these operations. Increases in speed using the TI parts are even more significant here, where multiplication is faster by 42% and division faster by 37%.

Benchmark II: Comparison of Am2901C/2910A with 'AS888-1/'AS890-1

The same 16-bit system can be constructed with Am2901C slices. Since the Am2901C has a smaller instruction set than the Am2903A or the 'AS888-1, multiplication and division must be emulated using external add with shift hardware and bit testing. For this reason, the comparison for this benchmark is restricted to the cases of addition and addition with shift.

The basic system for these two cases using the Am2901C is shown in Figure 3-6; timing calculations for the control and data paths are listed in Table 3-8. These can be compared directly with the 'AS888 design and calculations shown previously in Figure 3-3 and Table 3-2. Addition is 13% faster using the AS888-1.

To implement the shift function, two multiplexers and an exclusive-OR gate are needed. A modified design is shown in Figure 3-7, along with timing calculations in Table 3-9. A comparison of these with Figure 3-3 and data in Table 3-4 shows that the TI system performs an addition with shift 25% faster than the Am2901C equivalent.

SUMMARY OF RESULTS

Table 3-10 summarizes the timings of the various cases implemented with the TI and AMD parts. It can be seen that the TI 'AS888-1/'AS890-1 system runs faster than the others in all cases. Addition using the TI parts can be performed 26% faster than with the system using the Am2901C and 36% faster than that using the Am2903A. Addition with a

shift is 25% faster on the TI system than the Am2901C system and 32% faster than the Am2903C. An even wider variance occurs with the more complicated algorithms: multiplication is 42% faster using the TI chip; division is 37% faster.

Table 3-1. Am2903A/Am2910A Timings for Addition

COMPONENT	DATA PATH	TIME (NS)
Data Loop		
Pipeline register	Clock to output	9
Am2903A	A, B to \overline{G} , \overline{P}	52
Am2902A	$\overline{G0}$, $\overline{P0}$ to C_{n+z}	7
Am2903A	C_n to C_{n+4} , OVR, Z, Y	35
Am2903A	Setup time	5
Total for data loop		108
Control Loop		
Pipeline register	Clock to output	9
MUX	Select to output	13
Am2910A	\overline{CC} to output	30
PROM	Access time	20
Pipeline register	Setup time	2
Total for control loop		74
Critical path for Am2903 addition		108

Table 3-2. 'AS888-1/'AS890-1 Timings for Addition

COMPONENT	DATA PATH	TIME (NS)
Data Loop		
Pipeline register	Clock to output	9
'AS888-1	A, B to C_{n+8}	30
'AS888-1	C_n to C_{n+8} , OVR, Z, Y	27
Register	Setup time	2
Total for data loop		68
Control Loop		
Pipeline register	Clock to output	9
MUX	Select to output	13
'AS890-1	\overline{CC} to output	25
PROM	Access time	20
Pipeline register	Setup time	2
Total Control Loop		69
Critical path for 'AS888 addition		69

Table 3-3. Am2903A/Am2910A Timings for Addition with Shift

COMPONENT	DATA PATH	TIME (NS)
Data Loop		
Pipeline register	Clock to output	9
Am2903A	A, B to \overline{G} , \overline{P}	52
Am2902A	$\overline{G0}$, $\overline{P0}$ to C_{n+z}	7
Am2903A	C_n to C_{n+4} , $\overline{SIO0}$	23
Am2903A	$\overline{SIO}(n)$ shift to Y	23
Am2903A	RAM setup	5
	Total for data loop	119
Control Loop		
Pipeline register	Clock to output	9
MUX	Select to output	13
Am2910A	\overline{CC} to output	30
PROM	Access time	20
Pipeline register	Setup time	2
	Total for control loop	74
Critical path for AM2903 addition with shift		119

Table 3-5. Am2903A/Am2910A Timings for Multiplication

COMPONENT	DATA PATH	TIME (NS)
Data Loop		
Am2918	Clock to output	27
Am2903A	I8-I0 to \overline{G} , \overline{P}	71
Am2902A	$\overline{G0}$, $\overline{P0}$ to C_{n+z}	7
Am2903A	C_n to C_{n+4} , $\overline{SIO0}$	23
Am2903A	$\overline{SIO}(n)$ shift to Y	23
	Total for data loop	151
Control Loop		
Pipeline register	Clock to output	9
MUX	Select to output	13
Am2910A	\overline{CC} to output	30
PROM	Access time	20
Pipeline register	Setup time	2
	Total for control loop	74
Critical path for Am2903 multiplication		151

Table 3-4. 'AS888-1/'AS890-1 Timings for Addition with Shift

COMPONENT	DATA PATH	TIME (NS)
Data Loop		
Pipeline register	Clock to output	9
'AS888-1	A, B to C_{n+8}	30
'AS888-1	C_n to C_{n+8} , $\overline{SIO0}$	25
'AS888-1	$\overline{SIO}(n)$ shift to Y	14
'AS888-1	Register file setup time	2
	Total for data loop	80
Control Loop		
Pipeline register	Clock to output	9
MUX	Select to output	13
'AS890-1	\overline{CC} to output	25
PROM	Access time	20
Pipeline register	Setup time	2
	Total for control loop	69
Critical path for 'AS888 addition with shift		80

Table 3-6. Am2903A/Am2910A Timings for Division

COMPONENT	DATA PATH	TIME (NS)
Data Loop		
Am2918	Clock to output	27
Am2903A	I8-I0 to \overline{G} , \overline{P}	50
Am2902A	$\overline{G0}$, $\overline{P0}$ to C_{n+z}	7
Am2903A	C_n to C_{n+4} , $\overline{SIO0}$	32
Am2903A	$\overline{SIO}(n)$ shift to Y	23
	Total for data loop	139
Control Loop		
Pipeline register	Clock to output	9
MUX	Select to output	13
Am2910A	\overline{CC} to output	30
PROM	Access time	20
Pipeline register	Setup time	2
	Total for control loop	74
Critical path for Am2903 division		139



Table 3-7. 'AS888-1/'AS890-1 Timings for Multiplication and Division

COMPONENT	DATA PATH	TIME (NS)
Data Loop		
'AS888-1	Clock to C_{n+8}	46
'AS888-1	C_n to \overline{SI}	25
'AS888-1	$\overline{SI}(n)$ shift to Y	14
'AS888-1	Register file setup time	2
	Total for data loop	87
Control Loop		
Pipeline register	Clock to output	9
MUX	Select to output	13
'AS890-1	\overline{CC} to output	25
PROM	Access time	20
Pipeline register	Setup time	2
	Total Control Loop	69
Critical path for 'AS888 multiplication or division		87

Table 3-9. Am2901C/Am2910A Timings for Addition with Shift

COMPONENT	DATA PATH	TIME (NS)
Data Loop		
Pipeline register	Clock to output	9
Am2901C	A, B to $\overline{G}, \overline{P}$	37
Am2902A	$\overline{G0}, \overline{P0}$ to C_{n+z}	7
Am2901C	C_n to F3, OVR	22
XOR and MUX		21
Am2901C	RAM3 setup	12
	Total for data loop	108
Control Loop		
Pipeline register	Clock to output	9
MUX	Select to output	13
Am2910A	\overline{CC} to output	30
PROM	Access time	20
Pipeline register	Setup time	2
	Total for control loop	74
Critical path for Am2903 addition with shift		108

Table 3-8. Am2901C/Am2910A Timings for Addition

COMPONENT	DATA PATH	TIME (NS)
Data Loop		
Pipeline register	Clock to output	9
Am2901C	A, B to $\overline{G}, \overline{P}$	37
Am2902A	$\overline{G0}, \overline{P0}$ to C_{n+z}	7
Am2901C	C_n to C_{n+4} , OVR, F3, F = 0, Y	25
Register	Setup time	2
	Total for data loop	80
Control Loop		
Pipeline register	Clock to output	9
MUX	Select to output	13
Am2910A	\overline{CC} to output	30
PROM	Access time	20
Pipeline register	Setup time	2
	Total for control loop	74
Critical path for Am2901C addition		80

Table 3-10. Summary of Results

Operation	CALCULATED TIMINGS								
	DATA PATHS			CONTROL PATHS			SYSTEM CLOCK		
	Am2901C	Am2903A	'AS888-1	Am2901C	Am2903A	'AS888-1	Am2901C	Am2903A	'AS888-1
Addition	80	108	68	74	74	69	80	108	69
Addition with Shift	108	119	80	74	74	69	108	119	80
Multiplication	—	151	87	—	74	69	—	151	87
Division	—	139	87	—	74	69	—	139	87

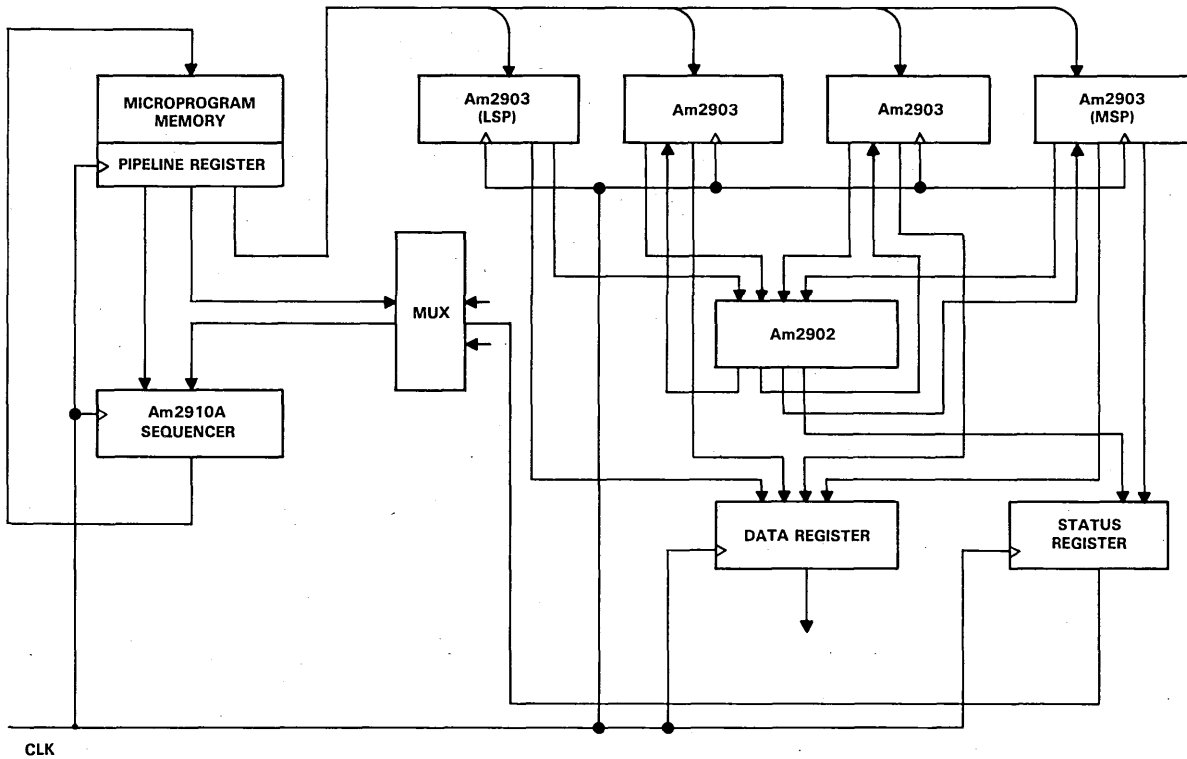


Figure 3-2. Am2903-Based 16-Bit Computer System



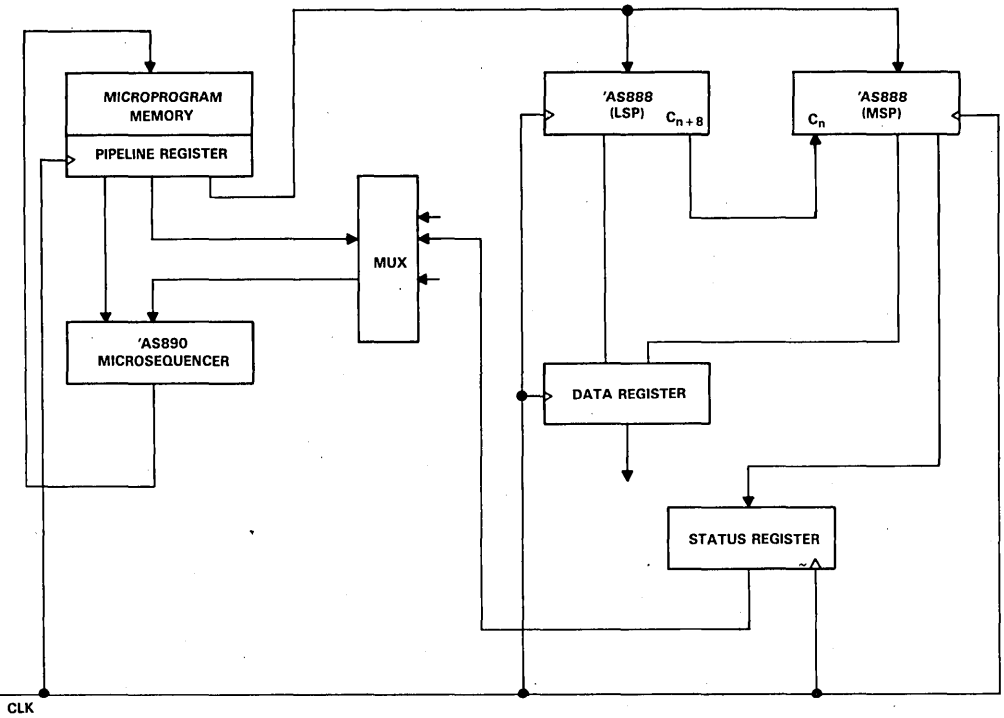


Figure 3-3. 'AS888-Based 16-Bit Computer System

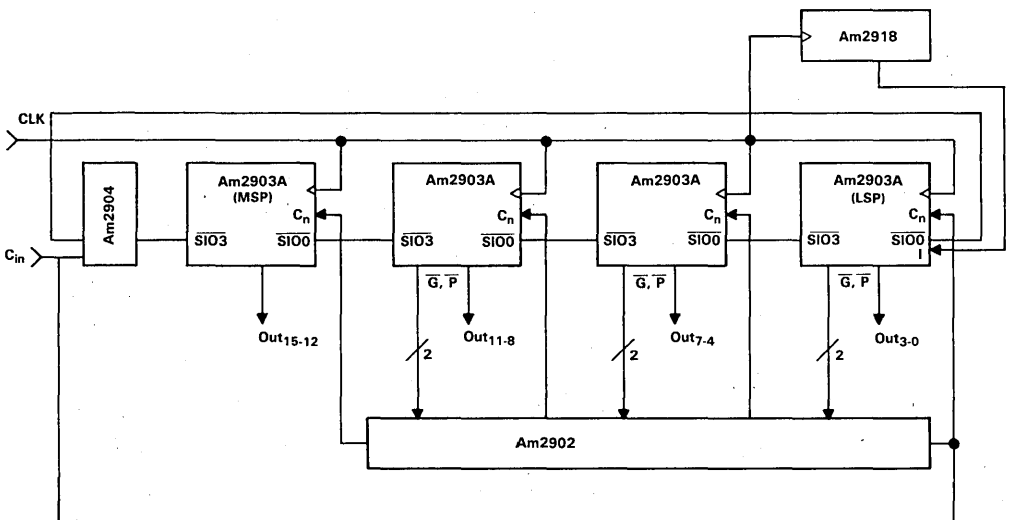


Figure 3-4. ALU Path for Multiplication and Division in the Am2903A System

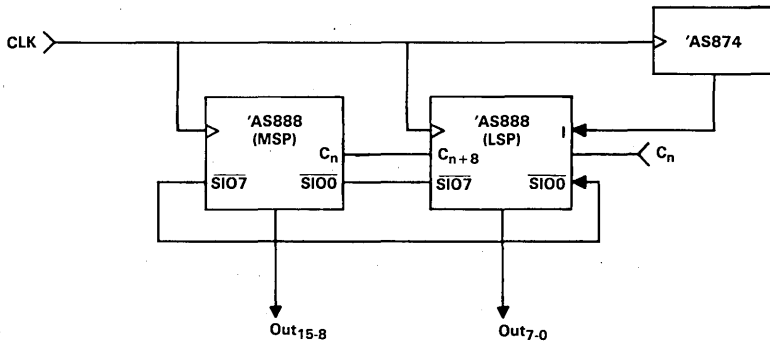


Figure 3-5. ALU Path for Multiplication and Division in the 'AS888 System

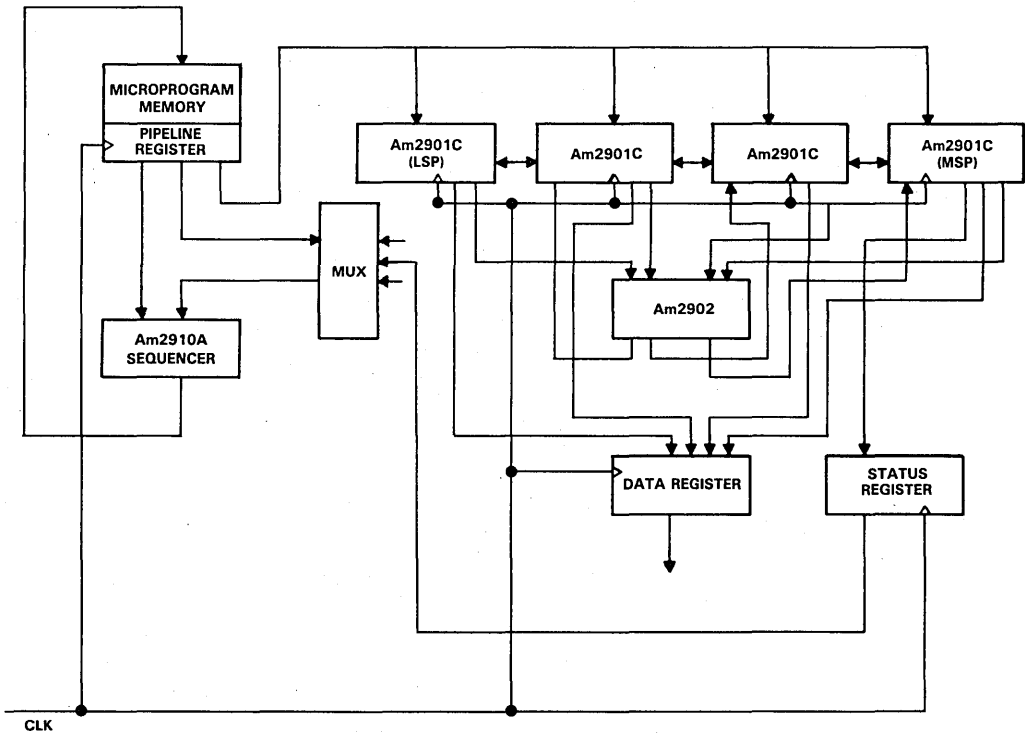


Figure 3-6. Am2901C-Based 16-Bit Computer System

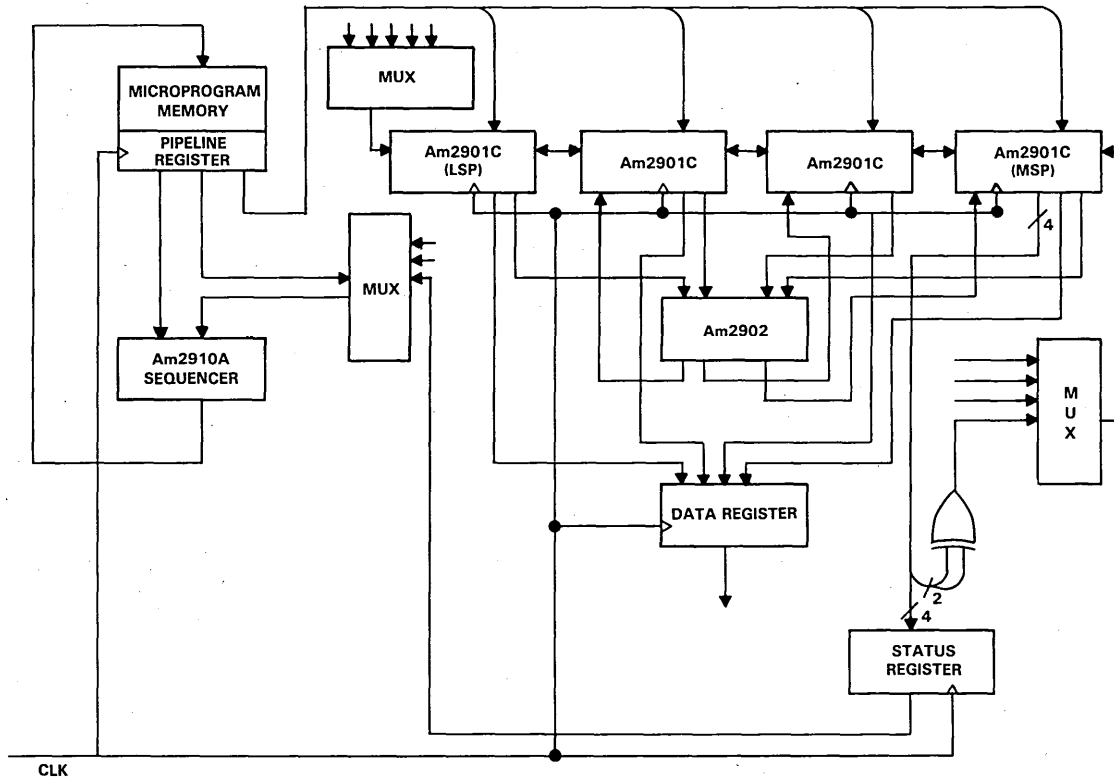


Figure 3-7. Modified Design of Am2901C-Based System

Section 4

32-Bit CPU Design With the 'AS888/'AS890

Microprogramming and bit slice technology have made possible the development of powerful systems using flexible instructions sets and wide address/data buses to access more than one gigaword of physical main memory. This section discusses one design approach to such a system, using 'AS888 bit slice and 'AS890 microsequencer components.

A structured approach to system design, such as that illustrated in Figure 4-1, is recommended in developing custom bit-slice designs. The product specification gives a starting point or basis for the project. In this example, four 'AS888 bit slices are used to implement the 32-bit arithmetic portion of the CPU, and an 'AS890 microsequencer is used for ALU and system control. A group of PROMs stores the microinstructions; a writable control store could also be implemented using additional control logic and components to load and modify the microprogram memory. The system is designed to access more than one gigaword of memory.

Since speed is a concern, carry look-ahead rather than ripple-through logic is recommended. If ripple-through logic were used, the system clock would need to be slowed down to allow the propagation of the carry bits through the various 'AS888 stages. By using carry look-ahead, the amount of time needed for the data to stabilize is greatly reduced by anticipating the carry across the 'AS888 packages.

So that the scratchpad area can be used for address calculations and mathematical computations, the 'AS888's internal register file is dedicated for system functions. To provide the system user with a macrolevel equivalent of register locations, a 16-word external register file is also included. Access to the external register file is under microprogram control, allowing address selection to come from the microcode itself or from one of the three operand fields of the instruction register.

PROMs eliminate the use of main memory as a source for constants used in initialization or table look-up functions. Accessing main memory for table values would require time and slow system throughput; by placing fixed values in fast PROMs, access time is kept to a minimum and system throughput is not altered.

Control, data and address buses shared by the system are accessed by three-state registers. The control register supplies the non-CPU part of a computer system with control signals. The data bus allows the ALU to supply data for the rest of the system and can also be a source of data for the ALU; this is accomplished by using three-state registers to drive the bidirectional data bus, along with registers to sample the bus. The address bus uses one of the external register file locations to maintain a program counter, thus allowing a 32-bit address bus capable of addressing about 4 gigawords

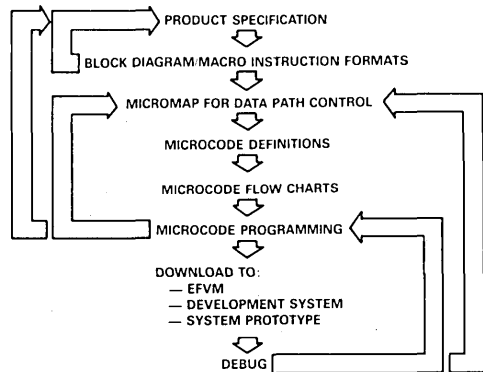


Figure 4-1. System Design Approach

of main memory. Using three-state drivers for this bus enables other subsystems to take control of the system buses.

A pipeline register supplies the microsequencer and the ALU with both data and instructions. To get macrocode into the system, an instruction register and a mapping PROM are used to convert the opcode to a microprogram routine address. The condition code signal, used for testing various conditions, is supplied by a register-input-based PAL. PAL inputs can be fixed values or combinations of the status signals coming from the ALU. The read address select pins for the 'AS888's internal B register can be sourced from the microword itself or from three nibbles of the macroword, to provide offsets for the N-way branches to various microcode routines.

DESIGNING A 32-BIT SYSTEM

A typical 32-bit system block diagram using the 'AS888 Bit-Slice and 'AS890 Microsequencer is shown in Figures 4-2 and 4-3. It can be broken down into two sections, the ALU (arithmetic logic unit) and the CCU (computer control unit). The ALU section performs all manipulation of data both to and from main memory, such as arithmetic and logical operations. The CCU section controls instruction (macro-code) flow and any miscellaneous control operations, such as fetching instructions or supplying addresses for main memory access.

Construction of the ALU

To cascade the four 'AS888s to obtain the 32-bit arithmetic unit shown in Figure 4-4, the shift multiplex SIOO

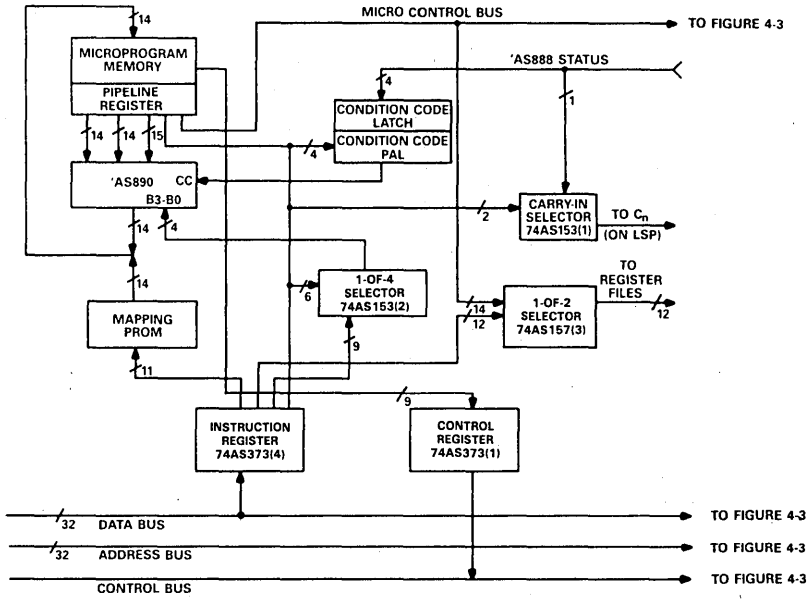


Figure 4-2. CCU Block Diagram

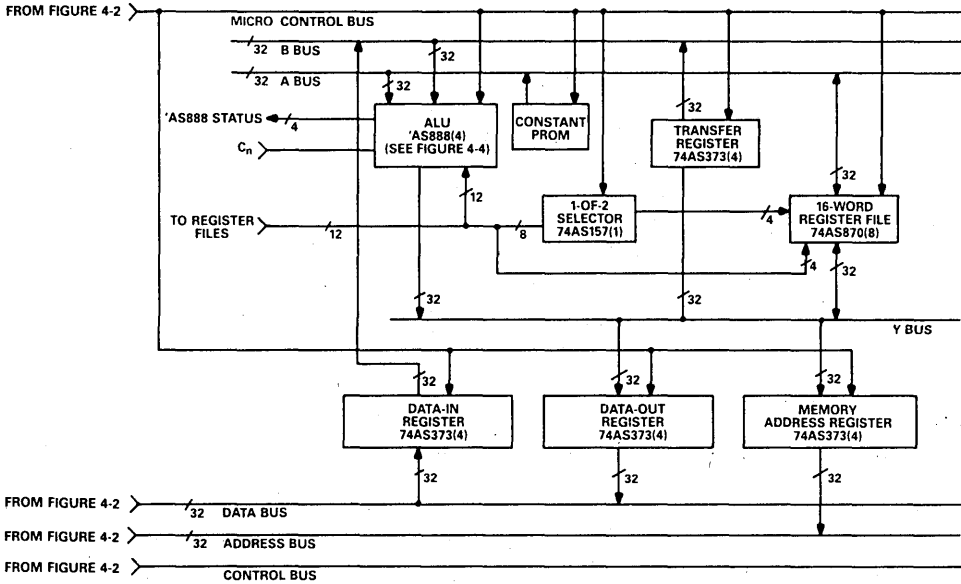


Figure 4-3. ALU Block Diagram

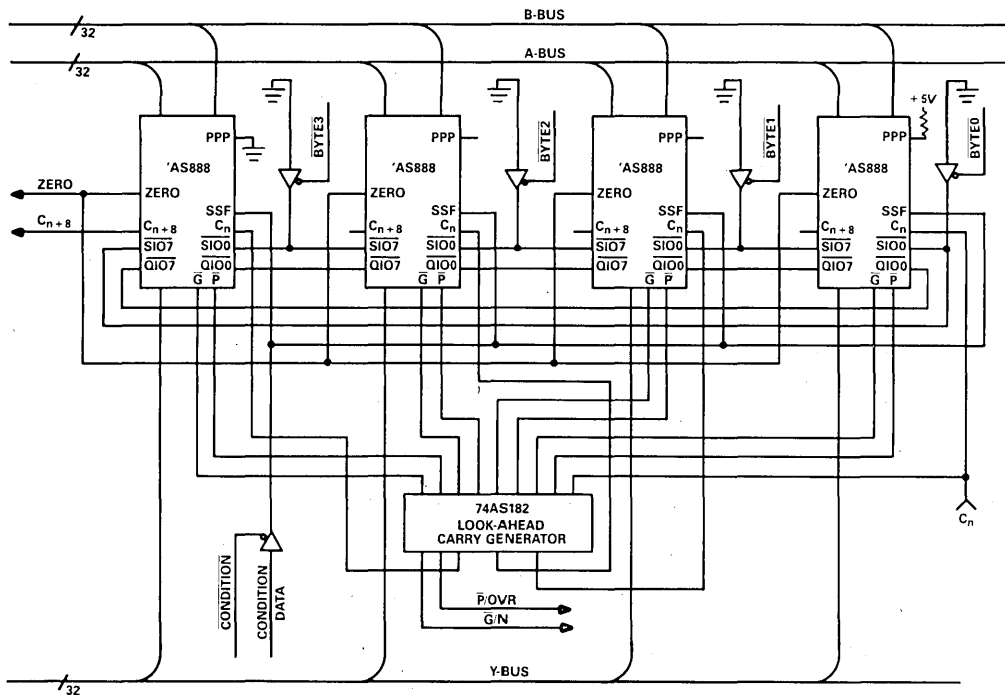


Figure 4-4. Cascaded 'AS888 Packages

and $\overline{QIO0}$ terminals are connected to the $\overline{SIO7}$ and $\overline{QIO7}$ terminals of adjacent packages, and the least significant package's signals are connected to the most-significant package's. Optionally, the SN74ALS240 inverting gates can be connected to the $\overline{SIO0}$ - $\overline{SIO7}$ terminals and the byte inputs to implement byte and bit control. Another chip, the SN74AS182 look-ahead carry generator, provides a ripple-carry function, to help system throughput.

The design includes a 16-word register file, the SN74AS870 (see Figure 4-3). This allows the user to access 16 working areas for temporary data storage or address calculations such as indexing. In this design example, the 'AS888's internal register file is not accessible directly by the user; it is reserved for microcode operations, such as address computation and temporary storage for arithmetic operations. Addressing the register files is permitted through the microprogram or from the macrocode instruction register under microcode control. The transfer register connected to the 'AS888's Y and DB buses allows for feedback into the 'AS888 under microprogram control. Since the constant PROMs and the external register file share the A bus, they cannot be accessed at the same time. The transfer register enables data from the external register file to be transmitted to the B bus, making possible the addition of operands from the constant PROMs and the external register file, for example.

Constant PROMs are also included to simplify the programming and operation of the ALU by supplying fixed data for various operations, such as:

1. Clearing the system register files for initialization. This brings the system up to a known state.
2. Supplying a correction value to the offset in a branch instruction, i.e., converting a 16-bit offset to a true 32-bit address.
3. Table look-up for fixed mathematical operations, such as computing sines and cosines.

Construction of the CCU

Sequencing and branching operations at speeds compatible with the 'AS888 are supplied by the 'AS890, a microprogrammed controller working as a powerful microsequencer. Features of the 'AS890 include:

1. Stack capability. The 9-word stack can be accessed by using a stack pointer or a read pointer; the latter is designed for nondestructive dumping of the stack contents.
2. Register/counter facility. Two registers, DRA and DRB, can be used for latching data from the external data buses or as counters for loops.

A ZERO signal is generated when the decremented counter reaches a zero value.

3. Interrupt control. A register for temporarily holding the return address is supplied; upon entering the interrupt routine, the contents of the return register must be pushed onto the stack for later use.
4. Next address generation. The Y output multiplexer offers a selection of same or incremented address, address from DRA or DRB buses, address from stack, or a concatenation of DRA13-DRA4 and B3-B0.

A microprogram memory/pipeline register supplies the microsequencer and the rest of the system with instructions (see Figure 4-2). The memory might consist of ROMs, or it could be a writable-control store with support logic to allow loading or updating of the control store. For a general purpose machine with a fixed instruction set, ROMs would be more economic.

Some 'AS890 instructions are influenced by the \overline{CC} input. Many are variations of branch and jump instructions. To form and supply \overline{CC} , a register can be used to latch the state of the 'AS888 and supply inputs to a PAL for decoding, based upon the microcode's needs. Combinatorial logic in the PAL allows multiple or single events to be selected or provides a fixed value of '1' or '0' for forced conditions.

To supply the microsequencer with the proper address of the microcode-equivalent version of the macrocode instruction, an instruction register and mapping PROM are needed. Under microprogram control, the instruction register samples the data bus to get the macrocode instruction. The opcode portion is passed to the mapping PROM to form an address to the microcode routine. When the microcode is ready to jump to the routine, it turns off the Y bus output of the 'AS890 and enables the output of the mapping PROM. An optional means of altering the address uses B3-B0 inputs of the 'AS890 to implement an N-way branch routine. In this method, the ten most significant address bits of DRA or DRA are concatenated with the B3-B0 bits to supply an address.

Control information is supplied to the rest of the system via the control register and bus. By setting various bits within the control register, information can be passed to other subsystems, such as memory and I/O peripherals. Bit 0 could represent the read/write control line while bit 1 could select memory or I/O for the read/write. Bit 2 might function to enable interrupts and bit 3 to indicate when the system should enter a "wait" state for slow memory. The remaining control bits can be programmed by the system designer to indicate additional condition states of the "macrosystem".

Addressing of the register files, both 'AS888 internal and 'AS870 external, is done through the use of two 1-of-2 selector banks. The first bank selects address source; this design offers a choice for operand processing of fixed values from the microcode or values from the macroinstruction latched in the instruction register. The second bank selects the first or second operand as an address source for port 0 of the external register file; port 1 uses the third operand

as an address source. It should be noted that the design presented in Figure 4-2 is a one-level pipeline that is instruction-data based. The address and contents of the next instruction are being fetched while the current instruction is being executed. Tracing through the data flow, the following can be observed:

1. The pipeline register contains the current instruction being executed
2. The ALU has just executed its instruction, and has the current status ready at its output pins
3. The status register that is attached to the ALU contains the previous instruction's resulting status
4. The contents of the next microprogram word are being fetched at the same time that the current instruction is being executed.

TRACING THROUGH A 32-BIT COMPUTER

With the 'AS888 and 'AS890 as foundation chips, the typical 32-bit supermini of Figures 4-2 and 4-3 can now be functionally traced. First, note that the data of the main program is handled separately from that of the microcode—each on its own bus. The system is initialized by setting the "clear" signal high—this causes a forced jump to the beginning of the microcode memory. Instructions carried out by the microcode at this point might run system diagnostics, clear all registers throughout the 'AS888-based system, and set up the initial macrocode program address. In this design, the first program address to fetch an instruction from main memory comes from a fixed value in the microcode memory; it is possible to allow the address to be retrieved from a permanent location in main memory or from either a front panel or console, by modifying the microcode program slightly.

Table 4-1 illustrates the microcode format for this design. Note that it contains control signals for all chips involved in the design. Some of these, such as TRANSLATCH and MARLATCH, are used with the system clock to provide controlled loading of the various holding registers. Others supply necessary addressing information, directing input from either the main data bus or from the microcode word itself.

The FETCH routine is shown in functional, assembler and microcoded forms in Tables 4-2, 4-3 and 4-4. First, the program counter is read from the external register file and stored into the memory address register. After the program counter is placed on the address bus, the program counter is updated and stored while the data from memory is allowed to settle down to a stable condition. The data is then latched in both the instruction register and data-in register.

The opcode field of the instruction register is passed through the mapping PROM to convert the opcode to an equivalent microcode routine address. When \overline{YOE} is forced high by the microcode, the 'AS890 is three-stated from the Y bus and the mapping PROM's output is taken out of the three-state mode to supply an address to the control store (microprogram memory); a forced jump is made to the microcode routine to perform the instruction.

Table 4-1. Microcode Definition

MICROCODE FIELD	PIN NAME	INPUT TO	FUNCTION
0-13	DRA13-DRA0	'AS890	Used for next-address branches
14-27	DRB13-DRB0	'AS890	Used for loading counter
28-30	RC2-RC0	'AS890	Register/counter controls
31-33	S2-S0	'AS890	Stack control
34-36	MUX2-MUX0	'AS890	MUX control of Y output bus
37	$\overline{\text{INT}}$	'AS890	Interrupt control
38	$\overline{\text{RAOE}}$	'AS890	Enables DRA output
39	$\overline{\text{RBOE}}$	'AS890	Enables DRB output
40	OSEL	'AS890	Mux control for DRA source
41	INC	'AS890	Incrementer control
42	YOE	'AS890	Enables Y output bus
43-50	I7-I0	'AS888	Instruction inputs
51	$\overline{\text{OEA}}$	'AS888	DA bus enable
52	$\overline{\text{EA}}$	'AS888	ALU input operand select
53	$\overline{\text{OEB}}$	'AS888	DB bus enable
54	OEY	'AS888	Y bus output enable
55	SELY	'AS888	Y bus select
56-57	EB1-EB0	'AS888	ALU input operand selects
58	$\overline{\text{WE}}$	'AS888	Register file write enable
59	$\overline{\text{MAP}}$	PROM	Enables mapping PROM to 'AS890 Y bus
60	$\overline{\text{IR}}$	Latch	Latches data bus to instruction register
61	$\overline{\text{CR}}$	Latch	Latches control data to bus
62-69	CTRL7-CTRL0	Latch	Data for control latch
70-71	BSEL1-BSELO	Multiplexer	Selects data for 'AS890
72-75	B3-B0	Multiplexer	Microcode data to switch
76	$\overline{\text{CONDCD}}$	Latch	Controls latch of 'AS888 status
77-80	SELC3-SELC0	PAL	Selects combination of 'AS888 status
81	$\overline{\text{DTALATCHI}}$	Latch	Controls latching of data-in
82	$\overline{\text{DTAIN}}$	Latch	Enables data-in output to bus
83	$\overline{\text{DTALATCHO}}$	Latch	Controls latching of data-out
84	$\overline{\text{DTAOUT}}$	Latch	Enables data-out output to DB bus
85	$\overline{\text{MARLATCH}}$	Latch	Controls latching of address
86	$\overline{\text{MAR}}$	Latch	Enables MAR output to address bus
87	$\overline{\text{CONSTPROM}}$	PROM	Enables PROM to DA bus
88-99	A11-A0	PROM	Address of constant in PROM
100	SWITCH2	Multiplexer	Selects microcode or Instruction Register data
101	SWITCH1	Multiplexer	Selects microcode or Instruction Register data
102-105	A3-A0	Multiplexer	Register file address ('AS888)
106-109	B3-B0	Multiplexer	Register file address ('AS888)
110-113	C3-C0	Multiplexer	Register file address ('AS888)
114	$\overline{\text{REGUWR}}$	Register File	Port 0 write enable
115	$\overline{\text{REGLWR}}$	Register File	Port 1 write enable
116	$\overline{\text{REGU}}$	Register File	Chip enable on port 0
117	$\overline{\text{REGL}}$	Register File	Chip enable on port 1
118	$\overline{\text{TRANSLATCH}}$	Latch	Controls latch between Y and DB bus
119	$\overline{\text{TRANS}}$	Latch	Enables output to DB bus
120	SELCN2	Multiplexer	Supplies carry input to 'AS888
121	SELCN1	Multiplexer	Supplies carry input to 'AS888
122	REGUB	Multiplexer	Selects address for external register file
123-126	BYTE3 - BYTE0	Three-state	Enables data for byte/bit operations

Table 4-2. Functional Listing of Fetch

FETCH:	MAR = PC, Enable MAR output
	PC = PC + 1
	IR = DIR = data bus, Disable 'AS890 Y bus, Enable mapping PROM to Y bus

Table 4-3. Assembler Listing of Fetch

FETCH: OP890 ...,111,10;INC;	Set 'AS890 for continue
OP888 NOFGROUP5,10,,,1111;	Perform NOP and read external register 15
OEY;SELY;	Enable Y bus output
CR;CTRL 00000011;	Generate external control bus signals
SELC 01;	Select fixed CC value to 'AS890
MARLATCH;MAR;	Latch value on Y bus and enable output
SWITCH 00;REGL;	Select address source and enable port
TRANSLATCH	Latch Y bus for transfer to B bus
OP890 ...,111,10;INC;	Set 'AS890 for continue
OP888 PASS,INCS,00,,,1111;	Increment program counter
OEB;OEY;	Enable Y bus output
SELC 01;	Select fixed CC value to 'AS890
MAR;	Output address to address bus
REGLWR;REGL;	Update program counter in register file
TRANS;	Enable transfer latch output to B bus
SELCN 01	Select carry input to LSP to be "1"
OP890 ...,111,10;	Set 'AS890 for continue
OP888 NOFGROUP5,10;	Perform NOP
MAP;	Enable mapping PROM to 'AS890 Y bus
IR;	Latch data bus to get macrolevel code
SELC 01	Select fixed CC value to 'AS890
DTALATCHI;	Put data bus also in data register
MAR	Output address to address bus

Key to Table 4-3

OP888 a,b,c,d,e,f

where:

- a = upper bits of instruction, 17-14
- b = lower bits of instruction, 13-10
- c = value of EB1-EB0

- d = A address of register files
- e = B address of register files
- f = C address of register files

OP890 v,w,x,y,z

where:

- v = DRA value, 14-bits
- w = DRB value, 14-bits
- x = RC2-RC0
- y = S2-S0
- z = MUX2-MUX0

After the routine is complete, a jump is made back to the FETCH routine by using the next-address supplied by the microprogram. It is up to the system designer/programmer to make sure that all system housekeeping is performed, so that nothing causes a fatal endless loop.

DEFINING THE MACROCODE INSTRUCTION FORMAT

Since this is a 32-bit design, a variety of instruction formats are available. The size of the opcode along with the types of addressing used, will affect both system size and performance. The formats shown in Table 4-5 will be used for discussion.

All Table 4-5 formats have an opcode field of 11 bits and source/destination fields of 7 bits; the first three bits of the latter designate the address type, and the remaining four

bits are used for register access. The opcode length allows 2,048 macrocoded instructions to be mapped to equivalent microcoded routines. The address fields can specify any of the following modes: register, relative, autoincrement/autodecrement, indexed, absolute, and deferred. The offset used in the Type 0 instruction can be used for branch-based instructions, for an offset range of ± 32727 .

TRACING A MACROCODE INSTRUCTION

Microcode for a Type 3 multiplication instruction is shown in Table 4-6, using the following assumptions:

1. Code for retrieving the operands will not be shown. Jumps will be made to routines that will place the temporary operands into internal register locations 2 and 3 of the 'AS888, after being fetched from main memory.

Table 4-4. Microcode Listing of Fetch

DRA13- DRA0	DRB13- DRB0	RC2-RC0	S2-S0	MUX2-MUX0	INT RAOE RBOE RDEL RVE	17-10	OEA EA OEB EB SELV EB1 EB0 WE	MAP IR CR
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0	1 1 1	0 1 0	1 1 1 0 1 0	1 1 1 1 1 1 1 1	1 1 1 0 1 1 0 1	1 1 1 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0	1 1 1	0 1 0	1 1 1 0 1 0	1 1 1 1 0 1 0 0	1 1 1 0 0 0 0 1	1 1 1 1
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0	1 1 1	0 1 0	1 1 1 0 0 1	1 1 1 1 1 1 1 1	0 1 1 1 1 1 0 1	0 0 1

Table 4-4. Microcode Listing of Fetch (Continued)

CTRL7- CTRL0	BSEL1-BSEL0	B3-B0	CONDCO	SEL3-SELCO	DTALATCH DTAIN DTALATCHO DTALATCHI MABLATCH MAR CONSTPRROM	A11-A0	SWITCH2-SWITCH1	A3-A0	B3-B0	C3-C0	REGUWR REGUWR REGU REGU TRANS LATCH SELN2 SELN1 REGUB	BYTES-BYTE0
0 0 0 0 0 0 1 1	0 0	0 0 0 0	1	0 0 0 1	1 1 1 1 1 0 0 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0	0 0 0 0	0 0 0 0	1 1 1 1	1 1 1 0 0 1 0 0 0	1 1 1 1
0 0 0 0 0 0 0 0	0 0	0 0 0 0	1	0 0 0 1	1 1 1 1 1 1 0 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0	0 0 0 0	0 0 0 0	1 1 1 1	1 0 1 0 1 0 0 1 0	1 1 1 1
0 0 0 0 0 0 0 0	0 0	0 0 0 0	1	0 0 0 1	0 1 1 1 1 0 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 1 1 1 1 1 0 0 0	1 1 1 1

Table 4-5. Possible Instruction Formats

TYPE 0 — OPCODE + 16-BIT OFFSET

0 — 10 Opcode	11 — 15 Not Used	16 — 31 Offset
------------------	---------------------	-------------------

TYPE 1 — OPCODE + DESTINATION

0 — 10 Opcode	11 — 24 Not used	25 — 31 Destination
------------------	---------------------	------------------------

TYPE 2 — OPCODE + SOURCE + DESTINATION

0 — 10 Opcode	11 — 17 Not used	18 — 24 Source	25 — 31 Destination
------------------	---------------------	-------------------	------------------------

TYPE 3 — OPCODE + SOURCE1 + SOURCE2 + DESTINATION

0 — 10 Opcode	11 — 17 Source	18 — 24 Source	25 — 31 Destination
------------------	-------------------	-------------------	------------------------

Table 4-6. Functional Listing of Multiply

UMUL3:

- JUMPSUB SOURCE1 Get first operand
- JUMPSUB SOURCE2, Get second operand
- BCOUNT = 32 Load DB counter register
- REG 9 = 0 Clear temporary accumulator
- MQ = REG 2 Load multiplier

LOOP:

- UMULI WITH REG 3 Issue the multiply
- DECREMENT BCOUNT, Decrement the DB counter
- BRANCH TO LOOP IF NOT ZERO, Loop back until done
- LATCH 'AS888 STATUS, Store 'AS888 flags
- REG 9 = ALU Store intermediate result
- REG 8 = MQ Store intermediate result
- JUMPSUB STORPSW Update macro program status
- JUMPSUB MDEST Store result at destination
- JUMP FETCH Get next instruction

Table 4-7. Assembler Code of Multiply

UMULI3:	
OP890 SOURCE1,,,110,110;	Perform a subroutine branch
INC;YOE;	Increment address and enable Y bus
OP888 NOP;GROUP5;	Tell 'AS888 to do nothing during jump
SELC 0001;	Set CC to "1" to set up 'AS890 continue
MAR	Maintain address on main address buss
OP890 SOURCE2,00000000100000,110,110,110;	Perform subroutine branch and load B counter
INC;YOE;	Increment microaddress and enable Y bus
OP888 NOP;GROUP5;	Tell 'AS888 to do nothing during jump
SELC 0001;	Set CC to "1" to set up 'AS890 continue
MAR	Maintain address on main address bus
OP890 ,, ,111,110;	Perform a continue instruction
INC;YOE;	Increment microaddress and enable Y bus
OP888 CLEAR,GROUP5,,,,1001;	Zero out register file accumulator
WE;	Enable writing to register file
SELC 0001;	Set CC to "1" to set up 'AS890 continue
MAR	Maintain address on main address buss
OP890 LOOP,,,111,110;	Perform a continue instruction
INC;YOE;	Increment microaddress and enable Y bus
OP888 LOADMQ,INCS,,,0010;	Load MQ register with S + Cn, from external register file
MAR	Maintain address on main address bus
LOOP:	
OP890 LOOP,,101,111,100;	Decrement B and loop til ZERO = 1
INC;YOE;	Increment microaddress and enable Y bus
OP888 UMULI,GROUP4,01,0011,,1001;	Perform unsigned multiply on accumulator
WE;	Update register file accumulator
MAR	Maintain address on main address bus
OP890 ,, ,111,110;	Perform a continue instruction
INC;YOE;	Increment microaddress and enable Y bus
OP888 PASS,INCS,,,,1000;	Put S + Cn in temporary register file
WE;	Allow updating of register file
MAR	Maintain address on main address bus
OP890 STORPSW,,,110,110;	Perform a subroutine branch
INC;YOE;	Increment microaddress and enable Y bus
OP888 NOP;GROUP5;	Tell 'AS888 to do nothing during jump
SELC 0001;	Set CC to "1" for set up 'AS890 continue
MAR	Maintain address on main address bus
OP890 FETCH,,,111;	Perform a branch to FETCH routine
INC;YOE;	Increment microaddress and enable Y bus
OP888 NOP;GROUP5;	Tell 'AS888 to do nothing during jump
SELC 0001	Set CC to "1" for 'AS890 continue

Key to Table 4-7.

OP888 a,b,c,d,e,f

where:

- a = upper bits of instruction, 17-14
- b = lower bits of instruction, 13-10
- c = value of EB1-EB0
- d = A address of register files
- e = B address of register files
- f = C address of register files

OP890 v,w,x,y,z

where:

- v = DRA value, 14-bits
- w = DRB value, 14-bits
- x = RC2-RC0
- y = S2-S0
- z = MUX2-MUX0

Table 4-8. Microcode Listing of Multiply

DRA13- DRA0	DRB13- DRB0	RC2-RC0	S2-S0	MUX2-MUX0	INT RAOE RBOE ROSEL INC YOE	17-10	OEA EA OEB EBY OEL ELB ERL ERB WE	MAP IR CR
0 0 0 0 0 0 0 0 0 0 0 1 1 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0	1 1 0	1 1 0	1 1 1 0 1 0	1 1 1 1 1 1 1 1	1 1 1 1 0 0 0 1	1 1 1
0 0 0 0 0 0 0 0 0 1 0 0 0 0	0 0 0 0 0 0 0 0 0 1 0 0 0 0 0	1 1 0	1 1 0	1 1 0	1 1 1 0 1 0	1 1 1 1 1 1 1 1	1 1 1 1 0 0 0 1	1 1 1
0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0	1 1 1	1 1 0	1 1 1 0 1 0	1 1 1 1 0 0 0 0	1 1 1 0 0 0 0 0	1 1 1
0 0 0 0 1 0 0 0 0 0 1 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0	1 1 1	1 1 0	1 1 1 0 1 0	1 1 1 0 0 1 0 0	1 1 1 0 0 0 0 1	1 1 1
0 0 0 0 1 0 0 0 0 0 1 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 0 1	1 1 1	1 0 0	1 1 1 0 1 0	1 1 1 0 1 0 0 0	1 1 1 0 0 0 0 1 0	1 1 1
0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0	1 1 1	1 0 1	1 1 1 0 1 0	1 1 1 1 1 1 1 1	1 1 1 0 0 0 0 1 0	1 1 1
0 0 0 0 0 0 0 0 0 1 0 1 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0	1 1 0	1 1 0	1 1 1 0 1 0	1 1 1 1 1 1 1 1	1 1 1 1 0 0 0 1	1 1 1
0 0 0 0 0 0 0 0 0 1 1 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0	1 1 0	1 1 0	1 1 1 0 1 0	1 1 1 1 1 1 1 1	1 1 1 1 0 0 0 1	1 1 1
0 0 0 0 0 0 0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0	1 1 1	0 0 0	1 1 1 0 1 0	1 1 1 1 1 1 1 1	1 1 1 1 0 0 0 1	1 1 1

Table 4-8. Microcode Listing of Multiply (Continued)

CTRL7- CTRL0	BSEL1-BSELO	B3-B0	CONDCO	SEL3-SELCO	D1ALATCHI D1AIN D1ALATCHO D1AOUT D1ALATCH MAR CONSTPRROM	A11-A0	SWITCH2-SWITCH1	A3-A0	B3-B0	C3-C0	REGUWR REGLWR REGU REGL TRANSLATCH TRANS SELN2 SELN1 REGUB	BYTE3-BYTE0
0 0 0 0 0 0 0 0	0 0	0 0 0 0	1	0 0 0 1	1 1 1 1 1 0 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 1 1 1 1 1 0 0 0	1 1 1 1
0 0 0 0 0 0 0 0	0 0	0 0 0 0	1	0 0 0 1	1 1 1 1 1 0 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 1 1 1 1 1 0 0 0	1 1 1 1
0 0 0 0 0 0 0 0	0 0	0 0 0 0	1	0 0 0 1	1 1 1 1 1 0 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0	0 0 0 0	0 0 0 0	1 0 0 1	1 1 1 1 1 0 0 0	1 1 1 1
0 0 0 0 0 0 0 0	0 0	0 0 0 0	0	0 0 0 1	1 1 1 1 1 0 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0	0 0 1 0	0 0 0 0	1 1 0 1	1 1 1 0 0 0 0	1 1 1 1
0 0 0 0 0 0 0 0	0 0	0 0 0 0	0	0 0 0 1	1 1 1 1 1 0 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0	0 0 1 1	0 0 0 0	1 0 0 1	1 0 1 0 1 1 0 0 0	1 1 1 1
0 0 0 0 0 0 0 0	0 0	0 0 0 0	0	0 0 0 1	1 1 1 1 1 0 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0	0 0 0 0	0 0 0 0	1 0 0 0	1 0 1 0 1 1 0 0 0	1 1 1 1
0 0 0 0 0 0 0 0	0 0	0 0 0 0	0	0 0 0 1	1 1 1 1 1 0 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 1 1 1 1 0 0 0	1 1 1 1
0 0 0 0 0 0 0 0	0 0	0 0 0 0	1	0 0 0 1	1 1 1 1 1 0 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 1 1 1 1 1 0 0 0	1 1 1 1
0 0 0 0 0 0 0 0	0 0	0 0 0 0	1	0 0 0 1	1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 1 1 1 1 1 0 0 0	1 1 1 1

2. A jump to a routine to store the product in the destination will be handled similarly.
3. Multiplication will be unsigned; the result will be placed in two temporary locations of the 'AS888.
4. An update to the program status word, which the user can access at the macrocode level, must also be performed but is not shown.

Assembler code is shown in Table 4-7; a microcode listing is given in Table 4-8. The first two lines of microcode are subroutine jumps to opcode fetching routines, which store the operands in register files 2 and 3 in the 'AS888. The next two instructions load up the 'AS890 with a counter constant for the multiply loop, load the MQ register of the 'AS888 with the multiplier and clear the register that is temporarily used for the accumulator.

A loop is then entered to perform the multiply instruction 32 times to form the product, with the multiplicand coming from the internal register file of the 'AS888. Upon exiting the loop, the MQ register is stored

in a temporary register location in the 'AS888. The MQ register now contains the least significant bits of the result and the temporary accumulator the most significant bits. A subroutine jump is made to the program status word update routine; this will take the status flags of the last multiplication iteration and change the macrolevel status word. The next subroutine jump is to a destination routine, which is followed by a branch to the FETCH routine to get the next macroinstruction to be executed.

SYSTEM ENHANCEMENTS

The above example provides a broad overview of 32-bit system design using the 'AS888 and 'AS890. Certain additional options may enhance system performance. These include:

1. Status latching. The design does not take into account changes that need to be examined at the microlevel while retaining macrolevel status information. One solution would be to include another register in parallel to the status latch

and provide control to choose between the two to form the condition code value.

2. Interrupts. To efficiently use a computer system, interrupts are used to alter program flow in the case of I/O programming and real-time applications (involving hardware timers). To include this capability, external hardware must be included and the microcode modified accordingly.
3. Control store. One way of implementing microprogram memory is to use a ROM-based design. It is becoming more common to design a writable control store, a completely RAM-based or part RAM, part ROM storage system, that can be altered by system operation, such as initialization from a floppy disk subsystem, or by the user to optimize or implement new macrolevel instructions. The cost of implementation must be weighed with the risks involved in changing instructions which may not be supported by other sites.
4. Instruction word definitions. Changing the instruction word definitions will have an effect on both system design and performance. Removing Type 3 instructions from the design, for example, will have an effect on both

hardware and software: the external register file addressing must be changed and the 1-of-2 selector removed. Likewise, changing the opcode length may restrict the instruction address capability and also cause either an increase or decrease in the microcode size.

5. Dynamic memory access (DMA). The above system does not support dynamic memory access. To include this function requires a change in the address output control, along with support circuitry for the type of DMA selected. Some error detection and correction logic for main memory might also be included.
6. Computer control unit. The design presented here shows a one-level pipeline architecture that is instruction-data based. System throughput may be increased by converting to a pipeline of greater depth, or using another variety of one-level pipeline, such as instruction-address based or address-data based. Care must be taken when increasing the size of the pipeline, especially when handling branch/jump situations. The reader is advised to carefully research this area before implementing any design.

Table 4-9. Critical Delay Path Analysis

CONTROL LOOP			DATA LOOP		
COMPONENT	DATA PATH	TIME (NS)	COMPONENT	DATA PATH	TIME (NS)
Pipeline register	Clock to output	9	'AS888-1	Clock to C_n	46
MUX	Select to output	13	'AS182	C_n to C_{n+z}	5
'AS890-1	\overline{CC} to output	25	'AS888-1	C_n to \overline{SIO}	25
PROM	Access time	20	'AS888-1	\overline{SIO} to Y	14
Pipeline register	Setup time	2			
		69			90

Table 4-10. Fetch Timing Comparison

FETCH	'AS888 32-BIT	Z8001	8086-1	80286	68000L
Data width	32	16	16	16	16
No. of cycles	4	3	4	4	4
Clock rate	11.11 MHz	4 MHz	10 MHz	10 MHz	8 MHz
Total time	360 ns	750 ns	400 ns	400 ns	600 ns

Table 4-11. Multiply Timing Comparison

MULTIPLY	'AS888 32-BIT	'AS888 16-BIT	Z8001	8086-1	80286	68000L
Size	32×32	16×16	16×16	16×16	16×16	16×16
No. of cycles	35	19	70	128	21	≤ 74
Clock rate	11.11 MHz	10.98 MHz	4 MHz	10 MHz	10 MHz	8 MHz
Total time	3.150 μ s	1.729 μ s	17.5 μ s	12.8 μ s	2.1 μ s	$\leq 9.25 \mu$ s

TIMING AND SYSTEM THROUGHPUT

A critical path analysis was undertaken to determine the maximum clock rate for the proposed system. The longest delay path is the multiplication data path, which involves the internal register file and the shift function of the 'AS888. Table 4-9 contains the critical delay calculations for both the ALU and CCU. Since both portions of the system must be satisfied, a clock rate of 90 ns was selected for the following comparisons.

FETCH ANALYSIS

Most microprocessors perform an instruction fetch in a pipeline mode; the next instruction is fetched while the current instruction is executing. The fetch code shown earlier requires a minimum of four cycles: three to issue the code and one to break the pipeline for processing the batch. This results in a total time of 360 ns, based on a 90 ns cycle time. Fetch times for the representative microprocessors have been estimated from data books and are shown in Table 4-10; wait states for slow memory are not included. As can be seen from the table, the 'AS888 design example is estimated to run from 1.1 to 2.1 times faster than the 16-bit microprocessors.

MULTIPLICATION ANALYSIS

This analysis assumes that multiplication is unsigned integer and register to register based. No account is taken of time needed for instruction fetch or operand fetch or store.

The basic loop for the multiply takes 35 cycles: 2 for accumulator and multiplier setup, 32 for actual multiply loop and 1 to store the least significant bits in an internal register file. Given a cycle time of 90 ns, a 32 by 32 bit multiplication can be implemented in 2.275 microseconds. A 16-bit multiply requires 16 iterations of the inner loop; both timings are included in Table 4-11 for comparison. Values for the 16-bit multiplies of the representative microprocessors have been estimated from data books.

As shown in Table 4-11, the 16 by 16 multiply can be performed with the 'AS888 at a faster rate than the 16-bit microprocessors. Even comparing the 32 by 32 multiply of the application design, one can see that the 'AS888 based system has a better macroinstruction execution speed. Using the 'AS888 and 'AS890 in a system design will allow high throughput and a flexible architecture.

3

Application Reports

Section 5

An Adaptive Clock Generator To Increase 'AS888 System Speed

'AS888-1 instructions execute within 50 to 90 ns; over half execute in less than 60 ns. It is therefore possible to enhance the speed of an 'AS888 system using an adaptive clock generator that spaces clock pulses according to the time required to complete each operation. The advantage of using this circuit is that the system can process each instruction in almost exactly the time it takes the desired results to reach steady-state. The alternative is to use a periodic 90 ns clock and waste use of 'AS888 "idle time." Just how fast the system will run with the adaptive clock is a function of the statistical distribution of microinstructions within any given microprogram.

The time required for an 'AS888 instruction depends on whether shift, carry, register file read, ZERO status test and/or N status test are used. These operations require varying lengths of time to execute, depending on the number of 'AS888 internal delays involved. Whether shift and/or carry are used is determined by the 'AS888 instruction field. ALU source operands can originate from the register file or the DA and DB buses; this is determined by the state of the EA and EB1-EB0 inputs. Whether or not ZERO or N status are tested depends on other system signals, such as a status select field in the microinstruction to select ALU status during conditional branching. Depending on the system architecture, the pipelining scheme used and the flexibility of the microprogram, the designer may wish to ensure that test ZERO and test N signals be made available during the cycle in which ZERO or N are generated in order to better match clock pulse spacing to processing delay. By also providing a register file read signal, the clock spacing will be optimally matched to the processing delay.

CIRCUIT DESCRIPTION

A diagram of the adaptive clock circuit is given in Figure 5-1. The circuit consists of a PROM decoder and a programmable oscillator. The PROM contains a table of cycle length codes as a function of the 'AS888 instruction field, register file read (RFRD), ZERO test (ZTST) and N test (NTST). These signals are connected to the PROM address inputs from the control store outputs as shown. If the RFRD, ZTST and NTST signals are not available, these inputs can be tied high, or a smaller PROM can be used.

The cycle length codes residing in PROM are used to select one of nine delays in the programmable delay line oscillator. The selected delay provides the phase shift required for oscillation. Two programmable delay lines (Data Delay Devices PDU-1613-5) are needed; they must be alternately switched into the feedback loop so that each has

time to empty. The programmable delay lines establish the timing from leading edge to leading edge of the clock for an overall error of only ± 3.5 ns. The delays for various fixed-length delay lines are indicated by the numbers in the numbered boxes in Figure 5-1.

Timing for this circuit is shown in Figure 5-2. RST initializes the circuit. When RST releases, the open collector output of U4a provides an initial rising edge from which all successive rising edges are regenerated. Toggle flip-flop U3a switches between the two halves of the oscillator. Latches U6a and U6b are alternately enabled by the Q and \overline{Q} outputs of U3b. In this manner only one delay line at a time is selected to receive a pulse. U3a generates $\overline{OE1}$ and $\overline{OE2}$ which select the available delay line for output. The pulse width regulation is also initiated by U3a. TQ and \overline{TQ} serve as references for edge detectors U5a-U5d. The fixed delay lines shape $\overline{OC1}$, CLR1, $\overline{OC2}$, and CLR2. The output control $\overline{OC1}$ (or $\overline{OC2}$) on U6a (or U6b) turns off several nanoseconds after a rising transition in TQ (or \overline{TQ}) has occurred thereby holding Q1 (or Q2) high. This stretches the on-time of the pulse to nearly 50 ns. U6a (or U6b) is cleared 10 ns later. After another 10 ns the output control turns on again, allowing the Q which was just cleared to establish the falling edge of the stretched pulse. This stretched pulse then enters the selected delay line, U7 (or U8), exiting at a time established by the cycle length code. The delay line output enable, OE1 (or OE2) switches in the delay line before its pulse is ready to exit. In this manner, the width of the previous pulse is regulated to within 20 to 30 ns.

PROM PROGRAM

The cycle lengths are defined by analyzing the propagation delays from the 'AS888 data sheet given in Table 5-1. Variations in cycle lengths depend on whether shift, carry, register file read, ZERO test or N test are used. The algorithm for determining cycle length is flowcharted in Figures 5-3—5-6. Total cycle length is found by adding up all the contributing delays for each possible case. Sums less than 50 ns must be adjusted to 50 ns since this is the minimum clock cycle length specified in the data sheet. Seven nanoseconds is used as the propagation time for $\overline{G/P}$ to Cn; this assumes an 'AS182 lookahead carry generator is used with the 'AS888. Each total delay is rounded up to the nearest integer multiple of 5 ns, which gives nine possible outcomes.

Use of the shifters or carry is inherent in each instruction as shown in Table 5-2. Cycle length codes can be generated by looking up Table 5-2 for each instruction, performing the algorithm in Figures 5-3—5-6, and encoding

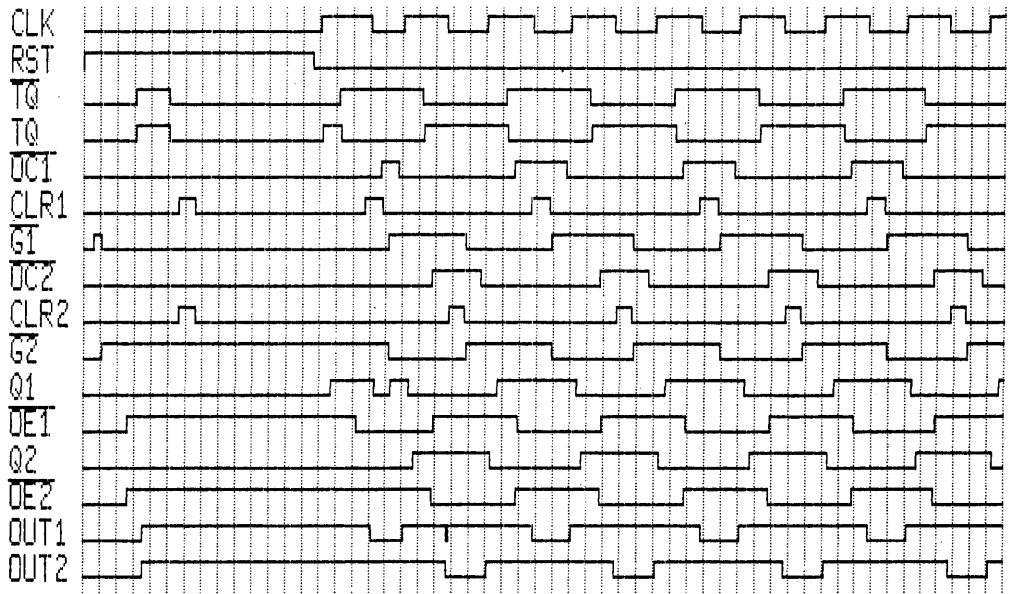


Figure 5-2. Adaptive Clock Generator Timing Diagram

Table 5-1. 'AS888-1 Timing Characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)										UNIT
		Y	C _n + 8	G, P	Z*	N	OVR	DA	DB	QIO	SIO	
t _{pd}	A3-A0, B3-B0	44	30	36	50	44	44	17	17	48	48	ns
	DA7-DA0, DB7-DB0	36	24	24	46	41	32	—	—	40	40	
	C _n	22	8	—	27	21	16	—	—	25	25	
	EA	40	25	25	49	41	41	—	—	44	44	
	EB	40	25	25	49	41	41	—	—	44	44	
	I7-I0	46	27	27	50	42	35	—	—	45	45	
	OE _B	—	—	—	—	—	—	—	12	—	—	
	OE _Y	12	—	—	—	—	—	—	—	—	—	
	QIO (n) Shift	14	—	—	20	—	—	—	—	—	—	
	SIO (n) Shift	14	—	—	20	18	—	—	—	—	—	
	CK	50	46	46	50	50	50	30	30	50	50	
	OE _A	—	—	—	—	—	—	12	—	—	—	
	SSF**	—	—	—	—	—	9	—	—	—	—	

*Load resistor R1 = 100

**For byte instructions only.

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of *The TTL Data Book*, Volume 3, 1984.

each of the nine possible time delays with a number from 0 to 8. A BASIC program which follows this procedure and generates the PROM data in Data I/O hex-ASCII format is shown in Program 5-1. Program lines 147-149 look up carry and shift for each instruction. Once carry and shift are known, the program solves the total delay algorithm in Figures

5-3—5-6 for all cases of ZTST, NTST, and RFRD as shown in program lines 163-184. At this point the actual time to process the microinstruction for the given conditions is solved. The time values are then encoded from 0 to 8 in program lines 188-195. The output is listed in Figure 5-7.

Table 5-2. Shift and Carry as a Function of I7-I0

GROUP 1 INSTRUCTIONS			
INSTRUCTION BITS (I3-I0) HEX CODE	MNEMONIC	CARRY	SHIFT
0			
1	ADD	/	
2	SUBR	/	
3	SUBS	/	
4	INCS	/	
5	INCNS	/	
6	INCR	/	
7	INCNR	/	
8			
9	XOR		
A	AND		
B	OR		
C	NAND		
D	NOR		
E	ANDNR		
F			
GROUP 2 INSTRUCTIONS			
INSTRUCTION BITS (I7-I4) HEX CODE	MNEMONIC	CARRY	SHIFT
0	SRA		/
1	SRAD		/
2	SRL		/
3	SRLD		/
4	SLA		/
5	SLAD		/
6	SLC		/
7	SLCD		/
8	SRC		/
9	SRCD		/
A	MQSRA		/
B	MQSRL		/
C	MQSLL		/
D	MQSLC		/
E	LOADMQ		/
F	PASS		

Table 5-2. Shift and Carry as a Function of I7-10 (Continued)

GROUP 3 INSTRUCTIONS			
INSTRUCTION BITS (I7-10) HEX CODE	MNEMONIC	CARRY	SHIFT
08	SET1	✓	
18	SET0		
28	TB1		
38	TB0		
48	ABS	✓	
58	SMTC	✓	
68	ADDI	✓	
78	SUBI	✓	
88	BADD	✓	
98	BSUBS	✓	
A8	BSUBR	✓	
B8	BINCS	✓	
C8	BINCNS	✓	
D8	BXOR		
E8	BAND		
F8	BOR		
GROUP 4 INSTRUCTIONS			
00	CRC		✓
10	SEL	✓	
20	SNORM	✓	✓
30	DNORM		✓
40	DIVRF	✓	
50	SDIVQF	✓	
60	SMULI	✓	✓
70	SMULT	✓	✓
80	SDIVIN		✓
90	SDIVIS	✓	✓
A0	SDIVI	✓	✓
B0	UDIVIS	✓	✓
C0	UDIVI	✓	✓
D0	UMULI	✓	✓
E0	SDIVIT	✓	✓
F0	UDIVIT	✓	✓
GROUP 5 INSTRUCTIONS			
0F	CLR		
1F	CLR		
2F	CLR		
3F	CLR		
4F	CLR		
5F	CLR		
6F	CLR		
7F	BCDBIN	✓	✓
8F	EX3BC	✓	
9F	EX3C	✓	
AF	SDIVO	✓	
BF	CLR		
CF	CLR		
DF	BINEX3	✓	✓
EF	CLR		
FF	NOP		



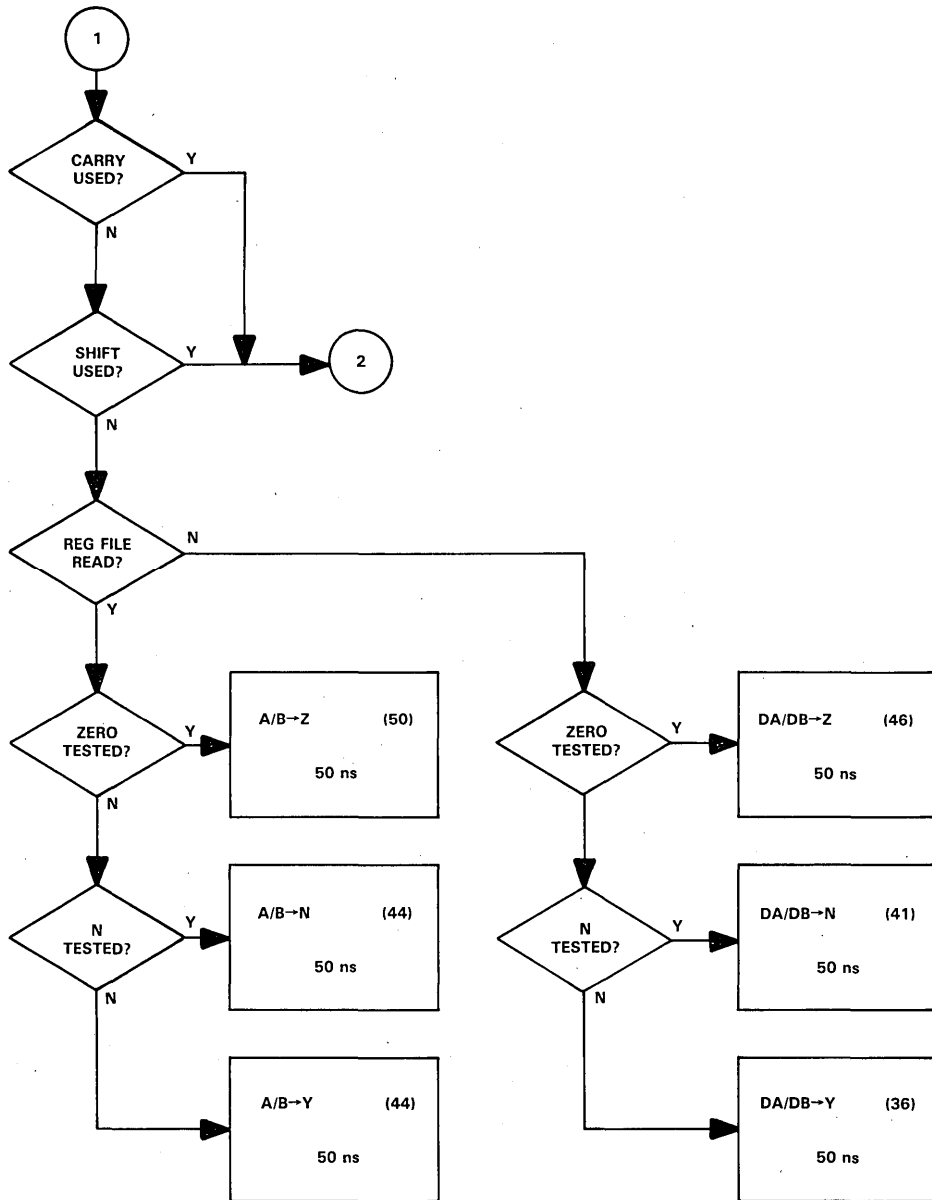


Figure 5-3. Propagation Delay Without Carry and Without Shift

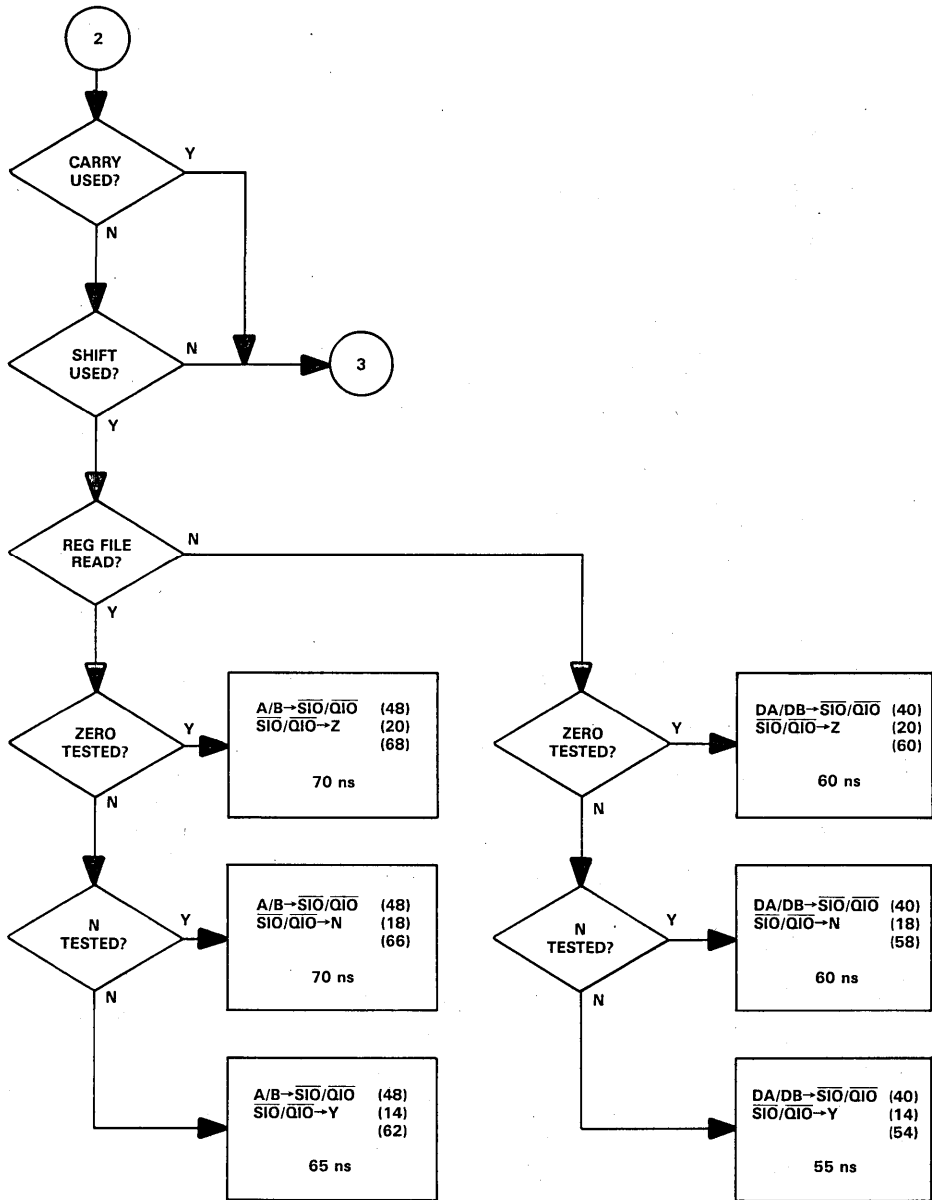


Figure 5-4. Propagation Delay Without Carry and With Shift

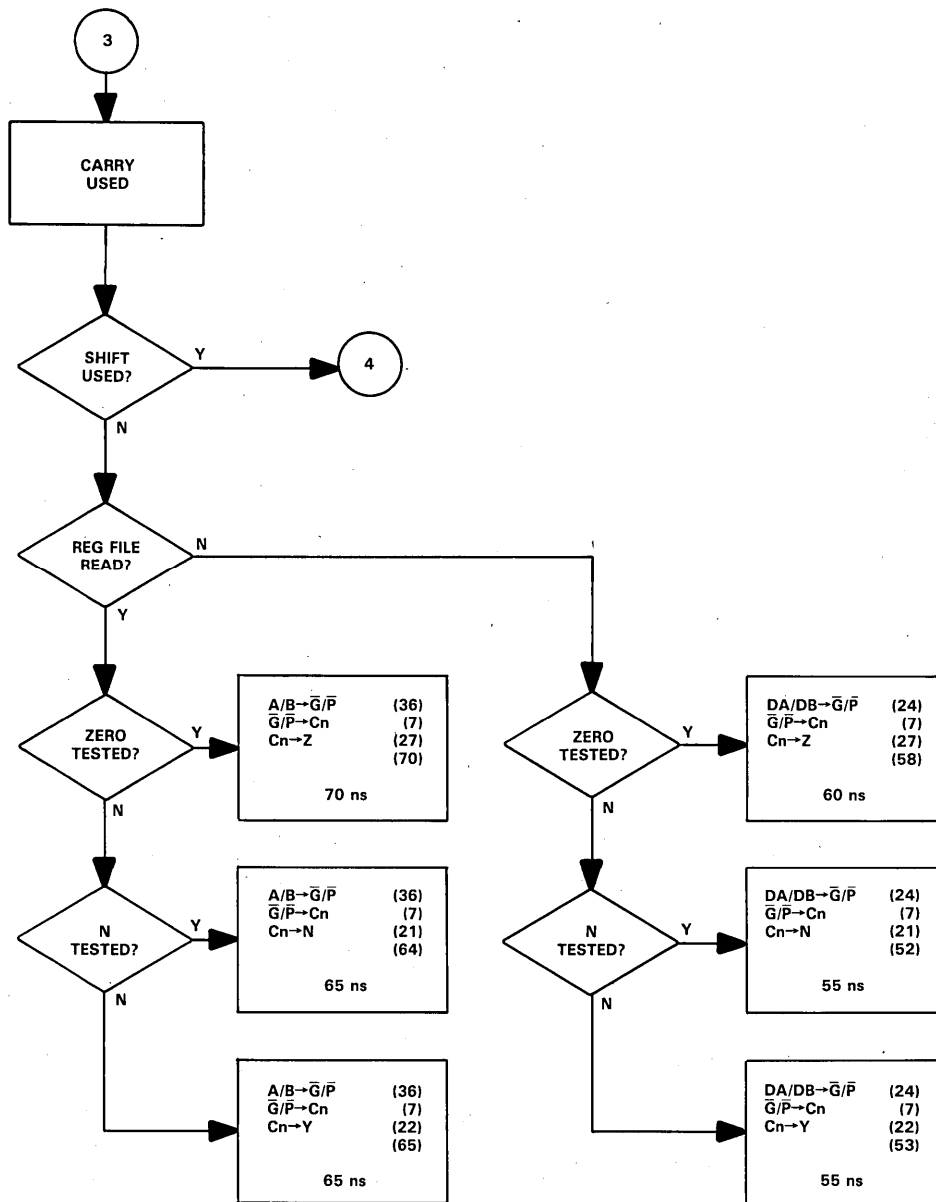


Figure 5-5. Propagation Delay With Carry and Without Shift

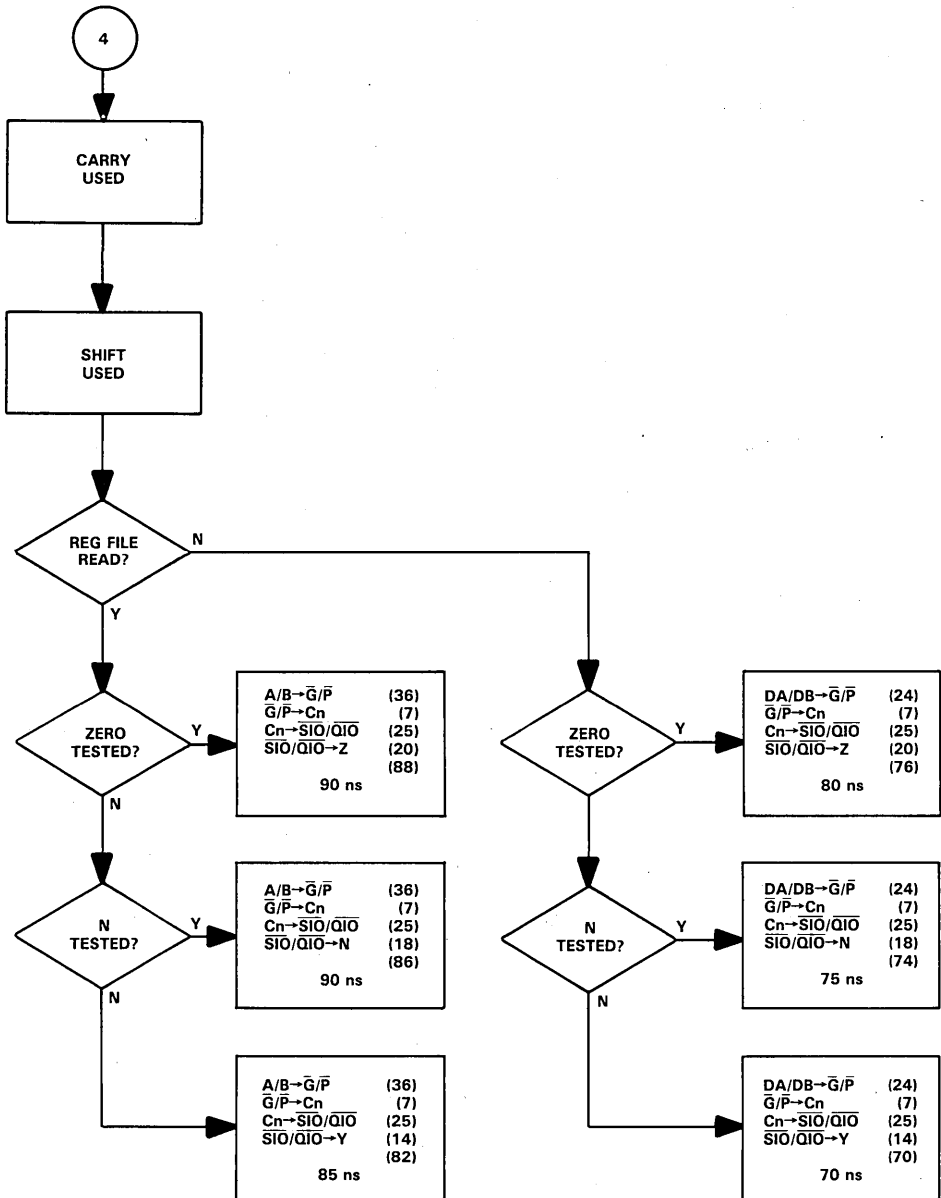


Figure 5-6. Propagation Delay With Carry and With Shift

```

100 *****
101 CLS
102 PRINT " 'AS888-1 ADAPTIVE CLOCK GENERATOR "
103 PRINT " PROM DATA GENERATION PROGRAM "
104 PRINT " MAY 24, 1985 "
105 *****
106
107
108 DEFINT A-Z
109 DIM TABLE(4096)
110
111 ' DEFINE TRANSMISSION CONTROL CHARACTERS
112
113 STX$=CHR$(2)
114 ETX$=CHR$(3)
115 CR$=CHR$(13)+CHR$(10)
116 TX$=STX$
117 BS$=CHR$(8)
118
119 ' INPUT USER'S PROM DATA FILE NAME AND OPEN THE FILE
120
121 PRINT:INPUT "PROM DATA OUTPUT FILE NAME";OF$: PRINT
122 OPEN "O",#1,OF$: PRINT "WRITING CYCLE LENGTH CODES TO ";OF$;"..." : PRINT
123
124 ' SET UP DATA I/O PROGRAMMER FOR HEX-ASCII (COMMA) FORMAT
125
126 PRINT #1,"53A"
127
128 ' FOR EACH 'AS888 INSTRUCTION (BITS I7-I0), DETERMINE IF
129 ' SHIFT AND/OR CARRY ARE USED
130
131 FOR I7I4 = 0 TO 15
132 FOR I3I0 = 0 TO 15
133
134 ' DEFINE THE 8-BIT INSTRUCTION FIELD AND IDENTIFY WHICH GROUP(S)
135 ' THE INSTRUCTION BELONGS TO
136
137 I7I0 = I7I4 * 16 + I3I0
138 GROUP1 = (I3I0<>0) AND (I3I0<>8) AND (I3I0<>15)
139 GROUP2 = GROUP1
140 GROUP3 = (I3I0 = 8)
141 GROUP4 = (I3I0 = 0)
142 GROUP5 = (I3I0 = 15)
143
144
145 ' DETERMINE WHETHER THE INSTRUCTION USES SHIFT AND/OR CARRY
146
147 CARRY = (GROUP1 AND (I7I4<8))
OR (GROUP3 AND (I7I4<3) AND (I7I4<13))
OR (GROUP4 AND (I7I4<>0) AND (I7I4<>3) AND (I7I4<>8))
OR (GROUP5 AND ((I7I4>7) AND (I7I4<11) OR (I7I4 = 13)))
148
149 SHIFT = (GROUP2 AND (I7I4<14))
OR (GROUP4 AND (I7I4<>1) AND (I7I4<>4) AND (I7I4<>5))
OR (GROUP5 AND ((I7I4=7) OR (I7I4 = 13)))
150
151
152 ' GIVEN WHETHER SHIFT AND/OR CARRY ARE USED, FIND THE WORST CASE DELAY
153 ' (IN INCREMENTS OF 5 NS) IF REGISTER FILE READ, ZERO TEST AND/OR N TEST
154 ' ALSO OCCUR
155
156 FOR RF = 0 TO -1 STEP -1
157 FOR Z = 0 TO -1 STEP -1
158 FOR N = 0 TO -1 STEP -1
159
160 ' SOLVE PROPAGATION DELAY USING 'AS888 DATA SHEET; ROUND UP TO NEAREST
161 ' 5 NS INCREMENT
162
163 IF NOT CARRY AND NOT SHIFT THEN TIME = 50
164
165 IF NOT CARRY AND SHIFT AND NOT RF AND Z THEN TIME = 60
166 IF NOT CARRY AND SHIFT AND NOT RF AND NOT Z AND N THEN TIME = 60

```

Program 5-1. BASIC Program to Generate PROM Data

```

167 IF NOT CARRY AND SHIFT AND NOT RF AND NOT Z AND NOT N THEN TIME = 55
168 IF NOT CARRY AND SHIFT AND RF AND Z THEN TIME = 70
169 IF NOT CARRY AND SHIFT AND RF AND NOT Z AND N THEN TIME = 70
170 IF NOT CARRY AND SHIFT AND RF AND NOT Z AND NOT N THEN TIME = 65
171
172 IF CARRY AND NOT SHIFT AND RF AND Z THEN TIME = 60
173 IF CARRY AND NOT SHIFT AND RF AND NOT Z AND N THEN TIME = 55
174 IF CARRY AND NOT SHIFT AND RF AND NOT Z AND NOT N THEN TIME = 55
175 IF CARRY AND NOT SHIFT AND NOT RF AND Z THEN TIME = 70
176 IF CARRY AND NOT SHIFT AND NOT RF AND NOT Z AND N THEN TIME = 65
177 IF CARRY AND NOT SHIFT AND NOT RF AND NOT Z AND NOT N THEN TIME = 65
178
179 IF CARRY AND SHIFT AND RF AND Z THEN TIME = 80
180 IF CARRY AND SHIFT AND RF AND NOT Z AND N THEN TIME = 75
181 IF CARRY AND SHIFT AND RF AND NOT Z AND NOT N THEN TIME = 70
182 IF CARRY AND SHIFT AND NOT RF AND Z THEN TIME = 90
183 IF CARRY AND SHIFT AND NOT RF AND NOT Z AND N THEN TIME = 90
184 IF CARRY AND SHIFT AND NOT RF AND NOT Z AND NOT N THEN TIME = 85
185
186 ' ENCODE THE TIME DELAYS AS FOLLOWS
187
188 IF TIME = 50 THEN CODE = 0
189 IF TIME = 55 THEN CODE = 1
190 IF TIME = 60 THEN CODE = 2
191 IF TIME = 65 THEN CODE = 3
192 IF TIME = 70 THEN CODE = 4
193 IF TIME = 75 THEN CODE = 5
194 IF TIME = 80 THEN CODE = 6
195 IF TIME = 85 THEN CODE = 7
196 IF TIME = 90 THEN CODE = 8
197
198 ' WRITE THE SELECT CODE TO THE OUTPUT FILE
199 ' IN DATA I/O HEX ASCII (COMMA) FORMAT
200
201 IF ADDR=4095 THEN TX$=ETX$
202 IF ADDR/16=INT(ADDR/16) THEN PRINT #1,TX$;"$A";RIGHT$("000"+HEX$(ADDR),4);"
"; ELSE PRINT #1,"";
203 PRINT #1,"0";RIGHT$(STR$(CODE),1);
204 ADDR=ADDR+1
205 TX$=ETX$+CR$+STX$
206 NEXT:NEXT:NEXT
207 PRINT STRING$(14,8);INT(100*ADDR/4096);"%;TAB(6);" COMPLETE";
208 NEXT:NEXT
209 CLOSE 1:PRINT"PROM DATA FILE ";OF$;" IS READY." :SYSTEM
210
211 ' END
212

```

Program 5-1. BASIC Program to Generate PROM Data (Continued)

Section 6

Floating-Point System Design Using the 'AS888/'AS890

Bit-slice processor architecture addresses the problem of optimizing system performance while allowing the user to balance hardware complexity against software flexibility. Bit-slice systems usually operate at or near the speed of the most primitive of programmable processors, the PROM state sequencer. Of course, bit-slice architecture incorporates circuitry dedicated not only to sequencing, but also data processing (ALU) operations. In keeping with the trend of these programmable devices to track the speed of fast discrete hardware, the 'AS888 8-bit slice ALU and 'AS890 microsequencer have been produced in Advanced Schottky bipolar technology. In addition to sheer speed, the components feature greater density (2 micron geometry) for greater functionality (more special purpose circuitry on board). The impact will be faster, more powerful systems in applications which previously pushed the limits of bit-slice processors.

Consider an application in which bit-slice architecture has dominated for years: CPU design. The microprogrammed CPU itself spans a spectrum of uses ranging from general purpose minicomputers to compact airborne computers. A specific example which illustrates various facets of design using the 'AS888 and 'AS890 is a CPU with a floating-point utility to compute $\sin(x)$.

The design process can be subject to many influences, including personal preference, available development tools, peculiarities of the application, and constraints from the user, customer or manufacturing environment. No hard and fast design rules could be applied universally, but most designers will start with a specific plan in mind.

The goal of this example is to produce the hardware and microprogram which will implement the $\sin(x)$ function in floating-point arithmetic. Before the microprogram can be assembled, the hardware must be defined since the fields of

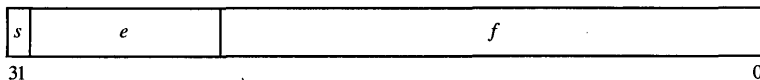
the microinstruction are dedicated to specific hardware once the microinstruction register is hardwired to the devices it controls. Since the final architecture chosen depends on trade-offs between implementing certain operations in hardware or software, critical applications will require that a cursory analysis of the software be made before the hardware is cast in concrete. Attempting to develop microcode for a tentative architecture will force the issue on which operations are better suited for hardware. Before the architecture or the microprogram requirements can be known, the algorithms which describe the application processes must be defined. Once an algorithm is formulated it can be broken down into operations involving variable and constant quantities. The variables can be assigned to registers and then the algorithm can be translated into a microprogram. The following steps illustrate the plan for this CPU design example incorporating a floating-point $\sin(x)$ utility:

- Step 1: Choose a floating-point number system
- Step 2: Choose an algorithm for approximating $\sin(x)$
- Step 3: Make 'AS888 register assignments
- Step 4: Substitute registers for variables in the algorithm
- Step 5: Decompose steps of the algorithm into simple operations
- Step 6: Translate into 'AS888/890 operations; identify subroutines
- Step 7: Expand subroutines into 'AS888/890 operations
- Step 8: Evaluate trade-offs and block diagram the hardware
- Step 9: Define microinstruction fields during detailed hardware design
- Step 10: Assemble the microprogram

STEP 1: CHOOSE A FLOATING-POINT NUMBER SYSTEM

An IEEE floating-point format will be chosen for this example for portability of data and software. It is important to note that the IEEE defines many standards in arithmetic processing, but for simplicity this example will encompass only number format. Furthermore, while several formats are IEEE compatible, only the basic single-precision format will be considered.

The IEEE basic single-precision format is defined as a 32-bit representation in which the component fields are a 1-bit sign s , an 8-bit biased exponent e and a 23-bit fraction f which are assembled in the following order:



The quantity is evaluated as $(-1)^s 2^{e-127} (1.f)$. Not-a-number, zero and infinity have special representations. The one preceding the binary point is implied and is called the implicit one or implicit bit. It coincides with the fact that the digits are normalized (left justified).

STEP 2: CHOOSE AN ALGORITHM FOR Sin(x)

Many algorithms are discussed in the literature for approximating useful quantities like $\sin(x)$. Literature research is a good place to start to familiarize oneself with various algorithms and trade-offs for a particular application. Computer simulation is also useful to compare algorithms for speed and accuracy. R.F. Ruckdeschel in *BASIC Scientific Subroutines*, Vol. 1 (BYTE, McGraw-Hill Publications Co., New York, N.Y., 1981, pp. 159–191) discusses trade-offs and provides a simulation in BASIC for a $\sin(x)$ algorithm. An adaptation of this material has been chosen for this example:

- A) Reduce angle range to first quadrant. ($0 \leq x \leq \pi/2$)
- B) Compute $\sin(x) \approx \sum_{n=0}^6 A_n x^{2n-1}$. The coefficients are:

Coefficient	Decimal	IEEE hex
A ₀	1.000000	3F80 0000
A ₁	-0.1666667	BE2A AAAD
A ₂	0.008333333	3C08 8888
A ₃	-0.0001984127	B950 0D01
A ₄	0.000002755760	3638 EF99
A ₅	-0.0000002507060	B2D7 5AD5
A ₆	0.000000001641060	2F34 6FBC

The algorithm can be implemented in the following steps:

- A) Reduce angle range to first quadrant. ($0 \leq x \leq \pi/2$)
- 1) SIGN = SGN(x)
 - 2) ABSX = |x|
 - 3) XNEW = ABSX - $2\pi \times \text{INT}(\text{ABSX}/2\pi)$
 - 4) If XNEW > π then SIGN = -SIGN and XNEW = XNEW - π
 - 5) If XNEW > $\pi/2$ then XNEW = π - XNEW

where

$$\text{SGN}(x) = \begin{cases} +1 & \text{if } x \geq 0 \\ -1 & \text{if } x < 0 \end{cases}$$

INT(x) = integer function

- B) Compute $\sin(x) \approx \sum_{n=0}^6 A_n x^{2n-1}$.
- 1) Let XSQR = XNEW²; INITIALIZE SINX = 0
 - 2) Do i = 6 to 1 step -1
 SINX = XSQR × SINX + A(i)
 Enddo
 - 3) SINX = SIGN × XNEW × SINX

Step B-2 computes the summation in a geometric series for economy. The major difference between steps A and B is that A requires more diverse ALU operations while B uses only multiplication and addition recursively.

STEP 3: MAKE 'AS888 REGISTER ASSIGNMENTS

Just as in assembly language programming, registers must be allocated for variables. Using R_n to denote the 'AS888 register whose address is n, where $0 \leq n \leq F$ (hex), the following register assignments can be made:

R0 = X
 R1 = SIGN
 R2 = ABSX
 R3 = XNEW
 R4 = XSQR
 R5 = SINX

The following constants can also be defined:

Constant	Decimal	IEEE hex
$PI = \pi$	3.141593	4059 0FDB
$PIOVR2 = \pi/2$	1.570797	3FC9 0FDB
$2PI = 2\pi$	6.283185	40C9 0FDB
$IOVR2PI = 1/2\pi$	0.159155	3E22 F981

STEP 4: SUBSTITUTE REGISTERS FOR VARIABLES IN THE ALGORITHM

Now the algorithm can be rewritten with registers replacing variables:

- A) Reduce angle range to first quadrant ($0 \leq x \leq \pi/2$).
- 1) $R1 = \text{SGN}(R0)$
 - 2) $R2 = \lceil R0 \rceil$
 - 3) $R3 = R2 - 2\pi \times \text{INT}(R2/2\pi)$
 - 4) If $R3 > \pi$ then $R1 = -R1$; $R3 = R3 - \pi$
 - 5) If $R3 > \pi/2$ then $R3 = \pi - R3$
- B) Compute $\sin(x) \approx \sum_{n=0}^6 A_n x^{2n-1}$.
- 1) Let $R4 = R0^2$; INITIALIZE $R5 = 0$
 - 2) Do $i=6$ to 1 step -1
 $R5 = R4 \times R5 + A(i)$
 Enddo
 - 3) $R5 = R1 \times R0 \times R5$

Since various references to constants are made, it is probably best to load constants as needed rather than attempt to allocate registers for them. Constants can be loaded from a constant field in the microinstruction or from ROM. The trade-off is 32 bits by 16K of micromemory versus 32 bits by the number of constants (typically less than 16K). For this example, it will be assumed that a constant field in the microinstruction is acceptable.

STEP 5: DECOMPOSE STEPS IN THE ALGORITHM INTO SIMPLE OPERATIONS

The $\sin(x)$ function can be microprogrammed as a subroutine; let FSIN be its entry address. R0 would be loaded with x before FSIN was called. Upon return, R5 would contain $\sin(x)$. Now decompose the steps in the algorithm into simple arithmetic and logical operations. Other operations can be left as functions to be defined later.

FSIN: SUBROUTINE

; A) Reduce angle range to first quadrant. ($0 \leq x \leq \pi/2$)

$R1 = \text{SGN}(R0)$; 1) Let $R1 = \text{Sign of } R0$
$R2 = \text{ABS}(R0)$; 2) $R2 = \lceil R0 \rceil$
$R3 = R2 * IOVR2PI$; 3) $R3 = R2 - 2\pi * \text{INT}(R2/2\pi)$
$R3 = \text{INT}(R3)$;
$R3 = R3 * 2PI$;
$R3 = R2 - R3$;
$Y = R3 - PI$; 4) If $R3 > \pi$,
Jump if Negative to Step A-5	;
$R1 = -R1$; then $R1 = -R1$;
$R3 = R3 - PI$; $R3 = R3 - \pi$
$Y = \text{PIOVR2} - R3$;
Jump if Negative to Step B-1	; 5) If $R3 > \pi/2$
$R3 = PI - R3$; then $R3 = \pi - R3$

```

; B) Compute  $\sin(x) \approx \sum_{n=0}^6 A_n x^{2n-1}$ 
R4 = R0 * R0 ; 1) Let R4 = R02. Let R5 = 0
R5 = 0 ;

R5 = R4 * R5 ; 2) Do i=6 to 1 step -1
R5 = R5 + A6 ; R5 = R4 × R5 + A(i)
R5 = R4 * R5 ; Enddo
R5 = R5 + A5 ;
R5 = R4 * R5 ; (To implement a loop,
R5 = R5 + A4 ; use an 'AS890 counter
R5 = R4 * R5 ; to index a memory containing
R5 = R5 + A3 ; the constants.)
R5 = R4 * R5 ;
R5 = R5 + A2 ;
R5 = R4 * R5 ;
R5 = R5 + A1 ;
R5 = R4 * R5 ;
R5 = R5 + A0 ;

R5 = R0 * R5 ; 3) R5 = R1 × R0 × R5
R5 = R5 * R1 : RETURN ;

```

END SUBROUTINE

STEP 6: TRANSLATE INTO 'AS888/890 INSTRUCTIONS; IDENTIFY SUBROUTINES

The simplified steps of the algorithm can be represented fairly easily as 'AS888/890 instructions. Necessary functions (and suggested names) can be identified by inspection as:

- 1) FMUL — Floating-point multiplication
- 2) FADD — Floating-point addition
- 3) FINT — Floating-point integer conversion
- 4) FINV — Floating-point additive inverse (to subtract using FADD)
- 5) FABS — Floating-point absolute value
- 6) FSGN — Floating-point sign test
- 7) FCHS — Floating-point change of sign (to multiply by SIGN)

"Function" in this context refers to a special operation regardless of how it is coded. In fact, FMUL and FADD are fairly complex and require detailed explanation. FINV, FABS, FSGN and FCHS are single instruction operations that mask or mask and test. FINT requires several inline instructions or a subroutine and will be left to the interested reader as an exercise. Now the steps of the algorithm can be translated into 'AS888/890 operations which include references to these functions.

FSIN: SUBROUTINE

```

; A) Reduce angle range to first quadrant. ( $0 \leq x \leq \pi/2$ )
R1 = FSGN(R0) ; Get sign bit (MSB)
R2 = FABS(R0) ; Take absolute value (clear MSB)
R3 = FMUL(R2, 1OVR2PI) ; Multiply register and constant
R3 = FINT(R3) ; Floating-point integer conversion
R3 = FMUL(R3, 2PI) ; Multiply register and constant
R3 = FADD(R2, INV(R3)) ; Subtract registers by adding inverse
Y = FADD(R3, NEGPI) : TEST NEG ; Subtract by adding negative constant
JT SIN1 ; Jump if true (jump if negative)
R1 = FINV(R1) ; Complement sign of R1
R3 = FADD(R3, NEGPI) ; Subtract by adding negative constant
SIN1: Y = PIOVR2 - R3 : TEST NEG ; Subtract to compare (don't store)
JT SIN2 ; Jump if true (jump if negative)
R3 = FADD(PI, FINV(R3)) ; Subtract by adding negative register

```

; B) Compute $\sin(x) \approx \sum_{n=0}^6 A_n X^{2n-1}$

```

SIN2: R4 = FMUL(R0,R0)           ; Square by multiplying
      R5 = A6                   ; Initialize series
      R5 = FMUL(R4,R5)          ; Multiply registers
      R5 = FADD(R5,A5)          ; Add coefficient
      R5 = FMUL(R4,R5)          ; Multiply registers
      R5 = FADD(R5,A4)          ; Add coefficient
      R5 = FMUL(R4,R5)          ; Multiply registers
      R5 = FADD(R5,A3)          ; Add coefficient
      R5 = FMUL(R4,R5)          ; Multiply registers
      R5 = FADD(R5,A2)          ; Add coefficient
      R5 = FMUL(R4,R5)          ; Multiply registers
      R5 = FADD(R5,A1)          ; Add coefficient
      R5 = FMUL(R4,R5)          ; Multiply registers
      R5 = FADD(R5,A0)          ; Add coefficient
      R5 = FMUL(R0,R5)          ; Multiply registers
      R5 = FCHS(R5,R1) : RETURN ; Change MSB of R5 to MSB of R1

```

END SUBROUTINE

This contrived language has a syntax which may be suitable for a source program. For the sake of illustration, it can be assumed that the microassembler recognizes this particular syntax. The series was computed inline instead of using a loop since it is relatively short. If a loop were used, a means of indexing the constants would be required.

STEP 7: EXPAND SUBROUTINES INTO 'AS888/890 OPERATIONS

FMUL and FADD algorithms can now be expanded. Since they are called extensively from FSIN, they are more critical to the efficiency of the final design. Wherever possible, it is desirable to reduce the execution time of both in order to maintain efficiency.

Floating-Point Multiplication

Let M1 be the multiplier and M2 be the multiplicand whose product is P. Let the sign, exponent and fraction fields of their IEEE representation be:

```

M1 : |S1|E1|F1|
M2 : |S2|E2|F2|
P  : |S3|E3|F3|

```

P is found by multiplying mantissas (fraction plus implicit one) and adding exponents. Since M1 and M2 are normalized, the range of $1.F1 \times 1.F2$ is

$$1.00\dots0 \leq 1.F1 \times 1.F2 \leq 11.1\dots10$$

The implicit bit may "overflow" into bit position 24. This type of overflow must be detected so that the result can be normalized. Normalization requires right shifting the result of $1.F1 \times 1.F2$ and incrementing E3. The implicit bit is then cleared when S3, E3 and M3 are packed to form P. The floating-point multiplication algorithm may then be defined as follows:

- 1) Unpack M1 into signed fraction (SF1) and exponent (E1)
- 2) Set the implicit bit in SF1
- 3) Unpack M2 into signed fraction (SF2) and exponent (E2)
- 4) Set the implicit bit in SF2
- 5) Perform SF3 = SF1 \times SF2 using signed integer multiplication
- 6) Perform E3 = E1 + E2
- 7) Test SF3 for overflow into bit 24
- 8) If true, then increment E3 and right shift SF3
- 9) Clear the implicit bit in SF3
- 10) Pack E3 and SF3 to get P

As before, the steps of this algorithm can be broken down into simpler operations:

- 1) Unpack M1 into signed fraction (SF1) and exponent (E1)
 $E1 = \text{FEXP}(M1)$
 $SF1 = \text{FRAC}(M1)$
- 2) Set the implicit bit in SF1
 $SF1 = SF1 \text{ OR } \text{BIT}23$
- 3) Unpack M2 into signed fraction (SF2) and exponent (E2)
 $E2 = \text{FEXP}(M2)$
 $SF2 = \text{FRAC}(M2)$
- 4) Set the implicit bit in SF2
 $SF2 = SF2 \text{ OR } \text{BIT}23$
- 5) Perform $SF3 = SF1 \times SF2$ using signed integer multiplication
 $SF3 = \text{IMUL}(SF1, SF2)$
- 6) Perform $E3 = E1 + E2$
 $E3 = E1 + E2$
- 7) Test SF3 for overflow into bit 24
 $\text{TEST}(SF3 \text{ AND } \text{BIT}24)$
 JUMP IF FALSE to step 9
- 8) If true, then increment E3 and right shift SF3
 $\text{INC } E3$
 $SF3 = \text{RSHFT}(SF3)$
- 9) Clear the implicit bit in SF3.
 $SF3 = SF3 \text{ AND } \text{NOT_BIT}23$
- 10) Pack E3 and SF3 to get P
 $P = SF3 \text{ OR } E3$

FEXP, FRAC, testing bit 24 and setting/clearing bit 23 are all mask operations that translate into single 'AS888 instructions. The integer multiplication (IMUL) is simply the multiplication algorithm supported by the 'AS888 instruction set. No significant hardware features are required to do floating-point multiplication, nor are any subroutines required to support it.

Register assignments can now be made as before. Since FSIN uses registers in the lower half of the register file, it might be preferable to restrict FMUL to the upper registers. For example:

```
RF = P
RE = M1, F1, SF1
RD = M2, F2, SF2
RC = E1
RB = E2
```

RE and RD can share variables that need not be preserved. Using this assignment, FMUL computes $RF = \text{FMUL}(RE, RD)$. RE and RD must be loaded prior to calling FMUL and RF must be stored upon return. By substituting registers for variables and reorganizing operations in the FMUL algorithm to better fit 'AS888/890 operations the following source program may be created:

```
FMUL: SUBROUTINE
      RC = FEXP(RE)           ; Unpack M1 into exponent
      RE = FRAC(RE)          ; and fraction
      RE = RE OR BIT23       ; Set implicit bit
      MQ = SMTC(RE)          ; Prepare to multiply
      RB = FEXP(RD)           ; Unpack M2 into exponent
      RD = FMAG(RD)          ; and fraction
      RD = RD OR BIT23       ; Set implicit bit
      RD = SMTC(RD)          ; Prepare to multiply
```

```

RE = 0 : RCA = #22d           ; Initialize to multiply
RE = SMULI RD : LOOP RCA     ; Integer multiplication iteration
RE = SMULT RD                 ; Final step in signed multiply
Y = TB0(RE,BIT1):BYTE = #0100b:TEST Z ; Test "overflow"
JF FMULI                      ; Jump if false (exponent ok)

INEX(RC)                      ; Increment exponent: add 00800000
RE = SRA(RE)                  ; Shift fraction to normalize

FMULI:RC = RC + RB : TEST CARRY ; Add exponents and test carry
JT ERROR                      ; Jump if carry true to handler

RE = SMTC(RE)                 ; Get sign magnitude fraction
RE = RE AND #807F_FFFFh      ; Clear implicit bit
RF = RE OR RC : RETURN        ; Pack fraction and exponent

```

Floating-Point Addition

The floating-point addition algorithm (FADD) is slightly more complex than FMUL, since the two addends will usually not have the same exponent. Therefore the smaller (absolute value) addend must first be chosen by comparing exponents. Then it must be denormalized to align its digits with the digits of the larger addend. In other words, the two addends must have the same exponent before their fractions can be added. This process can be described by the following algorithm:

- 1) Unpack A1 to get SF1 and E1
- 2) Set implicit bit in SF1
- 3) Unpack A2 to get SF2 and E2
- 4) Set implicit bit in SF2
- 5) If $E2 > E1$ then go to step 9
($|A1| \leq |A2|$)
- 6) Let DIFF = E1 - E2
- 7) Do i = 1 to DIFF
SF2 = RSHFT(SF2) (Arithmetic right shift)
Enddo
- 8) Let E3 = E1, go to step 12
($|A2| > |A1|$)
- 9) Let DIFF = E2 - E1
- 10) Do i = 1 to DIFF
SF1 = RSHFT(SF1) (Arithmetic right shift)
Enddo
- 11) Let E3 = E2
- 12) SF3 = SF1 + SF2
- 13) Test "overflow" into bit 24
- 14) Jump if false to step 17
- 15) Increment exponent E3
- 16) Normalize signed fraction with right arithmetic shift
- 17) Clear implicit bit
- 18) Pack: SUM = SF3 or E3
- 19) Return

Register assignments for variables must now be made. Since FSIN uses registers in the lower half of the 'AS888 register file, it is necessary to use the upper registers:

```

RF = SUM
RE = A1, F1, SF1
RD = A2, F2, SF2
RC = E1
RB = E2

```

By slightly reorganizing the sequence to better fit 'AS888/890 operations, the following microprogram to perform FADD can be created:

```

FADD: SUBROUTINE
; 1) Unpack A1 to get SF1 and E1
   RC = FEXP(RE)           ; Get exponent (E1)
   RE = FRAC(RE)          ; Get signed fraction (SF1)
; 2) Set implicit bit in SF1
   MQ = RE OR BIT23       ; Set implicit bit
   RE = SMTC(RE)         ; Convert to two's complement
; 3) Unpack A2 to get SF2 and A2
   RB = FEXP(RD)          ; Get exponent (E2)
   RD = FRAC(RD)         ; Get signed fraction (SF2)
; 4) Set implicit bit in SF2
   RD = RD OR BIT23       ; Set implicit bit
   RD = SMTC(RD)         ; Convert to two's complement
; 5) If E2 > E1 then go to step 9
   RF = RC - RB : TEST NEGATIVE ; Compare A2 from A1
   JT FADD1 : RCA = #8      ; Jump if E2 > E1; set up loop count
; 6) Let DIFF = E1 - E2.
   Y/RF = SLC(RF) : LOOP RCA ; Rotate 8 times to get difference
   RCA = Y/RF              ; Load difference in loop counter
; 7) Do i = 1 to DIFF
;   ;
;   SF2 = RSHFT(SF2)
;   Enddo
;   RD = SRA(RD) : LOOP RCA ; Orient digits of smaller addend
; 8) Let E3 = E1, go to step 12
   RB = RC : JUMP FADD2     ; Swap registers and branch
; 9) Let DIFF = E2 - E1
FADD1: RF = NOT(RF)         ; Complement result of E1 - E2
   Y/RF = SLC(RF) : LOOP RCA ; Shift 8 times to get DIFF
   RCA = Y/RF              ; Load DIFF in loop counter
;10) Do i = 1 TO DIFF
;   ;
;   SF1 = RSHFT(SF1)
;   Enddo
;   RE = SRA(RE) : LOOP RCA ; Align SF1 with SF2
;11) Let E3 = E2 (no instruction required — RB already has E2 in it)
;12) SF3 = SF1 + SF2
FADD2: RF = RD + RE         ; Add
   RF = SMTC(RF)          ; Convert to sign-magnitude
;13) Test "overflow" into bit 24
   RF = TB0 (RF, BIT24)   ; Check for normalization
;14) Jump if false to step 17
   JF FADD3                ; If so, finish and exit
;15) Else increment exponent
   INC RB : TEST NEG       ; Test for exponent overflow
;16) Normalize signed fraction
   RF = SRA(RF) : JT ERROR ; Jump to error handler if overflow

```

```

;17) Clear implicit bit
FADD3: RF = SET0 (RF, BIT23)           ; Reset bit 23 of RF

;18) Pack: SUM = SF3 OR E3
      RF = RF OR RB : RETURN           ; OR signed fraction and exponent

```

There is an important consequence of FADD which impacts the hardware. Since the number of shifts required to denormalize the small addend is data dependent (computed in the ALU), it is necessary to provide a path between the ALU Y bus and the 'AS890 DRA bus. All the other operations are simple 'AS888/890 instructions, including the FRAC and FEXP mask operations discussed during the development of FMUL. ERROR is a floating-point overflow error handler.

STEP 8: EVALUATE TRADE-OFFS AND BLOCK DIAGRAM THE HARDWARE

A rough estimate of the FSIN worst case execution time can be arrived at by making the following observations about FSIN, FMUL and FADD:

FMUL

```

integer recursion ≈ 22 cycles
other instructions ≈ 18 cycles
total ≈ 40 cycles

```

FADD

```

denormalization ≈ 23 cycles
other instructions ≈ 25 cycles
total ≈ 50 cycles

```

FSIN

```

number of calls to FMUL = 12
number of calls to FADD = 11
number of other cycles ≈ 10

```

Approximate worst case total = $10 + (12 \times 40) + (11 \times 50) = 1040$ cycles. At 50 nanoseconds per cycle, this requires approximately 52 microseconds. There are few improvements that could be made in hardware to speed this time, except perhaps the addition of a flash multiplier which would reduce the integer computation by about 20 cycles (an overall reduction of about two percent). A barrel shifter could have the same benefit during floating-point addition for a total reduction of about 4 percent. For the sake of simplicity, it will be assumed that 52 microseconds is acceptable for the $\sin(x)$ computation.

Another issue which must be considered is the problem of loading the 'AS888 and 'AS890 with constants. A slight materials cost reduction might be realized by storing constants in table PROMs rather than in control store memory. An interesting use of the DRA and DRB ports on the 'AS890 would be to use the output of RCA or RCB to index data in the constant PROM. This would allow long series to be implemented in loop form rather than the inline method used in FSIN. Once again, the constant PROM will not be implemented for the sake of simplicity.

Now the architecture can be designed to meet the requirements identified throughout this analysis:

- 1) A path between the 'AS888 Y bus and the 'AS890 DRA bus.
- 2) A path between the microinstruction register and the 'AS890 DRA bus for loading loop counts and branch addresses.
- 3) A path between the microinstruction register and the 'AS888 Y bus for loading constants.
- 4) Independent control of $\overline{STO0}$ in each 'AS888 slice to allow bit/byte instructions.
- 5) A status register to store 'AS888 status for testing.
- 6) A status mux to test the 'AS888 status, bit 23 of the 'AS888 Y bus, bit 24 of the 'AS888 Y bus and hardwired 0 and 1.

A system having these features is illustrated in Figure 6-1.

STEP 9: DEFINE MICROINSTRUCTION FIELDS DURING DETAILED HARDWARE DESIGN

The detailed hardware design will produce a wiring diagram that fixes the position within the microinstruction of each of the various control signals that are connected from the microinstruction register to the 'AS888, 'AS890, status mux and any other special hardware. Once this design is complete it is possible for the assembler to sort the control bits of each instruction properly so that they will be properly oriented when the microprogram is installed in the target system.

STEP 10: ASSEMBLE THE MICROPROGRAM

TI is currently developing an 'AS888/890 microassembler. Several microassemblers are commercially available, and many users prefer to write their own. The microprogram shown in Table 6-1 was hand-assembled, but has a syntax that is suitable for interpretation by a user-written assembler.

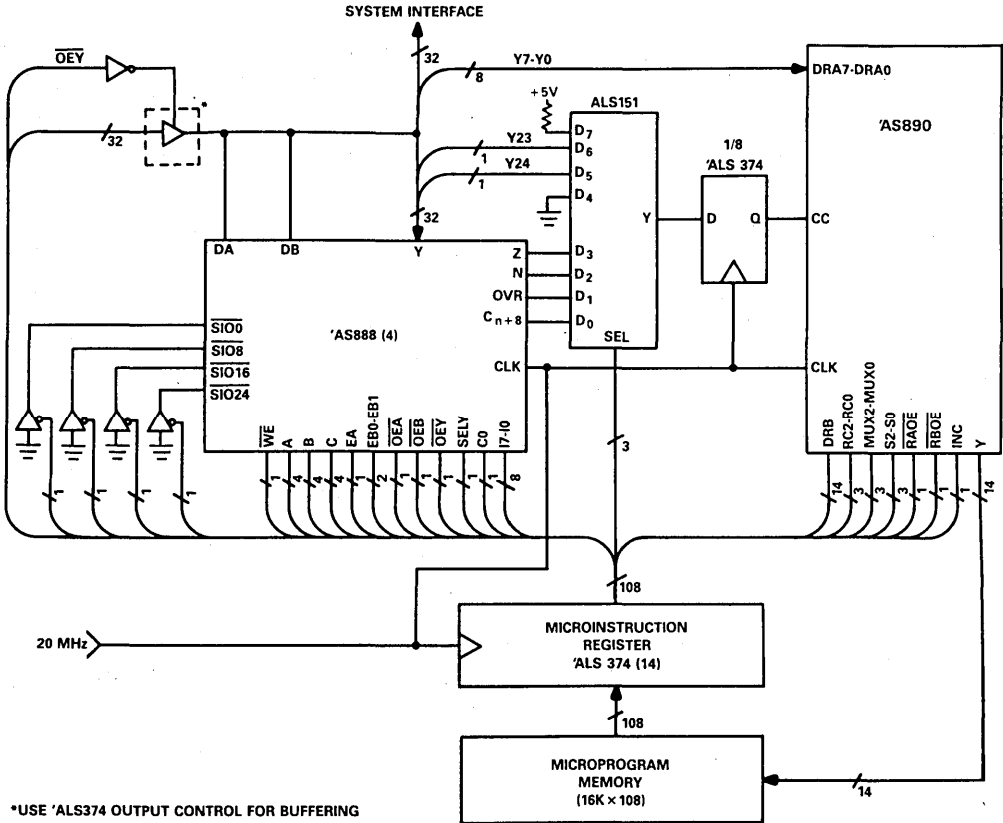


Figure 6-1. Block Diagram of Floating-Point Processor

Table 6.1. Floating Point Sin(x) Microprogram

	WE	A3-A0	B3-B0	C3-C0	EA	EB1-EB0	DEB	DEA	OEB	OEA	SELY	Cn	17:10	32-bit Constant	S100	S108	S1016	S1024	RC2-RC0	MUX2-MUX0	S2-S0	DRB13-DRB0	RAOE	RROE	INVC	SEL	
0000 SIN:														8 0 0 0 0 0 0 0	1 1 1 1					0 2 7	X X X X	1 1 1 1					
0001														X X X X X X X X	1 1 1 1						0 2 7	X X X X	1 1 1 1				
0002														X X X X X X X X	1 1 1 1	0					0 2 7	X X X X	1 1 1 1				
0003														X X X X X X X X	1 1 1 1						0 2 7	X X X X	1 1 1 1				
0004														3 E A 2 F 9 8 4	1 1 1 1						0 2 7	X X X X	1 1 1 1				
0005														X X X X X X X X	1 1 1 1						0 1 4	0 0 6 0 1	1 1 1 1				
0006														X X X X X X X X	1 1 1 1						0 2 7	X X X X	1 1 1 1				
0007														X X X X X X X X	1 1 1 1						0 2 7	X X X X	1 1 1 1				
0008														X X X X X X X X	1 1 1 1						0 1 4	1 1 1 1				
0009														X X X X X X X X	1 1 1 1						0 2 7	X X X X	1 1 1 1				
000A														X X X X X X X X	1 1 1 1						0 2 7	X X X X	1 1 1 1				
000B														4 0 C 9 0 F D B	1 1 1 1						0 2 7	X X X X	1 1 1 1				
000C														X X X X X X X X	1 1 1 1						0 1 4	0 0 6 0 1	1 1 1 1				
000D														X X X X X X X X	1 1 1 1						0 2 7	X X X X	1 1 1 1				
000E														X X X X X X X X	1 1 1 1						0 2 7	X X X X	1 1 1 1				
000F														8 0 0 0 0 0 0 0	1 1 1 1						0 2 7	X X X X	1 1 1 1				
0010														X X X X X X X X	1 1 1 1						0 1 4	0 0 7 4 1 1	1 1 1 1				
0011														X X X X X X X X	1 1 1 1						0 2 7	X X X X	1 1 1 1				
0012														X X X X X X X X	1 1 1 1						0 2 7	X X X X	1 1 1 1				
0013														C 0 5 9 0 F D B	1 1 1 1						0 2 7	X X X X	1 1 1 1				
0014														X X X X X X X X	1 1 1 1						0 1 4	0 0 7 4 1 1	1 1 1 1				
0015														X X X X X X X X	1 1 1 1						0 2 7	X X X X	1 1 1 1				
0016														X X X X X X X X	1 1 1 1						0 1 7	0 0 0 0 1 1	1 1 1 1				
0017														8 0 0 0 0 0 0 0	1 1 1 1						0 2 7	X X X X	1 1 1 1				
0018														X X X X X X X X	1 1 1 1						0 2 7	X X X X	1 1 1 1				
0019														C 0 5 9 0 F D B	1 1 1 1						0 2 7	X X X X	1 1 1 1				
001A														X X X X X X X X	1 1 1 1						0 1 4	0 0 7 4 1 1	1 1 1 1				
001B														X X X X X X X X	1 1 1 1						0 2 7	X X X X	1 1 1 1				
001C														X X X X X X X X	1 1 1 1						0 2 7	X X X X	1 1 1 1				
001D														8 0 0 0 0 0 0 0	1 1 1 1						0 2 7	X X X X	1 1 1 1				
001E														X X X X X X X X	1 1 1 1						0 1 4	0 0 7 4 1 1	1 1 1 1				
001F														X X X X X X X X	1 1 1 1						0 2 7	X X X X	1 1 1 1				
0020														X X X X X X X X	1 1 1 1						0 1 7	0 0 0 0 1 1	1 1 1 1				
0021														4 0 5 9 0 F D B	1 1 1 1						0 2 7	X X X X	1 1 1 1				
0022														8 0 0 0 0 0 0 0	1 1 1 1						0 2 7	X X X X	1 1 1 1				
0023														X X X X X X X X	1 1 1 1						0 1 4	0 0 7 4 1 1	1 1 1 1				
0024														X X X X X X X X	1 1 1 1						0 2 7	X X X X	1 1 1 1				
0025														X X X X X X X X	1 1 1 1						0 2 7	X X X X	1 1 1 1				
0026														X X X X X X X X	1 1 1 1						0 2 7	X X X X	1 1 1 1				
0027														X X X X X X X X	1 1 1 1						0 1 4	0 0 6 0 1	1 1 1 1				
0028														X X X X X X X X	1 1 1 1						0 2 7	X X X X	1 1 1 1				

Table 6.1. Floating Point Sin(x) Microprogram (Continued)

```

0056      * R5 = FADD(R5,A0)
          RE = R5
0057      RD = #3F80 0000h
0058      JSR FADD
0059      R5 = RF

          * R5 = FMUL(R0,R5)
005A      RE = R0
005B      RD = R5
005C      JSR FMUL
005D      R5 = RF

          * R5 = FCHS(R5,R1) : RETURN
005E      R1 = R1 OR #7FFF FFFFh
005F      R5 = R5 XOR R1 : RETURN

          * RC = FEXP(RE)
0060 FMUL: RC = RE AND #7F80 0000h

0061      * RE = FRAC(RE)
          RE = RE AND #807F FFFFh

0062      * RE = RE OR bit23
          RE = RE OR #0080 0000h

          * MQ = SMTC(RE)
0063      RE = SMTC(RE)
0064      LOADMQ : PASS

          * RB = FEXP(RD)
0065      RB = RD AND #7F80 0000h

          * RD = FRAC(RD)
0066      RD = RD AND #807F FFFFh

0067      RD = RD OR bit23
0068      RD = SMTC(RD)
0069      RE = 0 : RCB = #22D
006A      RE = SMULI RD : LOOP RCB
006B      RE = SMULT RD
006C      TB0(RE,bit1) : BYTE = #0100b : TEST Z
006D      JT FMUL1

          * INEX RC
006E      RC = RC ADD #0080 0000h
006F      RE = SRA(RE)

0070 FMUL1: RC = RC ADD RB : TEST CARRY
0071      JT ERROR

0072      RE = SMTC(RE)
0073      RE = RE AND #807F FFFFh

          * FADD: RC = FEXP(RE)
0074 FADD: RC = RC AND #7F80 0000

          * RE = FRAC(RE)
0075      RE = RE AND #807F FFFFh

0076      MQ = RE OR bit23
0077      RE = SMTC(RE)

          * RB = FEXP(RD)
0078      RB = RD AND #7F80 0000
    
```

VF	A3-A0	R3-R0	C3-C0	EA	EB1-EB0	DEB	OEB	SELY	Cn	I7-I0	32-bit Constant	S100	S108	S1016	S1024	RC2-RC0	MUX2-MUX0	S2-S0	DRB13-DRB0	RAOE	RBOE	INC	SEL							
0	5	X	E	0	X	1	1	1	0	0	F	6	X	X	X	X	X	X	X	0	2	7	X	X	X	X	1	1	1	7
0	X	X	D	X	X	1	1	1	X	F	F	3	F	8	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	7
1	X	X	X	X	1	1	1	X	X	F	F	X	X	X	X	X	X	X	X	1	1	1	1	1	1	1	1	1	1	7
0	F	X	5	0	X	1	1	1	0	0	F	6	X	X	X	X	X	X	X	1	1	1	1	1	1	1	1	1	1	7
0	0	X	E	0	X	1	1	1	0	0	F	6	X	X	X	X	X	X	X	0	2	7	X	X	X	X	1	1	1	7
0	5	X	D	0	X	1	1	1	0	0	F	6	X	X	X	X	X	X	X	1	1	1	1	1	1	1	1	1	1	7
1	X	X	X	X	1	1	1	X	X	F	F	X	X	X	X	X	X	X	X	1	1	1	1	1	1	1	1	1	1	7
0	F	X	5	0	X	1	1	1	0	0	F	6	X	X	X	X	X	X	X	1	1	1	1	1	1	1	1	1	1	7
0	1	X	1	0	2	1	1	1	0	0	F	B	7	F	F	F	F	F	F	1	1	1	1	1	1	1	1	1	1	7
0	5	1	5	0	0	1	1	1	0	0	F	0	X	X	X	X	X	X	X	1	1	1	1	1	1	1	1	1	1	7
0	E	X	C	0	2	1	1	1	0	0	F	A	7	F	8	0	0	0	0	1	1	1	1	1	1	1	1	1	1	7
0	E	X	E	0	2	1	1	1	0	0	F	A	8	0	7	F	F	F	F	1	1	1	1	1	1	1	1	1	1	7
0	E	X	F	0	2	1	1	1	0	0	F	B	0	0	8	0	0	0	0	1	1	1	1	1	1	1	1	1	1	7
0	X	E	E	X	0	1	1	1	1	0	5	8	X	X	X	X	X	X	X	1	1	1	1	1	1	1	1	1	1	7
1	E	X	X	0	X	1	1	1	1	0	E	6	X	X	X	X	X	X	X	1	1	1	1	1	1	1	1	1	1	7
0	D	X	B	0	2	1	1	1	0	0	F	A	7	F	8	0	0	0	0	1	1	1	1	1	1	1	1	1	1	7
0	D	X	D	0	2	1	1	1	0	0	F	A	8	0	7	F	F	F	F	1	1	1	1	1	1	1	1	1	1	7
0	D	X	D	0	2	1	1	1	0	0	F	B	0	0	8	0	0	0	0	1	1	1	1	1	1	1	1	1	1	7
0	X	D	D	X	0	1	1	1	D	5	8	X	X	X	X	X	X	X	X	1	1	1	1	1	1	1	1	1	1	7
0	E	E	E	0	0	1	1	1	1	0	F	9	0	0	0	0	0	1	6	1	1	1	1	1	1	1	1	1	1	7
0	D	E	E	0	0	1	1	1	0	6	0	X	X	X	X	X	X	X	X	1	1	1	1	1	1	1	1	1	1	7
0	D	E	E	0	0	1	1	1	0	7	0	X	X	X	X	X	X	X	X	1	1	1	1	1	1	1	1	1	1	7
0	0	F	0	0	1	1	1	1	0	3	8	X	X	X	X	X	X	X	X	1	0	1	1	1	1	1	1	1	1	7
1	X	X	X	X	X	1	1	1	X	F	F	X	X	X	X	X	X	X	X	1	1	1	1	1	1	1	1	1	1	7
0	C	X	C	0	2	1	1	1	0	0	F	1	0	0	8	0	0	0	0	1	1	1	1	1	1	1	1	1	1	7
0	E	X	E	0	X	1	1	1	0	0	6	X	X	X	X	X	X	X	X	1	1	1	1	1	1	1	1	1	1	7
0	C	B	C	0	0	1	1	0	0	F	1	X	X	X	X	X	X	X	X	1	1	1	1	1	1	1	1	1	1	7
1	X	X	X	X	1	1	1	X	X	F	F	X	X	X	X	X	X	X	X	1	1	1	1	1	1	1	1	1	1	7
0	X	E	E	X	0	1	1	1	1	0	5	8	X	X	X	X	X	X	X	1	1	1	1	1	1	1	1	1	1	7
0	E	X	E	0	2	1	1	1	0	0	F	A	8	0	7	F	F	F	F	1	1	1	1	1	1	1	1	1	1	7
0	C	X	C	0	2	1	1	1	0	0	F	A	7	F	8	0	0	0	0	1	1	1	1	1	1	1	1	1	1	7
0	E	X	E	0	2	1	1	1	0	0	F	A	8	0	7	F	F	F	F	1	1	1	1	1	1	1	1	1	1	7
1	E	X	X	0	1	1	1	1	0	E	B	0	0	8	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	7
0	E	X	E	0	2	1	1	1	0	0	F	A	8	0	7	F	F	F	F	1	1	1	1	1	1	1	1	1	1	7
0	D	X	B	0	2	1	1	1	0	0	F	A	7	F	8	0	0	0	0	1	1	1	1	1	1	1	1	1	1	7

Table 6.1. Floating Point Sin(x) Microprogram (Continued)

* RD = FRAC(RD)
 0079 RE = RE AND #807F FFFFh
 007A RD = RD OR bit23
 007B RD = SMTC(RD)
 007C RF = RC - RB : C0=0: TEST NEG
 007D JT FADD1 : RCB = #8
 007E Y/RF = SLC(RF) : LOOP RCB
 007F Y = RF : RCA = Y
 0080 RD = SRA(RD) : LOOP RCA
 0081 RB = RC : JUMP FADD2
 0082 FADD1: RF = NOT RF
 0083 Y/RF = SLC(RF) : LOOP RCB
 0084 Y = RF : RCA = Y
 0085 RE = SRA(RE) : LOOP RCA
 0086 FADD2: RF = RD + RE
 0087 RF = SMTC(RF)
 0088 RF = TB0 (RF, bit24) : TEST Z
 0089 JF FADD3
 008A INC RB : TEST NEG
 008B RF = SRA(RF) : JT ERROR
 008C FADD3: RF = SET0 (RF, bit23)
 008D RF = RF OR RB : RETURN

WE	A3-A0	B3-B0	C3-C0	EA	EB1-EB0	OEA	OEB	OEC	SELY	Cn	17-10	32-bit Constant	S100	S10B	S10R	S10Z4	FC2-RC0 MUX2-MUX0 S2-S0	DRB13-DRB0	RAOE	RBOE	INC	SEL		
0079	0	E	X	E	0	2	1	1	1	0	0	F	A	8	0	7	F	F	F	F	F	F	F	F
007A	0	D	X	D	0	2	1	1	1	0	0	F	B	0	0	8	0	0	0	0	0	0	0	0
007B	0	X	D	D	X	0	1	1	1	1	0	5	F	X	X	X	X	X	X	X	X	X	X	X
007C	0	C	B	F	0	0	1	1	1	0	0	F	3	X	X	X	X	X	X	X	X	X	X	X
007D	1	X	X	X	X	1	1	1	X	X	F	F		X	X	X	X	X	X	X	X	X	X	X
007E	0	F	X	F	0	X	1	1	0	X	0	6	6	X	X	X	X	X	X	X	X	X	X	X
007F	1	X	X	X	X	1	1	0	X	F	F			X	X	X	X	X	X	X	X	X	X	X
0080	0	D	X	D	0	X	1	1	1	0	0	6	6	X	X	X	X	X	X	X	X	X	X	X
0081	0	C	X	B	0	X	1	1	1	0	X	F	F	X	X	X	X	X	X	X	X	X	X	X
0082 FADD1:	0	F	X	F	0	X	1	1	1	0	0	F	7	X	X	X	X	X	X	X	X	X	X	X
0083	0	F	X	F	0	X	1	1	0	0	6	6	6	X	X	X	X	X	X	X	X	X	X	X
0084	1	X	X	X	X	1	1	0	X	F	F			X	X	X	X	X	X	X	X	X	X	X
0085	0	E	X	E	0	X	1	1	1	0	0	6	6	X	X	X	X	X	X	X	X	X	X	X
0086 FADD2:	0	D	E	F	0	1	1	1	0	0	F	1	1	X	X	X	X	X	X	X	X	X	X	X
0087	0	X	F	F	0	1	1	1	0	5	8			X	X	X	X	X	X	X	X	X	X	X
0088	0	0	F	0	0	1	1	1	0	3	8			X	X	X	X	X	X	X	X	X	X	X
0089	1	X	X	X	X	1	1	X	X	F	F			X	X	X	X	X	X	X	X	X	X	X
008A	0	B	X	B	0	X	1	1	1	1	F	6	6	X	X	X	X	X	X	X	X	X	X	X
008B	0	F	F	0	X	1	1	1	0	0	6	6	6	X	X	X	X	X	X	X	X	X	X	X
008C FADD3:	0	7	F	0	0	1	1	1	0	1	8			X	X	X	X	X	X	X	X	X	X	X
008D	0	F	B	F	0	0	1	1	1	0	0	F	B	X	X	X	X	X	X	X	X	X	X	X

Excerpt from
SN74AS888, SN74AS890
Bit-Slice Processor
User's Guide



TEXAS
INSTRUMENTS

3

Application Reports

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4. 32-Bit CPU Design Methodology

Microprogramming and bit-slice technology have made possible the development of powerful systems using flexible instructions sets and wide address/data buses to access more than one Gigaword of physical main memory. This section discusses one design approach to such a system, using 'AS888 bit-slice and 'AS890 microsequencer components.

A structured approach to system design, such as that illustrated in Figure 4-1, is recommended in developing custom bit-slice designs. The product specification gives a starting point or basis for the project. In this example, four 'AS888 bit slices are used to implement the 32-bit arithmetic portion of the CPU, and an 'AS890 microsequencer is used for ALU and system control. A group of PROMs stores the microinstructions; a writable control store could also be implemented using additional control logic and components to load and modify the microprogram memory. The system is designed to access more than one Gigaword of memory.

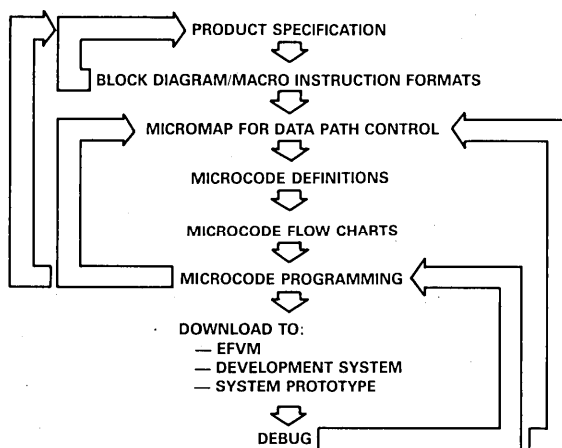


Figure 4-1. System Design Approach

Since speed is a concern, carry look-ahead rather than ripple-through logic is recommended. If ripple-through logic were used, the system clock would need to be slowed down to allow the propagation of the carry bits through the various 'AS888 stages. By using carry look-ahead, the amount of time needed for the data to stabilize is greatly reduced by anticipating the carry across the 'AS888 packages.

So that the scratchpad area can be used for address calculations and mathematical computations, the 'AS888's internal register file is dedicated for system functions. To provide the system user with a macrolevel equivalent of register locations, a 16-word external register file is also included. Access to the external register file will be under microprogram control, allowing address selection to come from the microcode itself or from one of the three operand fields of the instruction register.

PROMs eliminate the use of main memory as a source for constants used in initialization or table look-up functions. Accessing main memory for table values would require time and slow system throughput; by placing fixed values in fast PROMs, access time is kept to a minimum and system throughput is not altered.

Control, data and address buses shared by the system are accessed by three-state registers. The control register, as explained in section 4.1.2, supplies the non-CPU part of a computer system with control signals. The data bus allows the ALU to supply data for the rest of the system and can also be a source of data for the ALU; this is accomplished by using three-state registers to drive the bi-directional data bus, along with registers to sample the bus. The address bus uses one of the external register file locations to maintain a program counter, thus allowing a 32-bit address bus capable of addressing about four Gigawords of main memory. Using three-state drivers for this bus enables other subsystems to take control of the system buses.

A pipeline register supplies the microsequencer and the ALU with both data and instructions. To get macrocode into the system, an instruction register and a mapping PROM are used to convert the opcode to a microprogram routine address. The condition code signal, used for testing various conditions, is supplied by a register-input based PAL. PAL inputs can be fixed values or combinations of the status signals coming from the ALU. The read address select pins for the 'AS888's internal B register can be sourced from the microword itself or from three nibbles of the macroword, to provide offsets for the N-way branches to various microcode routines.

4.1 Designing a 32-Bit System

A typical 32-bit system block diagram using the 'AS888 bit-slice and 'AS890 microsequencer is shown in Figures 4-2 and 4-3. It can be broken down into two sections, the ALU (arithmetic logic unit) and the CCU (computer control unit). The ALU section performs all manipulation of data both to and from main memory, such as arithmetic and logical operations. The CCU section controls instruction (macrocode) flow and any miscellaneous control operations, such as fetching instructions or supplying addresses for main memory access.

4.1.1 Construction of the ALU

To cascade the four 'AS888s to obtain the 32-bit arithmetic unit shown in Figure 4-4, the shift multiplex $\overline{SIO0}$ and $\overline{QIO0}$ terminals are connected to the $\overline{SIO7}$ and $\overline{QIO7}$ terminals of adjacent packages, and the least significant package's signals are connected to the most-significant package's. Optionally, SN74ALS240 inverting gates can be connected to the $\overline{SIO0}$ - $\overline{SIO7}$ terminals and the byte inputs to implement byte and bit control. Another chip, the SN74AS182 look-ahead carry generator, provides a ripple-carry function, to help system throughput.

The design includes a 16-word register file, the SN74AS870 (see Figure 4-3). This allows the user to access 16 working areas for temporary data storage or address calculations such as indexing. In this design example, the 'AS888's internal register file is not accessible directly by the user; it is reserved for microcode operations, such as address computation and temporary storage for arithmetic operations. Addressing the register files is permitted through the microprogram or from the macrocode instruction register under microcode control.

The transfer register connected to the 'AS888's Y and DB buses allows for feedback into the 'AS888 under microprogram control. Since the constant PROMs and the external register file share the A bus, they cannot be accessed at the same time. The transfer register enables data from the external register file to be transmitted to the B bus, making possible the addition of operands from the constant PROMs and the external register file, for example.

Constant PROMs are also included to simplify the programming and operation of the ALU by supplying fixed data for various operations, such as:

- 1) Clearing the system register files for initialization. This will bring the system up to a known state.
- 2) Supplying a correction value to the offset in a branch instruction, i.e., converting a 16-bit offset to a true 32-bit address.
- 3) Table look-up for fixed mathematical operations, such as computing sines and cosines.

4.1.2 Construction of the CCU

Sequencing and branching operations at speeds compatible with the 'AS888 are supplied by the 'AS890, a microprogrammed controller working as a powerful microsequencer (see Figure 3-1). Features of the 'AS890 include:

- 1) Stack capability. The 9-word stack can be accessed by using a stack pointer or a read pointer; the latter is designed for non-destructive dumping of the stack contents.
- 2) Register/counter facility. Two registers, DRA and DRB, can be used for latching data from the external data buses or as counters for loops. A ZERO signal is generated when the decremented counter reaches a zero value.
- 3) Interrupt control. A register for temporarily holding the return address is supplied; upon entering the interrupt routine, the contents of the return register must be pushed onto the stack for later use.
- 4) Next address generation. The Y output multiplexer offers a selection of same or incremented address, address from DRA or DRB buses, address from stack, or a concatenation of DRA13-DRA4 and B3-B0.

A microprogram memory/pipeline register supplies the microsequencer and the rest of the system with instructions (see Figure 4-2). The memory might consist of ROMs, or it could be a writable-control store with support logic to allow loading or updating of the control store. For a general purpose machine with a fixed instruction set, ROMs would be more economic.

Some 'AS890 instructions are influenced by the \overline{CC} input. Many are variations of branch and jump instructions. To form and supply \overline{CC} , a register can be used to latch the state of the 'AS888 and supply inputs to a PAL for decoding, based upon the microcode's needs. Combinatorial logic in the PAL allows multiple or single events to be selected or provides a fixed value of "1" or "0" for forced conditions.

To supply the microsequencer with the proper address of the microcode-equivalent version of the macrocode instruction, an instruction register and mapping PROM are needed. Under microprogram control, the instruction register samples the data bus to get the macrocode instruction. The opcode portion is passed to the mapping PROM to form an address to the microcode routine. When the microcode is ready to jump to the routine, it turns off the Y bus output of the 'AS890 and enables the output of the mapping PROM. An optional means of altering the address uses B3-B0 inputs of the 'AS890 to implement a N-way branch routine. In this method, the ten most significant address bits of DRA or DRB are concatenated with the B3-B0 bits to supply an address.

Control information is supplied to the rest of the system via the control register and bus. By setting various bits within the control register, information can be passed to other subsystems, such as memory and I/O peripherals. Bit 0 could represent the read/write control line while bit 1 could select memory or I/O for the read/write. Bit 2 might function to enable interrupts and bit 3 to indicate when the system should enter a "wait" state for slow memory. The remaining control bits can be programmed by the system designer to indicate additional condition states of the "macrosystem".

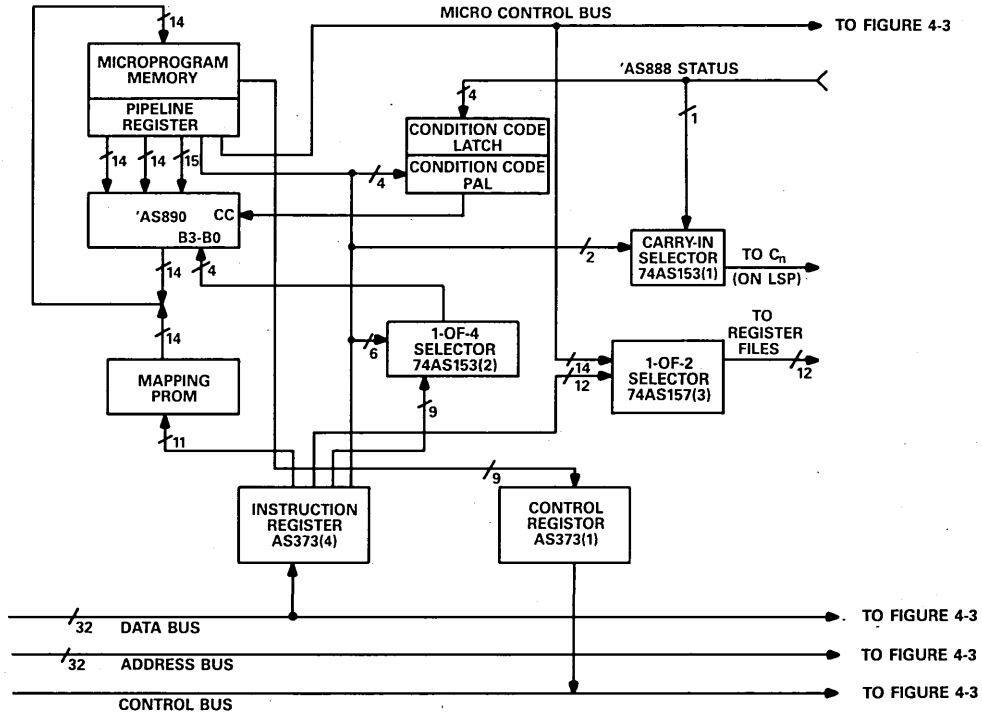


Figure 4-2. CCU Block Diagram

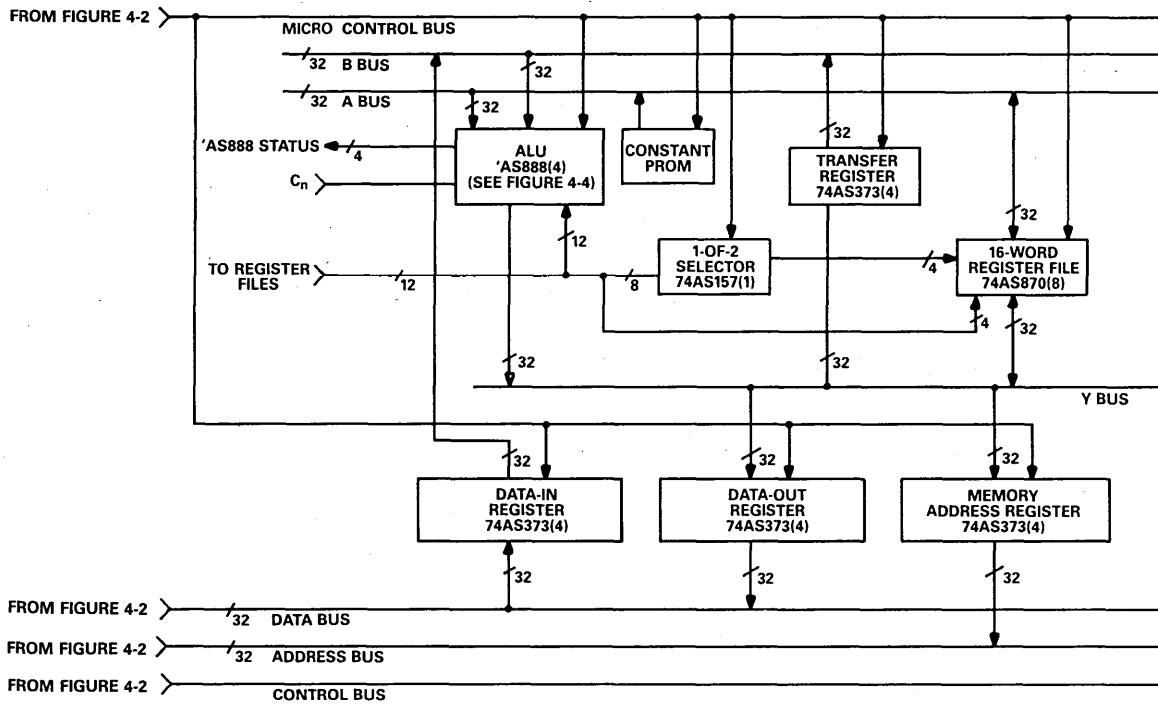


Figure 4-3. ALU Block Diagram



Addressing of the register files, both the 'AS888 internal and the 'AS870 external, is done through the use of two 1-of-2 selector banks. The first bank selects address source; this design offers a choice for operand processing of fixed values from the microcode or values from the macroinstruction latched in the instruction register. The second bank selects the first or second operand as an address source for port 0 of the external register file; port 1 uses the third operand as an address source.

It should be noted that the design presented in Figure 4-2 for the computer control unit is a one-level pipeline that is instruction-data based. The address and contents of the next instruction are being fetched while the current instruction is being executed. Tracing through the data flow, the following can be observed:

- 1) The pipeline register contains the current instruction being executed;
- 2) The ALU has just executed its instruction, and has the current status ready at its output pins;
- 3) The status register that is attached to the ALU contains the previous instruction's resulting status;
- 4) The contents of the next microprogram word are being fetched at the same time that the current instruction is being executed.

4.2 Tracing through a 32-Bit Computer

With the 'AS888 and 'AS890 as foundation chips, the typical 32-bit supermini of Figures 4-2 and 4-3 can now be functionally traced. First, note that the data of the main program is handled separately from that of the microcode — each on its own bus. The system is initialized by setting the "clear" signal high — this causes a forced jump to the beginning of the microcode memory. Instructions carried out by the microcode at this point might run system diagnostics, clear all registers throughout the 'AS888-based system, and set up the initial macrocode program address. In this design, the first program address to fetch an instruction from main memory comes from a fixed value in the microcode memory; it is possible to allow the address to be retrieved from a permanent location in main memory or from either a front panel or console, by modifying the microcode program slightly.

Table 4-1 illustrates the microcode format for this design. Note that it contains control signals for all chips involved in the design. Some of these, such as **TRANSLATCH** and **MARLATCH**, are used with the system clock to provide controlled loading of the various holding registers. Others supply necessary addressing information, directing input from either the main data bus or from the microcode word itself.

The **FETCH** routine is shown in functional, assembler and microcoded forms in Tables 4-2, 4-3 and 4-4. First, the program counter is read from the external register file and stored into the memory address register. After the program counter is placed on the address bus, the program counter is updated and stored while the data from memory is allowed to settle down to a stable condition. The data is then latched in both the instruction register and data-in register.

The opcode field of the instruction register is passed through the mapping PROM to convert the opcode to an equivalent microcode routine address. When **YOE** is forced high by the microcode, the 'AS890 is tri-stated from the Y bus, and the mapping PROM's output is taken out of the tri-state mode to supply an address to the control store (microprogram memory); a forced jump is made to the microcode routine to perform the instruction.

After the routine is complete, a jump is made back to the **FETCH** routine using the next-address supplied by the microprogram. It is up to the system designer/programmer to make sure that all system housekeeping is performed so that nothing causes a fatal endless loop.

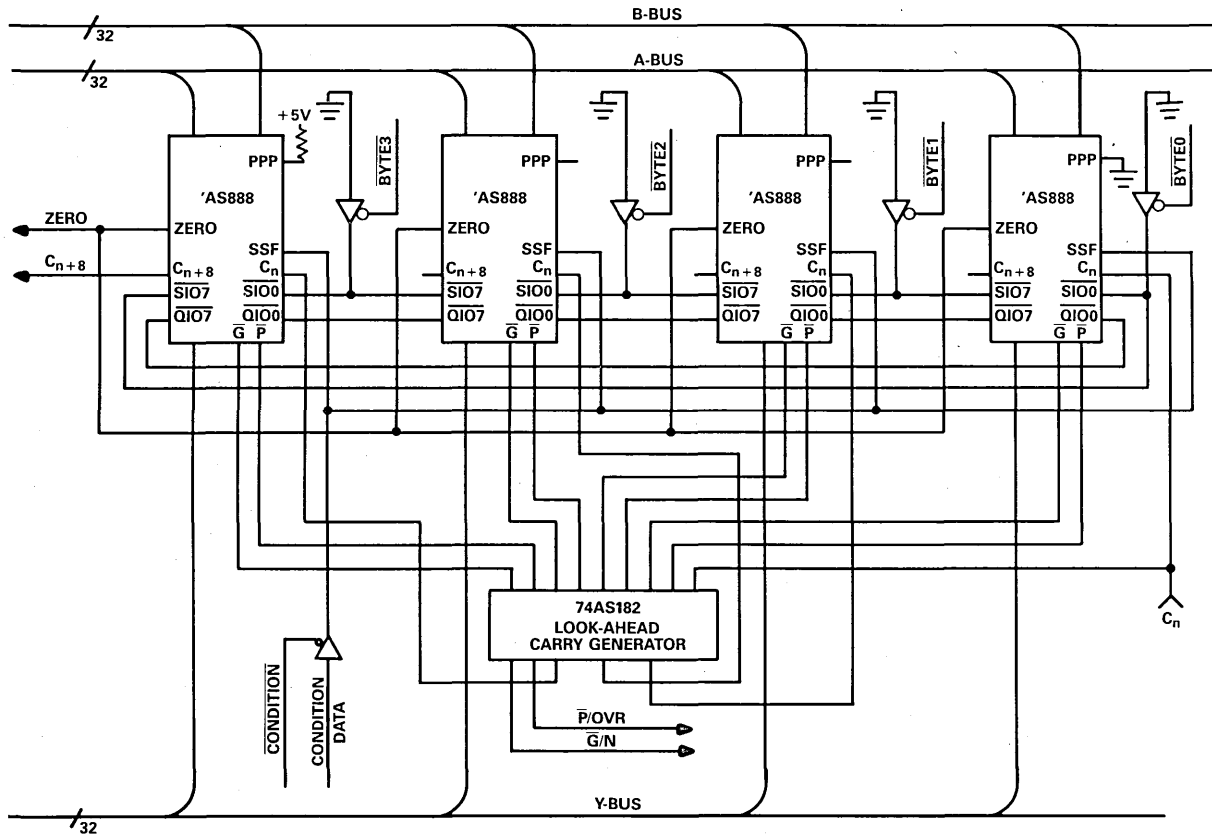


Figure 4-4. Cascaded 'AS888 Packages

Table 4-1. Microcode Definition

MICROCODE FIELD	PIN NAME	INPUT TO	FUNCTION
0-13	DRA13-DRA0	'AS890	Used for next-address branches
14-27	DRB13-DRB0	'AS890	Used for loading counter
28-30	RC2-RC0	'AS890	Register/counter controls
31-33	S2-S0	'AS890	Stack control
34-36	MUX2-MUX0	'AS890	MUX control of Y output bus
37	INT	'AS890	Interrupt control
38	RAOE	'AS890	Enables DRA output
39	RBOE	'AS890	Enables DRB output
40	OSEL	'AS890	Mux control for DRA source
41	INC	'AS890	Incrementer control
42	YOE	'AS890	Enables Y output bus
43-50	I7-I0	'AS888	Instruction inputs
51	OE \bar{A}	'AS888	DA bus enable
52	E \bar{A}	'AS888	ALU input operand select
53	OE \bar{B}	'AS888	DB bus enable
54	OEY	'AS888	Y bus output enable
55	SELY	'AS888	Y bus select
56-57	EB1-EB0	'AS888	ALU input operand selects
58	WE	'AS888	Register file write enable
59	MAP	PROM	Enables mapping PROM to 'AS890 Y bus
60	IR	Latch	Latches data bus to instruction register
61	CR	Latch	Latches control data to bus
62-69	CTRL7-CTRL0	Latch	Data for control latch
70-71	BSEL1-BSELO	Multiplexer	Selects data for 'AS890
72-75	B3-B0	Multiplexer	Microcode data to switch
76	CONDCD	Latch	Controls latch of 'AS888 status
77-80	SELC3-SELCO	PAL	Selects combination of 'AS888 status
81	DTALATCHI	Latch	Controls latching of data-in
82	DTAIN	Latch	Enables data-in output to bus
83	DTALATCHO	Latch	Controls latching of data-out
84	DTAOUT	Latch	Enables data-out output to DB bus
85	MARLATCH	Latch	Controls latching of address
86	MAR	Latch	Enables MAR output to address bus
87	CONSTPROM	PROM	Enables PROM to DA bus
88-99	A11-A0	PROM	Address of constant in PROM
100	SWITCH2	Multiplexer	Selects microcode or Instruction Register data
101	SWITCH1	Multiplexer	Selects microcode or Instruction Register data
102-105	A3-A0	Multiplexer	Register file address ('AS888)
106-109	B3-B0	Multiplexer	Register file address ('AS888)
110-113	C3-C0	Multiplexer	Register file address ('AS888)
114	REGUWR	Register File	Port 0 write enable
115	REGLWR	Register File	Port 1 write enable
116	REGU	Register File	Chip enable on port 0
117	REGL	Register File	Chip enable on port 1
118	TRANSLATCH	Latch	Controls latch between Y and DB bus
119	TRANS	Latch	Enables output to DB bus
120	SELCN2	Multiplexer	Supplies carry input to 'AS888
121	SELCN1	Multiplexer	Supplies carry input to 'AS888
122	REGUB	Multiplexer	Selects address for external register file
123-126	BYTE3 - BYTE0	Three-state	Enables data for byte/bit operations

Table 4-2. Functional Listing of Fetch

FETCH:	MAR = PC, Enable MAR output
	PC = PC + 1
	IR = DIR = data bus, Disable 'AS890 Y bus, Enable mapping PROM to Y bus

Table 4-3. Assembler Listing of Fetch

FETCH: OP890 ,,111,10;INC;	Set 'AS890 for continue
OP888 NOP,GROUP5,10,,,1111;	Perform NOP and read external register 15
OBY;SELY;	Enable Y bus output
CR;CTRL 00000011;	Generate external control bus signals
SELC 01;	Select fixed CC value to 'AS890
MARLATCH;MAR;	Latch value on Y bus and enable output
SWITCH 00;REGL;	Select address source and enable port
TRANSLATCH	Latch Y bus for transfer to B bus
OP890 ,,111,10;INC;	Set 'AS890 for continue
OP888 PASS,INCS,00,,,1111;	Increment program counter
OEB;OEY;	Enable Y bus output
SELC 01;	Select fixed CC value to 'AS890
MAR;	Output address to address bus
REGLWR;REGL;	Update program counter in register file
TRANS;	Enable transfer latch output to B bus
SELCN 01	Select carry input to LSP to be "1"
OP890 ,,111,10;	Set 'AS890 for continue
OP888 NOR,GROUP5,10;	Perform NOP
MAP;	Enable mapping PROM to 'AS890 Y bus
IR;	Latch data bus to get macrolevel code
SELC 01	Select fixed CC value to 'AS890
DTALATCHI;	Put data bus also in data register
MAR	Output address to address bus

Key to Table 4-3

OP888 a,b,c,d,e,f

where:

- a = upper bits of instruction, 17-14
- b = lower bits of instruction, 13-10
- c = value of EB1-EB0
- d = A address of register files
- e = B address of register files
- f = C address of register files

OP890 v,w,x,y,z

where:

- v = DRA value, 14-bits
- w = DRB value, 14-bits
- x = RC2-RC0
- y = S2-S0
- z = MUX2-MUX0



Table 4-4. Microcode Listing of Fetch.

DRA13- DRA0	DRB13- DRB0	RC2-RC0	S2-S0	MUX2-MUX0	INT RAGE RBOE OSEL INC YOE	17-10	OEA OEB OEC OED OEE OEF OEG OEH OEI OEN OEO OEP OEQ OER OES OET OEU OEV OEW OEX
0000000000000000	0000000000000000	000	111	010	1111010	1111111111	11101101
0000000000000000	0000000000000000	000	111	010	1111010	1111101000	11000001
0000000000000000	0000000000000000	000	111	010	1111001	1111111111	01111101

Table 4-4. Microcode Listing of Fetch (continued)

CTRL7- CTRL0	BSEL1-BSEL0	B3-B0	CONDCO	SELC3-SELC0	DIALATCHI DIAIN DIALATCHO DIAOUT MARLATCH MAR CONSTPROM	A11-A0	SWITCH2-SWITCH1	A3-A0	B3-B0	C3-C0	REGUWR REGLWR REGU REGL REGI REGO TRANS SELCN2 SELCN1 REGUB	BYTES-BYTE0
00000011	00	0000	1	0001	11111001	00000000000000	00	0000	0000	1111	1111001000	1111
00000000	00	0000	1	0001	11111101	00000000000000	00	0000	0000	1111	101010010	1111
00000000	00	0000	1	0001	01111101	00000000000000	00	0000	0000	0000	111111000	1111

4.3 Defining the Macrocode Instruction Format

Since this is a 32-bit design, a variety of instruction formats are available. The size of the opcode, along with the types of addressing used, will affect both system size and performance. The formats shown in Table 4-5 will be used for discussion.

All Table 4-5 formats have an opcode field of 11 bits and source/destination fields of 7 bits; the first three bits of the latter designate the address type, and the remaining four bits are used for register access. The opcode length allows 2,048 macrocoded instructions to be mapped to equivalent microcoded routines. The address fields can specify any of the following modes: register, relative, autoincrement/autodecrement, indexed, absolute, and deferred. The offset used in the Type 0 instruction can be used for branch-based instructions, for an offset range of ± 32727 .

Table 4-5. Possible Instruction Formats

TYPE 0 — OPCODE + 16-BIT OFFSET

0 — 10 Opcode	11 — 15 Not Used	16 — 31 Offset
------------------	---------------------	-------------------

TYPE 1 — OPCODE + DESTINATION

0 — 10 Opcode	11 — 24 Not used	25 — 31 Destination
------------------	---------------------	------------------------

TYPE 2 — OPCODE + SOURCE + DESTINATION

0 — 10 Opcode	11 — 17 Not used	18 — 24 Source	25 — 31 Destination
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TYPE 3 — OPCODE + SOURCE1 + SOURCE2 + DESTINATION

0 — 10 Opcode	11 — 17 Source	18 — 24 Source	25 — 31 Destination
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4.4 Tracing a Macrocode Instruction

Microcode for a Type 3 multiplication instruction is shown in Table 4-6, using the following assumptions:

- 1) Code for retrieving the operands will not be shown. Jumps will be made to routines that will place the temporary operands into internal register locations 2 and 3 of the 'AS888, after being fetched from main memory.
- 2) A jump to a routine to store the product in the destination will be handled similarly.
- 3) Multiplication will be unsigned; the result will be placed in two temporary locations of the 'AS888.
- 4) An update to the program status word, which the user can access at the macrocode level must also be performed, but is not shown.

Assembler code is shown in Table 4-7; a microcode listing is given in Table 4-8. The first two lines of microcode are subroutine jumps to opcode fetching routines, which store the operands in register files 2 and 3 in the 'AS888. The next two instructions load up the 'AS890 with a counter constant for performing the multiply loop, load the MQ register of the 'AS888 with the multiplier and clear the register that is temporarily used for the accumulator.

Table 4-6. Functional Listing of Multiply

UMUL3:	
JUMPSUB SOURCE1	Get first operand
JUMPSUB SOURCE2,	Get second operand
BCOUNT=32	Load DB counter register
REG 9=0	Clear temporary accumulator
MQ=REG 2	Load multiplier
LOOP:	
UMULI WITH REG 3	Issue the multiply
DECREMENT BCOUNT,	Decrement the DB counter
BRANCH TO LOOP IF NOT ZERO,	Loop back until done
LATCH 'AS888 STATUS,	Store 'AS888 flags
REG 9=ALU	Store intermediate result
REG 8=MQ	Store intermediate result
JUMPSUB STORPSW	Update macro program status
JUMPSUB MDEST	Store result at destination
JUMP FETCH	Get next instruction

A loop is then entered to perform the multiply instruction 32 times to form the product, with the multiplicand coming from the internal register file of the 'AS888. Upon exiting the loop, the MQ register is stored in a temporary register location in the 'AS888. The MQ register now contains the least-significant bits of the result and the temporary accumulator the most significant bits. A subroutine jump is made to the program status word update routine; this will take the status flags of the last multiplication iteration and change the macrolevel status word. The next subroutine jump is to a destination routine, which is followed by a branch to the FETCH routine to get the next macro instruction to be executed.

4.5 System Enhancements

The above example provides a broad overview of 32-bit system design using the 'AS888 and 'AS890. Certain additional options may enhance system performance. These include:

- 1) Status latching. The design does not take into account changes that need to be examined at the microlevel while retaining macrolevel status information. One solution would be to include another register in parallel to the status latch and provide control to choose between the two to form the condition code value.
- 2) Interrupts. To efficiently use a computer system, interrupts are used to alter program flow in the case of I/O programming and real-time applications (involving hardware timers). To include this capability, external hardware must be included and the microcode modified accordingly. Information on interrupt implementation is given in section 3.
- 3) Control store. One way of implementing microprogram memory is to use a ROM-based design. It is becoming more common to design a writable control store, a completely RAM-based or part RAM, part ROM storage system, that can be altered by system operation, such as initialization from a floppy disk subsystem, or by the user to optimize or implement new macrolevel instructions. The cost of implementation must be weighed with the risks involved in changing instructions which may not be supported by other sites.
- 4) Instruction word definitions. Changing the instruction word definitions will have an effect on both system design and performance. Removing Type 3 instructions from the design, for example, will have an effect on both hardware and software: the external register file addressing must be changed and the 1-of-2 selector

Table 4-7. Assembler Code of Multiply

UMULB:	
OP890 SOURCE1,,,110,110;	Perform a subroutine branch
INC;YOE;	Increment address and enable Y bus
OP888 NOP;GROUP5;	Tell 'AS888 to do nothing during jump
SELC 0001;	Set CC to "1" to set up 'AS890 continue
MAR	Maintain address on main address buss
OP890 SOURCE2,00000000100000,110,110,110;	Perform subroutine branch and load B counter
INC;YOE;	Increment microaddress and enable Y bus
OP888 NOP;GROUP5;	Tell 'AS888 to do nothing during jump
SELC 0001;	Set CC to "1" to set up 'AS890 continue
MAR	Maintain address on main address bus
OP890 ,,111,110;	Perform a continue instruction
INC;YOE;	Increment microaddress and enable Y bus
OP888 CLEAR,GROUP5,,,,1001;	Zero out register file accumulator
WE;	Enable writing to register file
SELC 0001;	Set CC to "1" to set up 'AS890 continue
MAR	Maintain address on main address buss
OP890 LOOP,,111,110;	Perform a continue instruction
INC;YOE;	Increment microaddress and enable Y bus
OP888 LOADMQ,INCS,,0010;	Load MQ register with S + Cn, from external register file
MAR	Maintain address on main address bus
LOOP:	
OP890 LOOP,101,111,100;	Decrement B and loop til ZERO = 1
INC;YOE;	Increment microaddress and enable Y bus
OP888 UMULI,GROUP4,01,0011,,1001;	Perform unsigned multiply on accumulator
WE;	Update register file accumulator
MAR	Maintain address on main address bus
OP890 ,,111,110;	Perform a continue instruction
INC;YOE;	Increment microaddress and enable Y bus
OP888 PASS,INCS,,,,1000;	Put S + Cn in temporary register file
WE;	Allow updating of register file
MAR	Maintain address on main address bus
OP890 STORPSW,,110,110;	Perform a subroutine branch
INC;YOE;	Increment microaddress and enable Y bus
OP888 NOP;GROUP5;	Tell 'AS888 to do nothing during jump
SELC 0001;	Set CC to "1" for set up 'AS890 continue
MAR	Maintain address on main address bus
OP890 FETCH,,,111;	Perform a branch to FETCH routine
INC;YOE;	Increment microaddress and enable Y bus
OP888 NOP;GROUP5;	Tell 'AS888 to do nothing during jump
SELC 0001	Set CC to "1" for 'AS890 continue

Key to Table 4-7.

OP888 a,b,c,d,e,f

where:

- a = upper bits of instruction, 17-14
- b = lower bits of instruction, 13-10
- c = value of EB1-EB0
- d = A address of register files
- e = B address of register files
- f = C address of register files

OP890 v,w,x,y,z

where:

- v = DRA value, 14-bits
- w = DRB value, 14-bits
- x = RC2-RC0
- y = S2-S0
- z = MUX2-MUX0

removed. Likewise, changing the opcode length may restrict the instruction address capability and also cause either an increase or decrease in the microcode size.

- 5) Dynamic memory access (DMA). The above system does not support dynamic memory access. To include this function requires a change in the address output control, along with support circuitry for the type of DMA selected. Some error detection and correction logic for main memory might also be included.
- 6) Computer control unit. The design presented here shows a one-level pipeline architecture that is instruction-data based. System throughput may be increased by converting to a pipeline of greater depth, or using another variety of one-level pipeline, such as instruction-address based or address-data based. Care must be taken when increasing the size of the pipeline, especially when handling branch/jump situations. The reader is advised to carefully research this area before implementing any design.

4.6 Timing and System Throughput

A critical path analysis was undertaken to determine the maximum clock rate for the proposed system. The longest delay path is the multiplication data path, which involves the internal register file and the shift function of the 'AS888. Table 4-9 contains the critical delay calculations for both the ALU and CCU. Since both portions of the system must be satisfied, a clock rate of 90 ns was selected for the following comparisons.

4.6.1 Fetch Analysis

Most microprocessors perform an instruction fetch in a pipeline mode; the next instruction is fetched while the current instruction is executing. The fetch code shown earlier requires a minimum of four cycles: three to issue the code and one to break the pipeline for processing the branch. This results in a total time of 360 ns, based on a 90 ns cycle time. Fetch times for the representative microprocessors have been estimated from data books and are shown in Table 4-10; wait states for slow memory are not included. As can be seen from the table, the 'AS888 design example is estimated to run from 1.1 to 2.1 times faster than the 16-bit microprocessors.

4.6.2 Multiplication Analysis

This analysis assumes that multiplication is unsigned integer and register to register based. No account is taken of time needed for instruction fetch or operand fetch or store.

The basic loop for the multiply takes 35 cycles: 2 for accumulator and multiplier set up, 32 for actual multiply loop and 1 to store the least-significant bits in an internal register file. Given a cycle time of 90 ns, a 32 by 32 bit multiplication can be implemented in 2.275 microseconds. A 16-bit multiply requires 16 iterations of the inner loop; both timings are included in Table 4-11 for comparison. Values for the 16-bit multiplies of the representative microprocessors have been estimated from data books.

As shown in Table 4-11, the 16 by 16 multiply can be performed with the 'AS888 at a faster rate than the 16-bit microprocessors. Even comparing the 32 by 32 multiply of the application design, one can see that the 'AS888 based system has a better macroinstruction execution speed. Using the 'AS888 and 'AS890 in a system design will allow high throughput and permit a flexible architecture.

Table 4-9. Critical Delay Path Analysis

CONTROL PATH			DATA PATH		
Pipeline Reg.	Clock to Output	9	'AS888-1	Clock to C _n	46
MUX	Select to Output	13	'AS182	C _n to C _{n+z}	5
'AS890-1	CC to Output	25	'AS888-1	C _n to SIO	25
PROM	Access Time	20	'AS888-1	SIO to Y	14
Pipeline Reg.	Setup Time	2			90 ns
		69 ns			

Table 4-10. Fetch Timing Comparison

FETCH	'AS888 32-BIT	Z8001	8086-1	80286	68000L
Data width	32	16	16	16	16
No. of cycles	4	3	4	4	4
Clock rate	11.11 MHz	4 MHz	10 MHz	10 MHz	8 MHz
Total time	360 ns	750 ns	400 ns	400 ns	600 ns

Table 4-11. Multiply Timing Comparison

MULTIPLY	'AS888 32-BIT	'AS888 16-BIT	Z8001	8086-1	80286	68000L
Size	32 × 32	16 × 16	16 × 16	16 × 16	16 × 16	16 × 16
No. of cycles	35	19	70	128	21	≤74
Clock rate	11.11 MHz	10.98 MHz	4 MHz	10 MHz	10 MHz	8 MHz
Total time	3.150 μs	1.729 μs	17.5 μs	12.8 μs	2.1 μs	≤9.25 μs

5. Floating-Point System Design

Bit-slice processor architecture addresses the problem of optimizing system performance while allowing the user to balance hardware complexity against software flexibility. Bit-slice systems usually operate at or near the speed of the most primitive of programmable processors, the PROM state sequencer. Of course, bit-slice architecture incorporates circuitry dedicated not only to sequencing, but also data processing (ALU) operations. In keeping with the trend of these programmable devices to track the speed of fast discrete hardware, the 'AS888 8-bit slice ALU and 'AS890 microsequencer have been produced in Advanced Schottky bipolar technology. In addition to sheer speed, the components feature greater density (2 micron geometry) for greater functionality (more special purpose circuitry on board). The impact will be faster, more powerful systems in applications which previously pushed the limits of bit-slice processors.

Consider an application in which bit-slice architecture has dominated for years: CPU design. The microprogrammed CPU itself spans a spectrum of uses ranging from general purpose minicomputers to compact airborne computers. A specific example which illustrates various facets of design using the 'AS888 and 'AS890 is a CPU with a floating-point utility to compute $\sin(x)$.

The design process can be subject to many influences, including personal preference, available development tools, peculiarities of the application, and constraints from the user, customer or manufacturing environment. No hard and fast design rules could be applied universally, but most designers will start with a specific plan in mind.

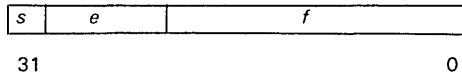
The goal of this example is to produce the hardware and microprogram which will implement the $\sin(x)$ function in floating-point arithmetic. Before the microprogram can be assembled, the hardware must be defined since the fields of the microinstruction are dedicated to specific hardware once the microinstruction register is hardwired to the devices it controls. Since the final architecture chosen depends on tradeoffs between implementing certain operations in hardware or software, critical applications will require that a cursory analysis of the software be made before the hardware is cast in concrete. Attempting to develop microcode for a tentative architecture will force the issue on which operations are better suited for hardware. Before the architecture or the microprogram requirements can be known, the algorithms which describe the application processes must be defined. Once an algorithm is formulated it can be broken down into operations involving variable and constant quantities. The variables can be assigned to registers and then the algorithm can be translated into a microprogram. The following steps illustrate the plan for this CPU design example incorporating a floating-point $\sin(x)$ utility:

- Step 1: Choose a floating-point number system
- Step 2: Choose an algorithm for approximating $\sin(x)$
- Step 3: Make 'AS888 register assignments
- Step 4: Substitute registers for variables in the algorithm
- Step 5: Decompose steps of the algorithm into simple operations
- Step 6: Translate into 'AS888/890 operations; identify subroutines
- Step 7: Translate subroutines into 'AS888/890 operations
- Step 8: Evaluate tradeoffs and block diagram the hardware
- Step 9: Define microinstruction fields during detailed hardware design
- Step 10: Assemble the microprogram

5.1 Choose a Floating-Point Number System

An IEEE floating-point format will be chosen for this example for portability of data and software. It is important to note that the IEEE defines many standards in arithmetic processing, but for simplicity this example will encompass only number format. Furthermore, while several formats are IEEE compatible, only the basic single-precision format will be considered.

The IEEE basic single-precision format is defined as a 32-bit representation in which the component fields are a 1-bit sign s , an 8-bit biased exponent e and a 23-bit fraction f which are assembled in the following order:



The quantity is evaluated as $(-1)^s 2^{e-127} (1.f)$. Not-a-number, zero and infinity have special representations. The one preceding the binary point is implied and is called the implicit one or implicit bit. It coincides with the fact that the digits are normalized (left justified).

5.2 Choose an Algorithm for Sin(x)

Many algorithms are discussed in the literature for approximating useful quantities like $\sin(x)$. Literature research is a good place to start to familiarize oneself with various algorithms and tradeoffs for a particular application. Computer simulation is also useful to compare algorithms for speed and accuracy. R.F. Ruckdeschel in *BASIC Scientific Subroutines*, Vol. 1 (BYTE, McGraw-Hill Publications Co. New York, N.Y., 1981, pp. 159–191) discusses tradeoffs and provides a simulation in BASIC for a $\sin(x)$ algorithm. An adaptation of this material has been chosen for this example:

A) Reduce angle range to first quadrant. ($0 \leq x \leq \pi/2$)

B) Compute $\sin(x) = \sum_{n=0}^6 A_n x^{2n-1}$. The coefficients are:

Coefficient	Decimal	IEEE hex
A ₀	1.000000	3F80 0000
A ₁	-0.1666667	BE2A AAAD
A ₂	0.008333333	3C08 8888
A ₃	-0.0001984127	B950 0D01
A ₄	0.000002755760	3638 EF99
A ₅	-0.00000002507060	B2D7 5AD5
A ₆	0.0000000001641060	2F34 6FBC

The algorithm can be implemented in the following steps:

- A) Reduce angle range to first quadrant. ($0 \leq x \leq \pi/2$)
- 1) SIGN = SGN(x)
 - 2) ABSX = $\|x\|$
 - 3) XNEW = ABSX - $2\pi \times \text{INT}(\text{ABSX}/2\pi)$
 - 4) If XNEW > π then SIGN = -SIGN and XNEW = XNEW - π
 - 5) If XNEW > $\pi/2$ then XNEW = $\pi - \text{XNEW}$

where

$$\text{SGN}(x) = \begin{cases} +1 & \text{if } x \geq 0 \\ -1 & \text{if } x < 0 \end{cases}$$

INT(x) = integer function

B) Compute $\sin(x) \approx \sum_{n=0}^6 A_n x^{2n-1}$.

- 1) Let XSQR = XNEW²; INITIALIZE SINX = 0
- 2) Do i=6 to 1 step -1
 $\text{SINX} = \text{XSQR} \times \text{SINX} + A(i)$
 Enddo
- 3) SINX = SIGN \times XNEW \times SINX

Step B-2 computes the summation in a geometric series for economy. The major difference between steps A and B is that A requires more diverse ALU operations while B uses only multiplication and addition recursively.

5.3 Make 'AS888 Register Assignments

Just as in assembly language programming, registers must be allocated for variables. Using R_n to denote the 'AS888 register whose address is n, where $0 \leq n \leq F$ (hex), the following register assignments can be made:

R0 = X
 R1 = SIGN
 R2 = ABSX
 R3 = XNEW
 R4 = XSQR
 R5 = SINX

The following constants can also be defined:

Constant	Decimal	IEEE hex
PI = π	3.141593	4059 0FDB
PIOVR2 = $\pi/2$	1.570797	3FC9 0FDB
2PI = 2π	6.283185	40C9 0FDB
1OVR2PI = $1/2\pi$	0.159155	3E22 F981

5.4 Substitute Registers for Variables in the Algorithm

Now the algorithm can be rewritten with registers replacing variables:

A) Reduce angle range to first quadrant ($0 \leq x \leq \pi/2$).

- 1) $R1 = \text{SGN}(R0)$
- 2) $R2 = \|R0\|$
- 3) $R3 = R2 - 2\pi \times \text{INT}(R2/2\pi)$
- 4) If $R3 > \pi$ then $R1 = -R1$; $R3 = R3 - \pi$
- 5) If $R3 > \pi/2$ then $R3 = \pi - R3$

B) Compute $\sin(x) = \sum_{n=0}^6 A_n x^{2n-1}$.

- 1) Let $R4 = R0^2$; INITIALIZE $R5 = 0$
- 2) Do $i=6$ to 1 step -1
 $R5 = R4 \times R5 + A(i)$
 Enddo
- 3) $R5 = R1 \times R0 \times R5$

Since various references to constants are made, it is probably best to load constants as needed rather than attempt to allocate registers for them. Constants can be loaded from a constant field in the microinstruction or from ROM. The tradeoff is 32 bits by 16K of micromemory versus 32 bits by the number of constants (typically less than 16K). For this example, it will be assumed that a constant field in the microinstruction is acceptable.

5.5 Decompose Steps in the Algorithm into Simple Operations

The $\sin(x)$ function can be microprogrammed as a subroutine; let FSIN be its entry address. R0 would be loaded with x before FSIN were called. Upon return, R5 would contain $\sin(x)$. Now decompose the steps in the algorithm into simple arithmetic and logical operations. Other operations can be left as functions to be defined later.

FSIN: SUBROUTINE

; A) Reduce angle range to first quadrant. ($0 \leq x \leq \pi/2$)

$R1 = \text{SGN}(R0)$; 1) Let $R1 = \text{Sign of } R0$

$R2 = \text{ABS}(R0)$; 2) $R2 = \|R0\|$

$R3 = R2 * 10VR2PI$; 3) $R3 = R2 - 2\pi * \text{INT}(R2/2\pi)$

$R3 = \text{INT}(R3)$;

$R3 = R3 * 2PI$;

$R3 = R2 - R3$;

$Y = R3 - PI$; 4) If $R3 > \pi$,

Jump if Negative to Step A-5 ;

$R1 = -R1$; then $R1 = -R1$;

$R3 = R3 - PI$; $R3 = R3 - \pi$

$Y = PI - R3$;

Jump if Negative to Step B-1 ; 5) If $R3 > \pi/2$

$R3 = PI - R3$; then $R3 = \pi - R3$

; B) Compute $\sin(x) \approx \sum_{n=0}^6 A_n x^{2n-1}$

```

R4 = R0 * R0          ; 1) Let R4 = R02. Let R5 = 0
R5 = 0                ;
;
R5 = R4 * R5          ; 2) Do i=6 to 1 step -1
R5 = R5 + A6          ;   R5 = R4 × R5 + A(i)
R5 = R4 * R5          ;   Enddo
R5 = R5 + A5          ;
R5 = R4 * R5          ;   (To implement a loop,
R5 = R5 + A4          ;   use an 'AS890 counter
R5 = R4 * R5          ;   to index a memory containing
R5 = R5 + A3          ;   the constants.)
R5 = R4 * R5          ;
R5 = R5 + A2          ;
R5 = R4 * R5          ;
R5 = R5 + A1          ;
R5 = R4 * R5          ;
R5 = R5 + A0          ;
;
R5 = R0 * R5          ; 3) R5 = R1 × R0 × R5
R5 = R5 * R1 : RETURN ;

```

END SUBROUTINE

5.6 Translate into 'AS888/890 Instructions; Identify Subroutines

The simplified steps of the algorithm can be represented fairly easily as 'AS888/890 instructions. Necessary functions (and suggested names) can be identified by inspection as:

- 1) FMUL — Floating-point multiplication
- 2) FADD — Floating-point addition
- 3) FINT — Floating-point integer conversion
- 4) FINV — Floating-point additive inverse (to subtract using FADD)
- 5) FABS — Floating-point absolute value
- 6) FSGN — Floating-point sign test
- 7) FCHS — Floating-point change of sign (to multiply by SIGN)

"Function" in this context refers to a special operation regardless of how it is coded. In fact, FMUL and FADD are fairly complex and require detailed explanation. FINV, FABS, FSGN and FCHS are single instruction operations that mask or mask and test. FINT requires several inline instructions or a subroutine and will be left to the interested reader as an exercise. Now the steps of the algorithm can be translated into 'AS888/890 operations which include references to these functions.

FSIN: SUBROUTINE

```
; A) Reduce angle range to first quadrant. (0 ≤ x ≤ π/2)
    R1 = FSGN(R0)           ; Get sign bit (MSB)
    R2 = FABS(R0)          ; Take absolute value (clear MSB)
    R3 = FMUL(R2,10VR2PI)  ; Multiply register and constant
    R3 = FINT(R3)          ; Floating-point integer conversion
    R3 = FMUL(R3,2PI)      ; Multiply register and constant
    R3 = FADD(R2,INV(R3))  ; Subtract registers by adding inverse
    Y = FADD(R3,NEGPI) : TEST NEG ; Subtract by adding negative constant
    JT SIN1                ; Jump if true (jump if negative)
    R1 = FINV(R1)          ; Complement sign of R1
    R3 = FADD(R3,NEGPI)    ; Subtract by adding negative constant
SIN1: Y = PIOVR2 - R3 : TEST NEG ; Subtract to compare (don't store)
    JT SIN2                ; Jump if true (jump if negative)
    R3 = FADD(PI,FINV(R3)) ; Subtract by adding negative register
```

```
; B) Compute  $\sin(x) \approx \sum_{n=0}^6 A_n X^{2n-1}$ 
```

```
SIN2: R4 = FMUL(R0,R0)      ; Square by multiplying
    R5 = A6                 ; Initialize series
    R5 = FMUL(R4,R5)       ; Multiply registers
    R5 = FADD(R5,A5)       ; Add coefficient
    R5 = FMUL(R4,R5)       ; Multiply registers
    R5 = FADD(R5,A4)       ; Add coefficient
    R5 = FMUL(R4,R5)       ; Multiply registers
    R5 = FADD(R5,A3)       ; Add coefficient
    R5 = FMUL(R4,R5)       ; Multiply registers
    R5 = FADD(R5,A2)       ; Add coefficient
    R5 = FMUL(R4,R5)       ; Multiply registers
    R5 = FADD(R5,A1)       ; Add coefficient
    R5 = FMUL(R4,R5)       ; Multiply registers
    R5 = FADD(R5,A0)       ; Add coefficient
    R5 = FMUL(R0,R5)       ; Multiply registers
    R5 = FCHS(R5,R1) : RETURN ; Change MSB of R5 to MSB of R1
```

END SUBROUTINE

This contrived language has a syntax which may be suitable for a source program. For the sake of illustration, it can be assumed that the microassembler recognizes this particular syntax. The series was computed inline instead of using a loop since it is relatively short. If a loop were used, a means of indexing the constants would be required.

5.7 Expand Subroutines into 'AS888/890 Operations

FMUL and FADD algorithms can now be expanded. Since they are called extensively from FSIN, they are more critical to the efficiency of the final design. Wherever possible, it is desirable to reduce the execution time of both in order to maintain efficiency.

5.7.1 Floating-Point Multiplication

Let M1 be the multiplier and M2 be the multiplicand whose product is P. Let the sign, exponent and fraction fields of their IEEE representation be:

M1 : |S1|E1|F1|
M2 : |S2|E2|F2|
P : |S3|E3|F3|

P is found by multiplying mantissas (fraction plus implicit one) and adding exponents. Since M1 and M2 are normalized, the range of $1.F1 \times 1.F2$ is

$$1.00\dots0 \leq 1.F1 \times 1.F2 \leq 11.1\dots10$$

The implicit bit may “overflow” into bit position 24. This type of overflow must be detected so that the result can be normalized. Normalization requires right shifting the result of $1.F1 \times 1.F2$ and incrementing E3. The implicit bit is then cleared when S3, E3 and M3 are packed to form P. The floating-point multiplication algorithm may then be defined as follows:

- 1) Unpack M1 into signed fraction (SF1) and exponent (E1)
- 2) Set the implicit bit in SF1
- 3) Unpack M2 into signed fraction (SF2) and exponent (E2)
- 4) Set the implicit bit in SF2
- 5) Perform $SF3 = SF1 \times SF2$ using signed integer multiplication
- 6) Perform $E3 = E1 + E2$
- 7) Test SF3 for overflow into bit 24
- 8) If true, then increment E3 and right shift SF3
- 9) Clear the implicit bit in SF3
- 10) Pack E3 and SF3 to get P

As before, the steps of this algorithm can be broken down into simpler operations:

- 1) Unpack M1 into signed fraction (SF1) and exponent (E1)
 $E1 = \text{FEXP}(M1)$
 $SF1 = \text{FRAC}(M1)$
- 2) Set the implicit bit in SF1
 $SF1 = SF1 \text{ OR BIT23}$
- 3) Unpack M2 into signed fraction (SF2) and exponent (E2)
 $E2 = \text{FEXP}(M2)$
 $SF2 = \text{FRAC}(M2)$
- 4) Set the implicit bit in SF2
 $SF2 = SF2 \text{ OR BIT23}$
- 5) Perform $SF3 = SF1 \times SF2$ using signed integer multiplication
 $SF3 = \text{IMUL}(SF1, SF2)$
- 6) Perform $E3 = E1 + E2$
 $E3 = E1 + E2$
- 7) Test SF3 for overflow into bit 24
TEST (SF3 AND BIT24)
JUMP IF FALSE to step 9
- 8) If true, then increment E3 and right shift SF3
INC E3
 $SF3 = \text{RSHFT}(SF3)$

9) Clear the implicit bit in SF3.
 SF3 = SF3 AND NOT _BIT23

10) Pack E3 and SF3 to get P
 P = SF3 OR E3

FEXP, FRAC, testing bit 24 and setting/clearing bit 23 are all mask operations that translate into single 'AS888 instructions. The integer multiplication (IMUL) is simply the multiplication algorithm supported by the 'AS888 instruction set. No significant hardware features are required to do floating-point multiplication, nor are any subroutines required to support it.

Register assignments can now be made as before. Since FSIN uses registers in the lower half of the register file, it might be preferable to restrict FMUL to the upper registers. For example:

```
RF = P
RE = M1, F1, SF1
RD = M2, F2, SF2
RC = E1
RB = E2
```

RE and RD can share variables that need not be preserved. Using this assignment, FMUL computes RF = FMUL(RE,RD). RE and RD must be loaded prior to calling FMUL and RF must be stored upon return. By substituting registers for variables and reorganizing operations in the FMUL algorithm to better fit 'AS888/890 operations the following source program may be created:

```
FMUL: SUBROUTINE
      RC = FEXP(RE)           ; Unpack M1 into exponent
      RE = FRAC(RE)          ; and fraction
      RE = RE OR BIT23       ; Set implicit bit
      MQ = SMTC(RE)          ; Prepare to multiply

      RB = FEXP(RD)           ; Unpack M2 into exponent
      RD = FMAG(RD)          ; and fraction
      RD = RD OR BIT23       ; Set implicit bit
      RD = SMTC(RD)          ; Prepare to multiply

      RE = 0 : RCA = #22d     ; Initialize to multiply
      RE = SMULI RD : LOOP RCA ; Integer multiplication iteration
      RE = SMULT RD           ; Final step in signed multiply
      Y = TBO(RE,BIT1):BYTE = #0100b:TEST Z ; Test "overflow"
      JF FMUL1                ; Jump if false (exponent ok)

      INEX(RC)                ; Increment exponent: add 00800000
      RE = SRA(RE)            ; Shift fraction to normalize

FMUL1:RC = RC + RB : TEST CARRY ; Add exponents and test carry
      JT ERROR                ; Jump if carry true to handler

      RE = SMTC(RE)           ; Get sign magnitude fraction
      RE = RE AND #807F_FFFFh ; Clear implicit bit
      RF = RE OR RC : RETURN   ; Pack fraction and exponent
```

5.7.2 Floating-Point Addition

The floating-point addition algorithm (FADD) is slightly more complex than FMUL, since the two addends will usually not have the same exponent. Therefore the smaller (absolute value) addend must first be chosen by comparing exponents. Then it must be denormalized to align its digits with the digits of the larger addend. In other words, the two addends must have the same exponent before their fractions can be added. This process can be described by the following algorithm:

- 1) Unpack A1 to get SF1 and E1
- 2) Set implicit bit in SF1
- 3) Unpack A2 to get SF2 and E2
- 4) Set implicit bit in SF2
- 5) If $E2 > E1$ then go to step 9
($|A1| \leq |A2|$)
- 6) Let $DIFF = E1 - E2$
- 7) Do $i = 1$ to $DIFF$
 $SF2 = RSHFT(SF2)$ (Arithmetic right shift)
 Enddo
- 8) Let $E3 = E1$, go to step 12
($|A2| > |A1|$)
- 9) Let $DIFF = E2 - E1$
- 10) Do $i = 1$ to $DIFF$
 $SF1 = RSHFT(SF1)$ (Arithmetic right shift)
 Enddo
- 11) Let $E3 = E2$
- 12) $SF3 = SF1 + SF2$
- 13) Test "overflow" into bit 24
- 14) Jump if false to step 17
- 15) Increment exponent $E3$
- 16) Normalize signed fraction with right arithmetic shift
- 17) Clear implicit bit
- 18) Pack: $SUM = SF3$ or $E3$
- 19) Return

Register assignments for variables must now be made. Since FSIN uses registers in the lower half of the 'AS888 register file, it is necessary to use the upper registers:

```
RF = SUM
RE = A1, F1, SF1
RD = A2, F2, SF2
RC = E1
RB = E2
```

By slightly reorganizing the sequence to better fit 'AS888/890 operations, the following microprogram to perform FADD can be created:

FADD: SUBROUTINE

- ```
; 1) Unpack A1 to get SF1 and E1
 RC = FEXP(RE) ; Get exponent (E1)
 RE = FRAC(RE) ; Get signed fraction (SF1)

; 2) Set implicit bit in SF1
 MQ = RE OR BIT23 ; Set implicit bit
 RE = SMTC(RE) ; Convert to two's complement
```



```

; 3) Unpack A2 to get SF2 and A2
 RB = FEXP(RD) ; Get exponent (E2)
 RD = FRAC(RD) ; Get signed fraction (SF2)

; 4) Set implicit bit in SF2
 RD = RD OR BIT23 ; Set implicit bit
 RD = SMTC(RD) ; Convert to two's complement

; 5) If E2 > E1 then go to step 9
 RF = RC - RB : TEST NEGATIVE ; Compare A2 from A1
 JT FADD1 : RCA = #8 ; Jump if E2 > E1; set up loop count

; 6) Let DIFF = E1 - E2.
 Y/RF = SLC(RF) : LOOP RCA ; Rotate 8 times to get difference
 RCA = Y/RF ; Load difference in loop counter

; 7) Do i = 1 to DIFF
 SF2 = RSHFT(SF2)
 Enddo
 RD = SRA(RD) : LOOP RCA ; Orient digits of smaller addend

; 8) Let E3 = E1, go to step 12
 RB = RC : JUMP FADD2 ; Swap registers and branch

; 9) Let DIFF = E2 - E1
FADD1: RF = NOT(RF) ; Complement result of E1 - E2
 Y/RF = SLC(RF) : LOOP RCA ; Shift 8 times to get DIFF
 RCA = Y/RF ; Load DIFF in loop counter

;10) Do i = 1 TO DIFF
 SF1 = RSHFT(SF1)
 Enddo
 RE = SRA(RE) : LOOP RCA ; Align SF1 with SF2

;11) Let E3 = E2 (no instruction required - RB already has E2 in it)

;12) SF3 = SF1 + SF2
FADD2: RF = RD + RE ; Add
 RF = SMTC(RF) ; Convert to sign-magnitude

;13) Test "overflow" into bit 24
 RF = TBO (RF, BIT24) ; Check for normalization

;14) Jump if false to step 17
 JF FADD3 ; If so, finish and exit

;15) Else increment exponent
 INC RB : TEST NEG ; Test for exponent overflow

;16) Normalize signed fraction
 RF = SRA(RF) : JT ERROR ; Jump to error handler if overflow

;17) Clear implicit bit
FADD3: RF = SETO (RF, BIT23) ; Reset bit 23 of RF

;18) Pack: SUM = SF3 OR E3
 RF = RF OR RB : RETURN ; Or signed fraction and exponent

```

There is an important consequence of FADD which impacts the hardware. Since the number of shifts required to denormalize the small addend is data dependent (computed in the ALU) it is necessary to provide a path between the ALU Y bus and the 'AS890 DRA bus. All the other operations are simple 'AS888/890 instructions, including the FRAC and FEXP mask operations discussed during the development of FMUL. ERROR is a floating-point overflow error handler.

## 5.8 Evaluate Tradeoffs and Block Diagram the Hardware

A rough estimate of the FSIN worst case execution time can be arrived at by making the following observations about FSIN, FMUL and FADD:

### FMUL

integer recursion  $\approx$  22 cycles  
other instructions  $\approx$  18 cycles  
total  $\approx$  40 cycles

### FADD

denormalization  $\approx$  23 cycles  
other instructions  $\approx$  25 cycles  
total  $\approx$  50 cycles

### FSIN

number of calls to FMUL = 12  
number of calls to FADD = 11  
number of other cycles  $\approx$  10

Approximate worst case total =  $10 + (12 \times 40) + (11 \times 50) = 1040$  cycles. At 50 nanoseconds per cycle, this requires approximately 52 microseconds. There are few improvements that could be made in hardware to speed this time, except perhaps the addition of a flash multiplier which would reduce the integer computation by about 20 cycles (an overall reduction of about two percent). A barrel shifter could have the same benefit during floating-point addition for a total reduction of about 4 percent. For the sake of simplicity, it will be assumed that 52 microseconds is acceptable for the  $\sin(x)$  computation.

Another issue which must be considered is the problem of loading the 'AS888 and 'AS890 with constants. A slight materials cost reduction might be realized by storing constants in table PROMs rather than in control store memory. An interesting use of the DRA and DRB ports on the 'AS890 would be to use the output of RCA or RCB to index data in the constant PROM. This would allow long series to be implemented in loop form rather than the inline method used in FSIN. Once again, the constant PROM will not be implemented for the sake of simplicity.

Now the architecture can be designed to meet the requirements identified throughout this analysis:

- 1) A path between the 'AS888 Y bus and the 'AS890 DRA bus.
- 2) A path between the microinstruction register and the 'AS890 DRA bus for loading loop counts and branch addresses.
- 3) A path between the microinstruction register and the 'AS888 Y bus for loading constants.
- 4) Independent control of  $\overline{SIOO}$  in each 'AS888 slice to allow bit/byte instructions.
- 5) A status register to store 'AS888 status for testing.
- 6) A status mux to test the 'AS888 status, bit 23 of the 'AS888 Y bus, bit 24 of the 'AS888 Y bus and hardwired 0 and 1.

A system having these features is illustrated in Figure 5.1.

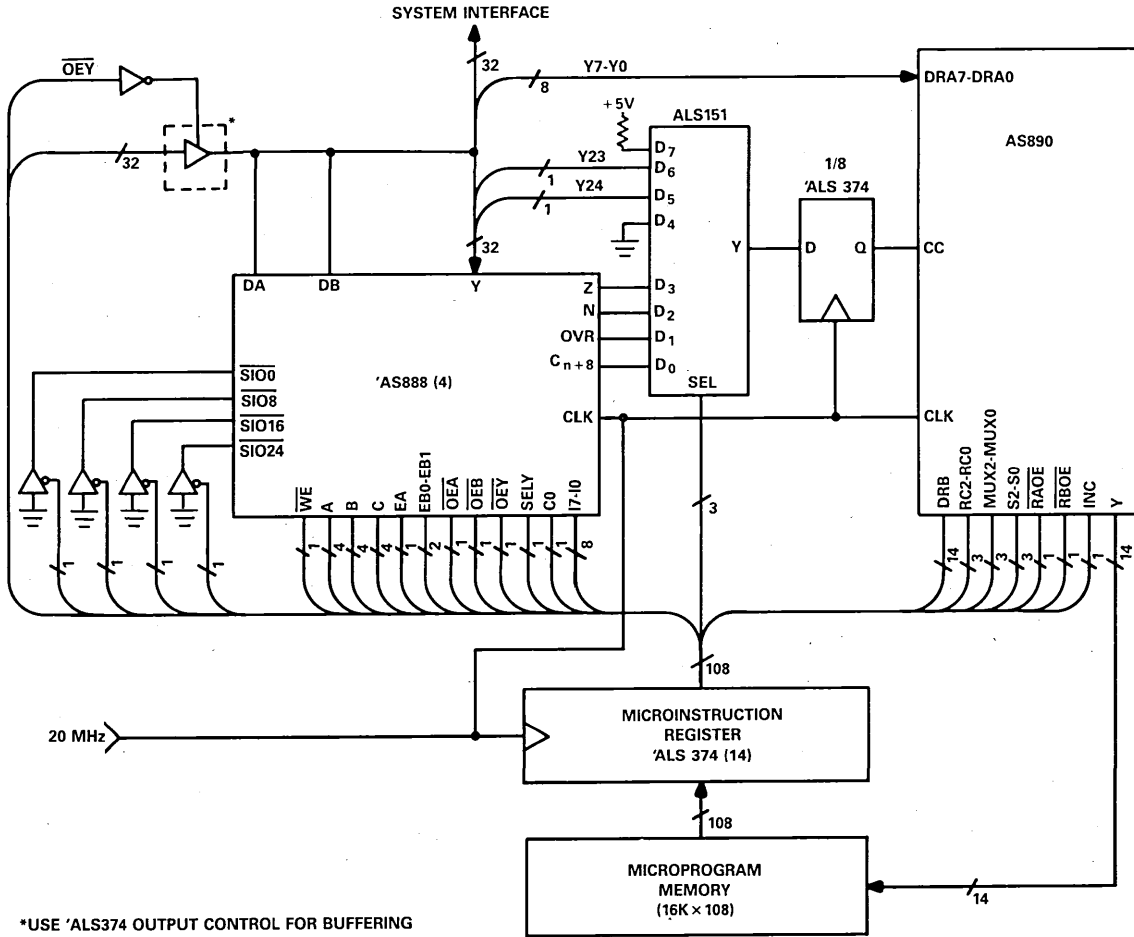


Figure 5-1. Block Diagram of Floating-Point Processor

### **5.9 Define Microinstruction Fields During Detailed Hardware Design**

The detailed hardware design will produce a wiring diagram that fixes the position within the microinstruction of each of the various control signals that are connected from the microinstruction register to the 'AS888, 'AS890, status mux and any other special hardware. Once this design is complete it is possible for the assembler to sort the control bits of each instruction so that they will be properly oriented when the microprogram is installed in the target system.

### **5.10 Assemble the Microprogram**

TI is currently developing an 'AS888/890 microassembler. Several microassemblers are commercially available, and many users prefer to write their own. The microprogram shown in Table 5-1 was hand-assembled, but has a syntax that is suitable for interpretation by a user-written assembler.

Table 5.1. Floating Point Sin(x) Microprogram

0000 SIN: \* R1 = FSGN(R0)  
 R1 = R0 AND #8000 0000h

0001 \* R2 = FABS(R0)  
 R2 = R0

0002 R2 = R0 SET0 #80h : BYTE = #1000b

0003 \* R3 = FMUL(R2,1OVR2PI)  
 RE = R2

0004 RD = #3EA2 F984h

0005 JSR FMUL

0006 R3 = RF

0007 \* R3 = FINT(R3)  
 RF = R3

0008 JSR FINT [EXERCISE FOR READER]

0009 R3 = RF

000A \* R3 = FMUL(R3,2PI)  
 RE = R3

000B RD = #40C9 0FDBh

000C JSR FMUL

000D R3 = RF

000E \* R3 = FADD(R2,INV(R3))  
 RE = R2

000F RD = R5 XOR #8000 0000h

0010 JSR FADD

0011 R3 = RF

| WE | A3-A0 | B3-B0 | C3-C0 | EA | EB1-EB0 | OEA | OEB | OEY | SELY | Cn | I7-I0 | 32-bit Constant | SIO0 | SIO8 | SIO16 | SIO24 | RC2-RC0 MUX2-MUX0 | S2-S0 | DRB13-DRB0 | RAOE | RBOE | INCC | SEL |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|----|-------|-------|-------|----|---------|-----|-----|-----|------|----|-------|-----------------|------|------|-------|-------|-------------------|-------|------------|------|------|------|-----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0  | 0     | X     | 1     | 0  | 2       | 1   | 1   | 1   | 0    | 0  | F     | A               | 8    | 0    | 0     | 0     | 0                 | 0     | 0          | 0    | 0    | 0    | 0   | 0 | 1 | 1 | 1 | 1 | 0 | 2 | 7 | X | X | X | X | 1 | 1 | 1 | 7 |   |
| 0  | 0     | X     | 2     | 0  | X       | 1   | 1   | 1   | 0    | 0  | F     | 6               | X    | X    | X     | X     | X                 | X     | X          | X    | X    | X    | X   | X | X | 1 | 1 | 1 | 1 | 0 | 2 | 7 | X | X | X | X | 1 | 1 | 1 | 7 |
| 0  | 0     | 2     | 8     | 0  | 0       | 1   | 1   | 1   | 0    | 0  | 1     | 8               | X    | X    | X     | X     | X                 | X     | X          | X    | X    | X    | X   | X | X | 1 | 1 | 1 | 0 | 0 | 2 | 7 | X | X | X | X | 1 | 1 | 1 | 7 |
| 0  | 2     | X     | E     | 0  | X       | 1   | 1   | 1   | 0    | 0  | F     | 6               | X    | X    | X     | X     | X                 | X     | X          | X    | X    | X    | X   | X | X | 1 | 1 | 1 | 1 | 0 | 2 | 7 | X | X | X | X | 1 | 1 | 1 | 7 |
| 0  | X     | X     | D     | X  | X       | 1   | 1   | 1   | X    | F  | F     | 3               | E    | A    | 2     | F     | 9                 | 8     | 4          | 1    | 1    | 1    | 1   | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 2 | 7 | X | X | X | X | 1 | 1 | 1 | 7 |
| 1  | X     | X     | X     | X  | 1       | 1   | X   | X   | F    | F  | X     | X               | X    | X    | X     | X     | X                 | X     | X          | X    | X    | X    | X   | X | X | 1 | 1 | 1 | 1 | 0 | 1 | 4 | 0 | 0 | 6 | 0 | 1 | 1 | 1 | 7 |
| 0  | F     | X     | 3     | 0  | X       | 1   | 1   | 1   | 0    | 0  | F     | 6               | X    | X    | X     | X     | X                 | X     | X          | X    | X    | X    | X   | X | X | 1 | 1 | 1 | 1 | 0 | 2 | 7 | X | X | X | X | 1 | 1 | 1 | 7 |
| 0  | 3     | X     | F     | 0  | X       | 1   | 1   | 1   | 0    | 0  | F     | 6               | X    | X    | X     | X     | X                 | X     | X          | X    | X    | X    | X   | X | X | 1 | 1 | 1 | 1 | 0 | 2 | 7 | X | X | X | X | 1 | 1 | 1 | 7 |
| 1  | X     | X     | X     | X  | 1       | 1   | X   | X   | F    | F  | X     | X               | X    | X    | X     | X     | X                 | X     | X          | X    | X    | X    | X   | X | X | 1 | 1 | 1 | 1 | 0 | 1 | 4 | . | . | . | . | 1 | 1 | 1 | 7 |
| 0  | F     | X     | 3     | 0  | X       | 1   | 1   | 1   | 0    | 0  | F     | 6               | X    | X    | X     | X     | X                 | X     | X          | X    | X    | X    | X   | X | X | 1 | 1 | 1 | 1 | 0 | 2 | 7 | X | X | X | X | 1 | 1 | 1 | 7 |
| 0  | 3     | X     | E     | 0  | X       | 1   | 1   | 1   | 0    | 0  | F     | 6               | X    | X    | X     | X     | X                 | X     | X          | X    | X    | X    | X   | X | X | 1 | 1 | 1 | 1 | 0 | 2 | 7 | X | X | X | X | 1 | 1 | 1 | 7 |
| 0  | X     | X     | D     | X  | X       | 1   | 1   | 1   | 0    | X  | F     | F               | 4    | 0    | C     | 9     | 0                 | F     | D          | B    | 1    | 1    | 1   | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 2 | 7 | X | X | X | X | 1 | 1 | 1 | 7 |
| 1  | X     | X     | X     | X  | 1       | 1   | X   | X   | F    | F  | X     | X               | X    | X    | X     | X     | X                 | X     | X          | X    | X    | X    | X   | X | X | 1 | 1 | 1 | 1 | 0 | 1 | 4 | 0 | 0 | 6 | 0 | 1 | 1 | 1 | 7 |
| 0  | F     | X     | 3     | 0  | X       | 1   | 1   | 1   | 0    | 0  | F     | 6               | X    | X    | X     | X     | X                 | X     | X          | X    | X    | X    | X   | X | X | 1 | 1 | 1 | 1 | 0 | 2 | 7 | X | X | X | X | 1 | 1 | 1 | 7 |
| 0  | 2     | X     | E     | 0  | X       | 1   | 1   | 1   | 0    | 0  | F     | 6               | X    | X    | X     | X     | X                 | X     | X          | X    | X    | X    | X   | X | X | 1 | 1 | 1 | 1 | 0 | 2 | 7 | X | X | X | X | 1 | 1 | 1 | 7 |
| 0  | 5     | X     | D     | 0  | 2       | 1   | 1   | 1   | 0    | 0  | F     | 9               | 8    | 0    | 0     | 0     | 0                 | 0     | 0          | 0    | 0    | 0    | 0   | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 2 | 7 | X | X | X | X | 1 | 1 | 1 | 7 |
| 1  | X     | X     | X     | X  | 1       | 1   | X   | X   | F    | F  | X     | X               | X    | X    | X     | X     | X                 | X     | X          | X    | X    | X    | X   | X | X | 1 | 1 | 1 | 1 | 0 | 1 | 4 | 0 | 0 | 7 | 4 | 1 | 1 | 1 | 7 |
| 0  | F     | X     | 3     | 0  | X       | 1   | 1   | 1   | 0    | 0  | F     | 6               | X    | X    | X     | X     | X                 | X     | X          | X    | X    | X    | X   | X | X | 1 | 1 | 1 | 1 | 0 | 2 | 7 | X | X | X | X | 1 | 1 | 1 | 7 |

Table 5.1. Floating Point Sin(x) Microprogram (continued)

```

* Y = FADD(R2,NEGPI)
0012 RE = R2
0013 RD = #C059 0FDBh
0014 JSR FADD
0015 Y = RF : TEST NEG
0016 JT SIN1

* R1 = FINV(R1)
0017 R1 = R1 XOR #8000 0000h

* R3 = FADD(R3,NEGPI)
0018 RE = R3
0019 RD = #C059 0FDBh
001A JSR FADD
001B R3 = RF

* SIN1: Y = FADD(PIOVR2,INV(R3)) : TEST NEG
001C RE = #3FC9 0FDBh
001D RD = R3 XOR #8000 0000h
001E JSR FADD
001F Y = RF : TEST NEG
0020 JT SIN2

* R3 = FADD(PI,FINV(R3))
0021 RE = #4059 0FDBh
0022 RD = R3 XOR #8000 0000h
0023 JSR FADD
0024 R3 = RF

* SIN2: R4 = FMUL(R0,R0)
0025 SIN2: RE = R0
0026 RD = R0
0027 JSR FMUL
0028 R4 = RF

```

| WE   | A3-A0 | B3-B0 | C3-C0 | EA | EB1-EB0 | OEA | OEB | OEC | SELY | Cn | I7-I0 | 32-bit Constant | S100 | S108 | S106 | S104 | RC2-RC0 | MUX2-MUX0 | S2-S0 | DRB13-DRB0 | RAOE | RBOE | INC | SEL |   |   |   |   |   |   |
|------|-------|-------|-------|----|---------|-----|-----|-----|------|----|-------|-----------------|------|------|------|------|---------|-----------|-------|------------|------|------|-----|-----|---|---|---|---|---|---|
| 0012 | 0     | 2     | X     | E  | 0       | X   | 1   | 1   | 1    | 0  | 0     | F6              | X    | X    | X    | X    | X       | X         | X     | 0          | 2    | 7    | X   | X   | X | 1 | 1 | 1 | 7 |   |
| 0013 | 0     | X     | X     | D  | X       | X   | 1   | 1   | 1    | 0  | X     | F               | F    | C    | 0    | 5    | 9       | 0         | F     | D          | B    | 1    | 1   | 1   | 1 | 1 | 1 | 1 | 7 |   |
| 0014 | 1     | X     | X     | X  | X       | X   | 1   | 1   | 1    | X  | X     | F               | F    | X    | X    | X    | X       | X         | X     | 1          | 1    | 1    | 1   | 1   | 1 | 1 | 1 | 1 | 7 |   |
| 0015 | 1     | F     | X     | X  | 0       | X   | 1   | 1   | 0    | 0  | 0     | F6              | X    | X    | X    | X    | X       | X         | X     | 1          | 1    | 1    | 1   | 1   | 1 | 1 | 1 | 1 | 1 | 2 |
| 0016 | 1     | X     | X     | X  | X       | X   | 1   | 1   | 1    | X  | X     | F               | F    | X    | X    | X    | X       | X         | X     | 1          | 1    | 1    | 1   | 1   | 1 | 1 | 1 | 1 | 1 | 7 |
| 0017 | 0     | 1     | X     | 1  | 0       | 2   | 1   | 1   | 1    | 1  | 0     | F9              | 8    | 0    | 0    | 0    | 0       | 0         | 0     | 0          | 0    | 1    | 1   | 1   | 1 | 1 | 1 | 1 | 1 | 7 |
| 0018 | 0     | 3     | X     | E  | 0       | X   | 1   | 1   | 1    | 0  | 0     | F6              | X    | X    | X    | X    | X       | X         | X     | 1          | 1    | 1    | 1   | 1   | 1 | 1 | 1 | 1 | 1 | 7 |
| 0019 | 0     | 3     | X     | D  | X       | X   | 1   | 1   | 1    | X  | F     | F               | C    | 0    | 5    | 9    | 0       | F         | D     | B          | 1    | 1    | 1   | 1   | 1 | 1 | 1 | 1 | 1 | 7 |
| 001A | 1     | X     | X     | X  | X       | 1   | 1   | 1   | X    | X  | F     | F               | X    | X    | X    | X    | X       | X         | X     | 1          | 1    | 1    | 1   | 1   | 1 | 1 | 1 | 1 | 1 | 7 |
| 001B | 0     | F     | X     | 3  | 0       | X   | 1   | 1   | 1    | 0  | 0     | F6              | X    | X    | X    | X    | X       | X         | X     | 1          | 1    | 1    | 1   | 1   | 1 | 1 | 1 | 1 | 1 | 7 |
| 001C | 0     | X     | X     | E  | X       | X   | 1   | 1   | 1    | 0  | F6    | 3               | 5    | C    | 9    | 0    | F       | D         | B     | 1          | 1    | 1    | 1   | 1   | 1 | 1 | 1 | 1 | 1 | 7 |
| 001D | 0     | 3     | X     | D  | 0       | 2   | 1   | 1   | 1    | 0  | F9    | 8               | 0    | 0    | 0    | 0    | 0       | 0         | 0     | 0          | 1    | 1    | 1   | 1   | 1 | 1 | 1 | 1 | 1 | 7 |
| 001E | 1     | X     | X     | X  | X       | 1   | 1   | 1   | X    | X  | F     | F               | X    | X    | X    | X    | X       | X         | X     | 1          | 1    | 1    | 1   | 1   | 1 | 1 | 1 | 1 | 1 | 7 |
| 001F | 1     | F     | X     | X  | 0       | X   | 1   | 1   | 0    | 0  | F6    | X               | X    | X    | X    | X    | X       | X         | X     | 1          | 1    | 1    | 1   | 1   | 1 | 1 | 1 | 1 | 1 | 2 |
| 0020 | 1     | X     | X     | X  | X       | X   | 1   | 1   | 1    | X  | X     | F               | F    | X    | X    | X    | X       | X         | X     | 1          | 1    | 1    | 1   | 1   | 1 | 1 | 1 | 1 | 1 | 7 |
| 0021 | 0     | X     | X     | E  | X       | X   | 1   | 1   | 1    | 0  | F6    | 4               | 0    | 5    | 9    | 0    | F       | D         | B     | 1          | 1    | 1    | 1   | 1   | 1 | 1 | 1 | 1 | 1 | 7 |
| 0022 | 0     | 3     | X     | D  | 0       | 2   | 1   | 1   | 1    | 0  | F9    | 8               | 0    | 0    | 0    | 0    | 0       | 0         | 0     | 0          | 1    | 1    | 1   | 1   | 1 | 1 | 1 | 1 | 1 | 7 |
| 0023 | 1     | X     | X     | X  | X       | 1   | 1   | 1   | X    | X  | F     | F               | X    | X    | X    | X    | X       | X         | X     | 1          | 1    | 1    | 1   | 1   | 1 | 1 | 1 | 1 | 1 | 7 |
| 0024 | 0     | F     | X     | 3  | 0       | X   | 1   | 1   | 1    | 0  | F6    | X               | X    | X    | X    | X    | X       | X         | X     | 1          | 1    | 1    | 1   | 1   | 1 | 1 | 1 | 1 | 1 | 7 |
| 0025 | 0     | 0     | X     | E  | 0       | X   | 1   | 1   | 1    | 0  | F6    | X               | X    | X    | X    | X    | X       | X         | X     | 1          | 1    | 1    | 1   | 1   | 1 | 1 | 1 | 1 | 1 | 7 |
| 0026 | 0     | 0     | X     | D  | 0       | X   | 1   | 1   | 1    | 0  | F6    | X               | X    | X    | X    | X    | X       | X         | X     | 1          | 1    | 1    | 1   | 1   | 1 | 1 | 1 | 1 | 1 | 7 |
| 0027 | 1     | X     | X     | X  | X       | 1   | 1   | 1   | X    | X  | F     | F               | X    | X    | X    | X    | X       | X         | X     | 1          | 1    | 1    | 1   | 1   | 1 | 1 | 1 | 1 | 1 | 7 |
| 0028 | 0     | F     | X     | 4  | 0       | X   | 1   | 1   | 1    | 0  | F6    | X               | X    | X    | X    | X    | X       | X         | X     | 1          | 1    | 1    | 1   | 1   | 1 | 1 | 1 | 1 | 1 | 7 |

Table 5.1. Floating Point Sin(x) Microprogram (continued)

0029 \* R5 = A6  
R5 = #2F34 6FBCh

002A \* R5 = FMUL(R4,R5)  
RE = R4

002B RD = R5

002C JSR FMUL

002D R5 = RF

002E \* R5 = FADD(R5,A5)  
RE = R5

002F RD = #B2D7 5AD5h

0030 JSR FADD

0031 R5 = RF

0032 \* R5 = FMUL(R4,R5)  
RE = R4

0033 RD = R5

0034 JSR FMUL

0035 R5 = RF

0036 \* R5 = FADD(R5,A4)  
RE = R5

0037 RD = #3638 EF99h

0038 JSR FADD

0039 R5 = RF

003A \* R5 = FMUL(R4,R5)  
RE = R4

003B RD = R5

003C JSR FMUL

003D R5 = RF

| WE | A3-A0 | B3-B0 | C3-C0 | EA | EB1-E0 | OEA | OEB | OEC | OED | SELY | Cn | 17-10 | 32-bit Constant | S100 | S108 | S1016 | S1024 | R2-R0 | MUX2-MUX0   | S2-S0 | DRB13-DRB0 | RAOE | RBOE | INC | SEL |
|----|-------|-------|-------|----|--------|-----|-----|-----|-----|------|----|-------|-----------------|------|------|-------|-------|-------|-------------|-------|------------|------|------|-----|-----|
| 0  | X     | X     | 5     | 0  | X      | 1   | 1   | 1   | 1   | 0    | F  | 6     | 2 F 3 4 6 F B C | 1    | 1    | 1     | 1     | 0     | 2 7 X X X X | 1     | 1          | 1    | 1    | 7   |     |
| 0  | 4     | X     | E     | 0  | X      | 1   | 1   | 1   | 0   | 0    | F  | 6     | X X X X X X X X | 1    | 1    | 1     | 1     | 0     | 2 7 X X X X | 1     | 1          | 1    | 1    | 7   |     |
| 0  | 5     | X     | D     | 0  | X      | 1   | 1   | 1   | 0   | 0    | F  | 6     | X X X X X X X X | 1    | 1    | 1     | 1     | 0     | 2 7 X X X X | 1     | 1          | 1    | 1    | 7   |     |
| 1  | X     | X     | X     | X  | 1      | 1   | X   | X   | F   | F    |    |       | X X X X X X X X | 1    | 1    | 1     | 1     | 0     | 1 4 0 0 6 0 | 1     | 1          | 1    | 1    | 7   |     |
| 0  | F     | X     | 5     | 0  | X      | 1   | 1   | 1   | 0   | 0    | F  | 6     | X X X X X X X X | 1    | 1    | 1     | 1     | 0     | 2 7 X X X X | 1     | 1          | 1    | 1    | 7   |     |
| 0  | 5     | X     | E     | 0  | X      | 1   | 1   | 1   | 0   | 0    | F  | 6     | X X X X X X X X | 1    | 1    | 1     | 1     | 0     | 2 7 X X X X | 1     | 1          | 1    | 1    | 7   |     |
| 0  | X     | X     | D     | X  | X      | 1   | 1   | 1   | X   | F    | F  |       | B 2 D 7 5 A D 5 | 1    | 1    | 1     | 1     | 0     | 2 7 X X X X | 1     | 1          | 1    | 1    | 7   |     |
| 1  | X     | X     | X     | X  | 1      | 1   | X   | X   | F   | F    |    |       | X X X X X X X X | 1    | 1    | 1     | 1     | 0     | 1 4 0 0 7 4 | 1     | 1          | 1    | 1    | 7   |     |
| 0  | F     | X     | 5     | 0  | X      | 1   | 1   | 1   | 0   | 0    | F  | 6     | X X X X X X X X | 1    | 1    | 1     | 1     | 0     | 2 7 X X X X | 1     | 1          | 1    | 1    | 7   |     |
| 0  | 4     | X     | E     | 0  | X      | 1   | 1   | 1   | 0   | 0    | F  | 6     | X X X X X X X X | 1    | 1    | 1     | 1     | 0     | 2 7 X X X X | 1     | 1          | 1    | 1    | 7   |     |
| 0  | 5     | X     | D     | 0  | X      | 1   | 1   | 1   | 0   | 0    | F  | 6     | X X X X X X X X | 1    | 1    | 1     | 1     | 0     | 2 7 X X X X | 1     | 1          | 1    | 1    | 7   |     |
| 1  | X     | X     | X     | X  | 1      | 1   | X   | X   | F   | F    |    |       | X X X X X X X X | 1    | 1    | 1     | 1     | 0     | 1 4 0 0 6 0 | 1     | 1          | 1    | 1    | 7   |     |
| 0  | F     | X     | 5     | 0  | X      | 1   | 1   | 1   | 0   | 0    | F  | 6     | X X X X X X X X | 1    | 1    | 1     | 1     | 0     | 2 7 X X X X | 1     | 1          | 1    | 1    | 7   |     |
| 0  | 5     | X     | E     | 0  | X      | 1   | 1   | 1   | 0   | 0    | F  | 6     | X X X X X X X X | 1    | 1    | 1     | 1     | 0     | 2 7 X X X X | 1     | 1          | 1    | 1    | 7   |     |
| 0  | X     | X     | D     | X  | X      | 1   | 1   | 1   | X   | F    | F  |       | 3 6 3 8 E F 9 9 | 1    | 1    | 1     | 1     | 0     | 2 7 X X X X | 1     | 1          | 1    | 1    | 7   |     |
| 1  | X     | X     | X     | X  | 1      | 1   | X   | X   | F   | F    |    |       | X X X X X X X X | 1    | 1    | 1     | 1     | 0     | 1 4 0 0 7 4 | 1     | 1          | 1    | 1    | 7   |     |
| 0  | F     | X     | 5     | 0  | X      | 1   | 1   | 1   | 0   | 0    | F  | 6     | X X X X X X X X | 1    | 1    | 1     | 1     | 0     | 2 7 X X X X | 1     | 1          | 1    | 1    | 7   |     |
| 0  | 4     | X     | E     | 0  | X      | 1   | 1   | 1   | 0   | 0    | F  | 6     | X X X X X X X X | 1    | 1    | 1     | 1     | 0     | 2 7 X X X X | 1     | 1          | 1    | 1    | 7   |     |
| 0  | 5     | X     | D     | 0  | X      | 1   | 1   | 1   | 0   | 0    | F  | 6     | X X X X X X X X | 1    | 1    | 1     | 1     | 0     | 2 7 X X X X | 1     | 1          | 1    | 1    | 7   |     |
| 1  | X     | X     | X     | X  | 1      | 1   | X   | X   | F   | F    |    |       | X X X X X X X X | 1    | 1    | 1     | 1     | 0     | 1 4 0 0 6 0 | 1     | 1          | 1    | 1    | 7   |     |
| 0  | F     | X     | 5     | 0  | X      | 1   | 1   | 1   | 0   | 0    | F  | 6     | X X X X X X X X | 1    | 1    | 1     | 1     | 0     | 2 7 X X X X | 1     | 1          | 1    | 1    | 7   |     |

Table 5.1. Floating Point Sin(x) Microprogram (continued)

003E \* R5 = FADD(R5,A3)  
 RE = R5  
 003F RD = #B950 0D01h  
 0040 JSR FADD  
 0041 R5 = RF

0042 \* R5 = FMUL(R4,R5)  
 RE = R4  
 0043 RD = R5  
 0044 JSR FMUL  
 0045 R5 = RF

0046 \* R5 = FADD(R5,A2)  
 RE = R5  
 0047 RD = #3C08 8888h  
 0048 JSR FADD  
 0049 R5 = RF

004A \* R5 = FMUL(R4,R5)  
 RE = R4  
 004B RD = R5  
 004C JSR FMUL  
 004D R5 = RF

004E \* R5 = FADD(R5,A1)  
 RE = R5  
 004F RD = #BE2A AAADh  
 0050 JSR FADD  
 0051 R5 = RF

0052 \* R5 = FMUL(R4,R5)  
 RE = R4  
 0053 RD = R5  
 0054 JSR FMUL  
 0055 R5 = RF

| WE | A3-A0 | B3-B0 | C3-C0 | EA | EB1-EB0 | OEA | OEB | OEC | SELY | Cn | I7-I0 | 32-bit Constant | SIO0 | SIO8 | SIO16 | SIO24 | RC2-RC0 | MUX2-MUX0 | S2-S0 | DRB13-DRB0 | RAOE | RBOE | INC | SEL |   |   |   |
|----|-------|-------|-------|----|---------|-----|-----|-----|------|----|-------|-----------------|------|------|-------|-------|---------|-----------|-------|------------|------|------|-----|-----|---|---|---|
| 0  | 0     | 5     | X     | E  | 0       | X   | 1   | 1   | 1    | 0  | 0     | F               | 6    | X    | X     | X     | X       | X         | X     | 1          | 1    | 1    | 1   | 1   | 7 |   |   |
| 0  | X     | X     | D     | X  | X       | 1   | 1   | 1   | 1    | X  | F     | F               | B    | 9    | 5     | 0     | 0       | D         | 0     | 1          | 1    | 1    | 1   | 1   | 7 |   |   |
| 1  | X     | X     | X     | X  | 1       | 1   | 1   | X   | X    | F  | F     | X               | X    | X    | X     | X     | X       | X         | X     | 1          | 1    | 1    | 1   | 1   | 7 |   |   |
| 0  | F     | X     | 5     | 0  | X       | 1   | 1   | 1   | 0    | 0  | F     | 6               | X    | X    | X     | X     | X       | X         | X     | 0          | 2    | 7    | X   | X   | 1 | 1 | 7 |
| 0  | 4     | X     | E     | 0  | X       | 1   | 1   | 1   | 0    | 0  | F     | 6               | X    | X    | X     | X     | X       | X         | X     | 1          | 1    | 1    | 1   | 1   | 7 |   |   |
| 0  | 5     | X     | D     | 0  | X       | 1   | 1   | 1   | 0    | 0  | F     | 6               | X    | X    | X     | X     | X       | X         | X     | 0          | 2    | 7    | X   | X   | 1 | 1 | 7 |
| 1  | X     | X     | X     | X  | 1       | 1   | 1   | X   | X    | F  | F     | X               | X    | X    | X     | X     | X       | X         | X     | 1          | 1    | 1    | 1   | 1   | 7 |   |   |
| 0  | F     | X     | 5     | 0  | X       | 1   | 1   | 1   | 0    | 0  | F     | 6               | X    | X    | X     | X     | X       | X         | X     | 0          | 2    | 7    | X   | X   | 1 | 1 | 7 |
| 0  | 5     | X     | E     | 0  | X       | 1   | 1   | 1   | 0    | 0  | F     | 6               | X    | X    | X     | X     | X       | X         | X     | 1          | 1    | 1    | 1   | 1   | 7 |   |   |
| 0  | X     | X     | D     | X  | X       | 1   | 1   | 1   | X    | F  | F     | 3               | C    | 0    | 8     | 8     | 8       | 8         | 8     | 1          | 1    | 1    | 1   | 1   | 7 |   |   |
| 1  | X     | X     | X     | X  | 1       | 1   | 1   | X   | X    | F  | F     | X               | X    | X    | X     | X     | X       | X         | X     | 1          | 1    | 1    | 1   | 1   | 7 |   |   |
| 0  | F     | X     | 5     | 0  | X       | 1   | 1   | 1   | 0    | 0  | F     | 6               | X    | X    | X     | X     | X       | X         | X     | 0          | 2    | 7    | X   | X   | 1 | 1 | 7 |
| 0  | 4     | X     | E     | 0  | X       | 1   | 1   | 1   | 0    | 0  | F     | 6               | X    | X    | X     | X     | X       | X         | X     | 1          | 1    | 1    | 1   | 1   | 7 |   |   |
| 0  | 5     | X     | D     | 0  | X       | 1   | 1   | 1   | 0    | 0  | F     | 6               | X    | X    | X     | X     | X       | X         | X     | 0          | 2    | 7    | X   | X   | 1 | 1 | 7 |
| 1  | X     | X     | X     | X  | 1       | 1   | 1   | X   | X    | F  | F     | X               | X    | X    | X     | X     | X       | X         | X     | 1          | 1    | 1    | 1   | 1   | 7 |   |   |
| 0  | F     | X     | 5     | 0  | X       | 1   | 1   | 1   | 0    | 0  | F     | 6               | X    | X    | X     | X     | X       | X         | X     | 0          | 2    | 7    | X   | X   | 1 | 1 | 7 |
| 0  | 5     | X     | E     | 0  | X       | 1   | 1   | 1   | 0    | 0  | F     | 6               | X    | X    | X     | X     | X       | X         | X     | 1          | 1    | 1    | 1   | 1   | 7 |   |   |
| 0  | X     | X     | D     | X  | X       | 1   | 1   | 1   | 1    | F  | F     | B               | E    | 2    | A     | A     | A       | A         | D     | 1          | 1    | 1    | 1   | 1   | 7 |   |   |
| 1  | X     | X     | X     | X  | 1       | 1   | 1   | X   | X    | F  | F     | X               | X    | X    | X     | X     | X       | X         | X     | 1          | 1    | 1    | 1   | 1   | 7 |   |   |
| 0  | F     | X     | 5     | 0  | X       | 1   | 1   | 1   | 0    | 0  | F     | 6               | X    | X    | X     | X     | X       | X         | X     | 0          | 2    | 7    | X   | X   | 1 | 1 | 7 |
| 0  | 4     | X     | E     | 0  | X       | 1   | 1   | 1   | 0    | 0  | F     | 6               | X    | X    | X     | X     | X       | X         | X     | 1          | 1    | 1    | 1   | 1   | 7 |   |   |
| 0  | 5     | X     | D     | 0  | X       | 1   | 1   | 1   | 0    | 0  | F     | 6               | X    | X    | X     | X     | X       | X         | X     | 0          | 2    | 7    | X   | X   | 1 | 1 | 7 |
| 1  | X     | X     | X     | X  | 1       | 1   | 1   | X   | X    | F  | F     | X               | X    | X    | X     | X     | X       | X         | X     | 1          | 1    | 1    | 1   | 1   | 7 |   |   |
| 0  | F     | X     | 5     | 0  | X       | 1   | 1   | 1   | 0    | 0  | F     | 6               | X    | X    | X     | X     | X       | X         | X     | 0          | 2    | 7    | X   | X   | 1 | 1 | 7 |





Table 5.1. Floating Point Sin(x) Microprogram (continued)

0056 \* R5 = FADD(R5,A0)  
RE = R5

0057 RD = #3F80 0000h

0058 JSR FADD

0059 R5 = RF

\* R5 = FMUL(R0,R5)

005A RE = R0

005B RD = R5

005C JSR FMUL

005D R5 = RF

\* R5 = FCHS(R5,R1) : RETURN

005E R1 = R1 OR #7FFF FFFFh

005F R5 = R5 XOR R1 : RETURN

\* RC = FEXP(RE)

0060 FMUL: RC = RE AND #7F80 0000h

\* RE = FRAC(RE)

0061 RE = RE AND #807F FFFFh

\* RE = RE OR bit23

0062 RE = RE OR #0080 0000h

\* MQ = SMTC(RE)

0063 RE = SMTC(RE)

0064 LOADMQ : PASS

\* RB = FEXP(RD)

0065 RB = RD AND #7F80 0000h

| WE<br>A3-A0<br>B3-B0<br>C3-C0<br>EA<br>EB1-EB0<br>OE $\bar{A}$<br>OEB<br>OEY<br>SELY<br>Cn<br>I7-I0 | 32-bit<br>Constant | SIO0<br>SIOB<br>SIO16<br>SIO24 | RC2-RC0<br>MUX2-MUX0<br>S2-S0 | DRB13-<br>DRB0 | RAOE<br>RBOE<br>INC | SEL |
|-----------------------------------------------------------------------------------------------------|--------------------|--------------------------------|-------------------------------|----------------|---------------------|-----|
| 0 5 X E 0 X 1 1 1 0 0 F 6                                                                           | X X X X X X X X    | 1 1 1 1                        | 0 2 7 X X X X                 | 1 1 1 7        |                     |     |
| 0 X X D X X 1 1 1 1 X F F                                                                           | 3 F 8 0 0 0 0 0    | 1 1 1 1                        | 0 2 7 X X X X                 | 1 1 1 7        |                     |     |
| 1 X X X X X 1 1 1 X X F F                                                                           | X X X X X X X X    | 1 1 1 1                        | 0 1 4 0 0 7 4                 | 1 1 1 7        |                     |     |
| 0 F X 5 0 X 1 1 1 0 0 F 6                                                                           | X X X X X X X X    | 1 1 1 1                        | 0 2 7 X X X X                 | 1 1 1 7        |                     |     |
| 0 0 X E 0 X 1 1 1 0 0 F 6                                                                           | X X X X X X X X    | 1 1 1 1                        | 0 2 7 X X X X                 | 1 1 1 7        |                     |     |
| 0 5 X D 0 X 1 1 1 0 0 F 6                                                                           | X X X X X X X X    | 1 1 1 1                        | 0 2 7 X X X X                 | 1 1 1 7        |                     |     |
| 1 X X X X X 1 1 1 X X F F                                                                           | X X X X X X X X    | 1 1 1 1                        | 0 1 4 0 0 6 0                 | 1 1 1 7        |                     |     |
| 0 F X 5 0 X 1 1 1 0 0 F 6                                                                           | X X X X X X X X    | 1 1 1 1                        | 0 2 7 X X X X                 | 1 1 1 7        |                     |     |
| 0 1 X 1 0 2 1 1 1 0 0 F B                                                                           | B 7 F F F F F F    | 1 1 1 1                        | 0 2 7 X X X X                 | 1 1 1 7        |                     |     |
| 0 5 1 5 0 0 1 1 1 0 0 F 0                                                                           | X X X X X X X X    | 1 1 1 1                        | 0 2 2 X X X X                 | 1 1 1 7        |                     |     |
| 0 E X C 0 2 1 1 1 0 0 F A                                                                           | 7 F 8 0 0 0 0 0    | 1 1 1 1                        | 0 2 7 X X X X                 | 1 1 1 7        |                     |     |
| 0 E X E 0 2 1 1 1 0 0 F A                                                                           | 8 0 7 F F F F F    | 1 1 1 1                        | 0 2 7 X X X X                 | 1 1 1 7        |                     |     |
| 0 E X F 0 2 1 1 1 0 0 F B                                                                           | 0 0 8 0 0 0 0 0    | 1 1 1 1                        | 0 2 7 X X X X                 | 1 1 1 7        |                     |     |
| 0 X E E X 0 1 1 1 1 0 5 8                                                                           | X X X X X X X X    | 1 1 1 1                        | 0 2 7 X X X X                 | 1 1 1 7        |                     |     |
| 1 E X X 0 X 1 1 1 1 0 E 6                                                                           | X X X X X X X X    | 1 1 1 1                        | 0 2 7 X X X X                 | 1 1 1 7        |                     |     |
| 0 D X B 0 2 1 1 1 0 0 F A                                                                           | 7 F 8 0 0 0 0 0    | 1 1 1 1                        | 0 2 7 X X X X                 | 1 1 1 7        |                     |     |

Table 5.1. Floating Point Sin(x) Microprogram (continued)

0066 \* RD = FRAC(RD)  
RD = RD AND #807 FFFFh

0067 RD = RD OR bit23

0068 RD = SMTC(RD)

0069 RE = 0 : RCB = #22D

006A RE = SMULI RD : LOOP RCB

006B RE = SMULT RD

006C TBO(RE,bit1) : BYTE = #0100b : TEST Z

006D JT FMUL1

\* INEX RC

006E RC = RC ADD #0080 0000h

006F RE = SRA(RE)

0070 FMUL1: RC = RC ADD RB : TEST CARRY

0071 JT ERROR

0072 RE = SMTC(RE)

0073 RE = RE AND #807 FFFFh

\* FADD: RC = FEXP(RE)

0074 FADD: RC = RC AND #7F80 0000

\* RE = FRAC(RE)

0075 RE = RE AND #807 FFFFh

0076 MQ = RE OR bit23

0077 RE = SMTC(RE)

\* RB = FEXP(RD)

0078 RB = RD AND #7F80 0000

| WE<br>A3-A0<br>B3-B0<br>C3-C0<br>EA<br>EB1-EB0<br>OEA<br>OEB<br>OEV<br>SELY<br>Cn<br>17-10 | 32-bit<br>Constant | S100<br>S108<br>S1016<br>S1024 | RC2-RC0<br>MUX2-MUX0<br>S2-S0 | DRB13-<br>DRB0 | RAOE<br>RBOE<br>INC | SEL |
|--------------------------------------------------------------------------------------------|--------------------|--------------------------------|-------------------------------|----------------|---------------------|-----|
| 0DXD0211100FA                                                                              | 807FFFFF           | 1111                           | 027XXXX                       | 111            | 7                   |     |
| 0DXD0211100FB                                                                              | 00800000           | 1111                           | 027XXXX                       | 111            | 7                   |     |
| 0XDDX01111D58                                                                              | XXXXXXXX           | 1111                           | 027XXXX                       | 111            | 7                   |     |
| 0EE0011110F9                                                                               | 00000016           | 1111                           | 617XXXX                       | 111            | 4                   |     |
| 0DEE001111060                                                                              | XXXXXXXX           | 1111                           | 567006A                       | 111            | 4                   |     |
| 0DEE001110070                                                                              | XXXXXXXX           | 1111                           | 067XXXX                       | 111            | 7                   |     |
| 00F0001111038                                                                              | XXXXXXXX           | 1011                           | 027XXXX                       | 111            | 4                   |     |
| 1XXXXXX111XF                                                                               | XXXXXXXX           | 1111                           | 017XXXX                       | 111            | 7                   |     |
| 0CXC0211100F1                                                                              | 00800000           | 1111                           | 027XXXX                       | 111            | 7                   |     |
| 0EXE0X1110006                                                                              | XXXXXXXX           | 1111                           | 027XXXX                       | 111            | 7                   |     |
| 0CBC0011100F1                                                                              | XXXXXXXX           | 1111                           | 027XXXX                       | 111            | 0                   |     |
| 1XXXXX111XFF                                                                               | XXXXXXXX           | 1111                           | 017XXXX                       | 111            | 7                   |     |
| 0XEE0X01111058                                                                             | XXXXXXXX           | 1111                           | 027XXXX                       | 111            | 7                   |     |
| 0XEE0211100FA                                                                              | 807FFFFF           | 1111                           | 027XXXX                       | 111            | 7                   |     |
| 0CXC0211100FA                                                                              | 7F800000           | 1111                           | 027XXXX                       | 111            | 7                   |     |
| 0XEE0211100FA                                                                              | 807FFFFF           | 1111                           | 027XXXX                       | 111            | 7                   |     |
| 1EXX0111100EB                                                                              | 00800000           | 1111                           | 027XXXX                       | 111            | 7                   |     |
| 0XEE0211100FA                                                                              | 807FFFFF           | 1111                           | 027XXXX                       | 111            | 7                   |     |
| 0DXB0211100FA                                                                              | 7F800000           | 1111                           | 027XXXX                       | 111            | 7                   |     |



Table 5.1. Floating Point Sin(x) Microprogram (continued)

\* RD = FRAC(RD)  
 0079 RE = RE AND #807F FFFFh  
 007A RD = RD OR bit23  
 007B RD = SMTC(RD)  
 007C RF = RC - RB : C0=0: TEST NEG  
 007D JT FADD1 : RCB = #8  
 007E Y/RF = SLC(RF) : LOOP RCB  
 007F Y = RF : RCA = Y  
 0080 RD = SRA(RD) : LOOP RCA  
 0081 RB = RC : JUMP FADD2  
 0082 FADD1: RF = NOT RF  
 0083 Y/RF = SLC(RF) : LOOP RCB  
 0084 Y = RF : RCA = Y  
 0085 RE = SRA(RE) : LOOP RCA  
 0086 FADD2: RF = RD + RE  
 0087 RF = SMTC(RF)  
 0088 RF = TB0 (RF, bit24) : TEST Z  
 0089 JF FADD3  
 008A INC RB : TEST NEG  
 008B RF = SRA(RF) : JT ERROR  
 008C FADD3: RF = SET0 (RF, bit23)  
 008D RF = RF OR RB : RETURN

| WE          | A3-A0 | B3-B0 | C3-C0 | EA | EB1-EB0 | OEA | OEB | OEV | SELY | Cn  | I7-I0 | 32-bit Constant | S100 | S108 | S1016 | S1024 | RC2-RC0 | MUX2-MUX0 | DRB13-DRB0 | RAOE | RBOE | INC | SEL |   |   |
|-------------|-------|-------|-------|----|---------|-----|-----|-----|------|-----|-------|-----------------|------|------|-------|-------|---------|-----------|------------|------|------|-----|-----|---|---|
| 0079        | 0     | E     | X     | E  | 0       | 2   | 1   | 1   | 1    | 0   | 0     | F A             | 8    | 0    | 7     | F     | F       | F         | F          | F    | 1    | 1   | 1   | 1 | 7 |
| 007A        | 0     | D     | X     | D  | 0       | 2   | 1   | 1   | 1    | 0   | 0     | F B             | 0    | 0    | 8     | 0     | 0       | 0         | 0          | 0    | 0    | 0   | 0   | 0 | 7 |
| 007B        | 0     | X     | D     | D  | X       | 0   | 1   | 1   | 1    | 1   | 0     | 5 8             | X    | X    | X     | X     | X       | X         | X          | X    | X    | X   | X   | X | 7 |
| 007C        | 0     | C     | B     | F  | 0       | 0   | 1   | 1   | 1    | 0   | 0     | F 3             | X    | X    | X     | X     | X       | X         | X          | X    | X    | X   | X   | X | 2 |
| 007D        | 1     | X     | X     | X  | X       | 1   | 1   | 1   | X    | X   | F F   | X               | X    | X    | X     | X     | 8       | 1         | 1          | 1    | 1    | 1   | 1   | 1 | 4 |
| 007E        | 0     | F     | X     | F  | 0       | X   | 1   | 1   | 0    | X   | 0     | 6 6             | X    | X    | X     | X     | X       | X         | X          | 1    | 1    | 1   | 1   | 1 | 4 |
| 007F        | 1     | X     | X     | X  | X       | 1   | 1   | 0   | 0    | X   | F F   | X               | X    | X    | X     | X     | X       | 1         | 1          | 1    | 1    | 1   | 1   | 1 | 7 |
| 0080        | 0     | D     | X     | D  | X       | 1   | 1   | 1   | 0    | 0   | 0     | 6               | X    | X    | X     | X     | X       | 1         | 1          | 1    | 1    | 1   | 1   | 1 | 4 |
| 0081        | 0     | C     | X     | B  | 0       | X   | 1   | 1   | 0    | X   | F F   | X               | X    | X    | X     | X     | X       | 1         | 1          | 1    | 1    | 1   | 1   | 1 | 7 |
| 0082 FADD1: | 0     | F     | X     | F  | 0       | X   | 1   | 1   | 1    | 0   | 0     | F 7             | X    | X    | X     | X     | X       | X         | 1          | 1    | 1    | 1   | 1   | 1 | 7 |
| 0083        | 0     | F     | X     | F  | 0       | X   | 1   | 1   | 0    | 0   | 0     | 6 6             | X    | X    | X     | X     | X       | 1         | 1          | 1    | 1    | 1   | 1   | 1 | 4 |
| 0084        | 1     | X     | X     | X  | X       | 1   | 1   | 0   | 0    | X   | F F   | X               | X    | X    | X     | X     | X       | 1         | 1          | 1    | 1    | 1   | 1   | 1 | 4 |
| 0085        | 0     | E     | X     | E  | 0       | X   | 1   | 1   | 1    | 0   | 0     | 6               | X    | X    | X     | X     | X       | X         | 1          | 1    | 1    | 1   | 1   | 1 | 7 |
| 0086 FADD2: | 0     | D     | E     | F  | 0       | 0   | 1   | 1   | 1    | 0   | 0     | F 1             | X    | X    | X     | X     | X       | X         | 1          | 1    | 1    | 1   | 1   | 1 | 7 |
| 0087        | 0     | X     | F     | F  | X       | 0   | 1   | 1   | 1    | 1   | 0     | 5 8             | X    | X    | X     | X     | X       | X         | 1          | 1    | 1    | 1   | 1   | 1 | 7 |
| 0088        | 0     | X     | F     | 0  | 0       | 1   | 1   | 1   | 1    | 0   | 3 8   | X               | X    | X    | X     | X     | X       | 0         | 1          | 1    | 1    | 1   | 1   | 1 | 4 |
| 0089        | 1     | X     | X     | X  | X       | 1   | 1   | X   | X    | F F | X     | X               | X    | X    | X     | X     | X       | 1         | 1          | 1    | 1    | 1   | 1   | 1 | 7 |
| 008A        | 0     | B     | X     | B  | 0       | X   | 1   | 1   | 1    | 1   | F 6   | X               | X    | X    | X     | X     | X       | 1         | 1          | 1    | 1    | 1   | 1   | 1 | 3 |
| 008B        | 0     | F     | 7     | F  | 0       | X   | 1   | 1   | 0    | 0   | 0     | 6               | X    | X    | X     | X     | X       | X         | 1          | 1    | 1    | 1   | 1   | 1 | 7 |
| 008C FADD3: | 0     | 7     | F     | 0  | 0       | 0   | 1   | 1   | 1    | 0   | 1     | 8               | X    | X    | X     | X     | X       | X         | 1          | 0    | 1    | 1   | 1   | 1 | 7 |
| 008D        | 0     | F     | B     | F  | 0       | 0   | 1   | 1   | 1    | 0   | 0     | F B             | X    | X    | X     | X     | X       | X         | 1          | 1    | 1    | 1   | 1   | 1 | 7 |

## **General Information**

**1**

**Numerical Index**  
**Glossary**  
**Explanation of Function Tables**  
**Parameter Measurement Information**  
**Functional Index**

## **LSI Devices**

**2**

## **Application Reports**

**3**

**Advanced Schottky Family**  
**Error Detection and Correction**  
**Memory Mapping**  
**Bit-Slice Processor 8-Bit Family**  
**Excerpt — SN74AS888, SN74AS890**  
**Bit-Slice Processor User's Guide**

## **Mechanical Data**

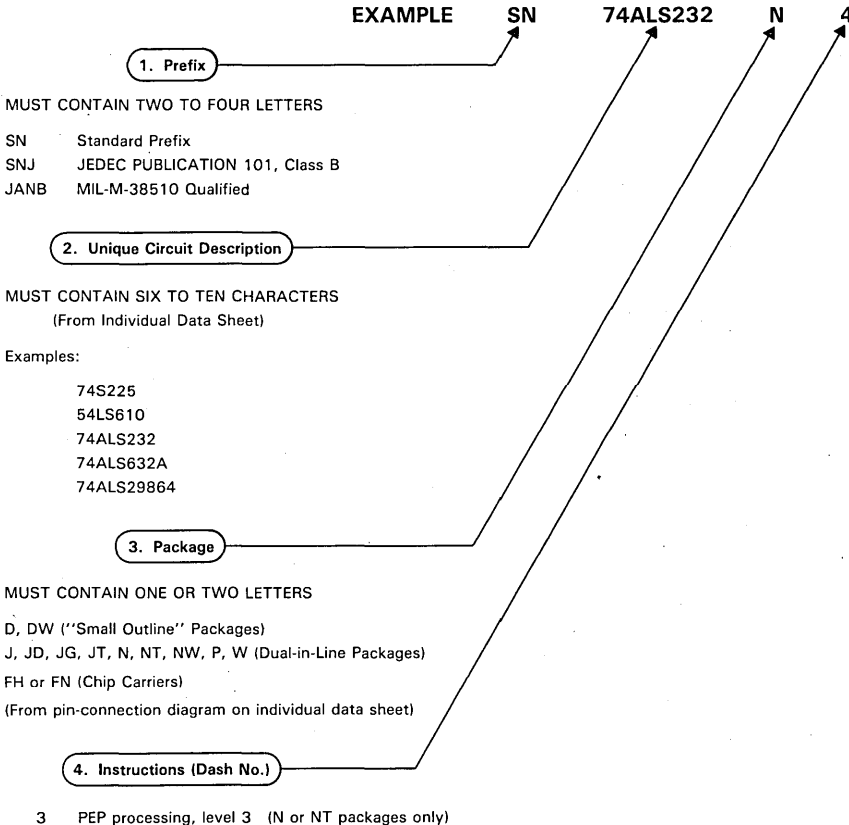
**4**



ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.



†These circuits in dual-in-line and "small outline" packages are shipped in one of the carriers shown below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped in the most practical carrier. Please contact your TI sales representative for the method that will best suit your particular needs.

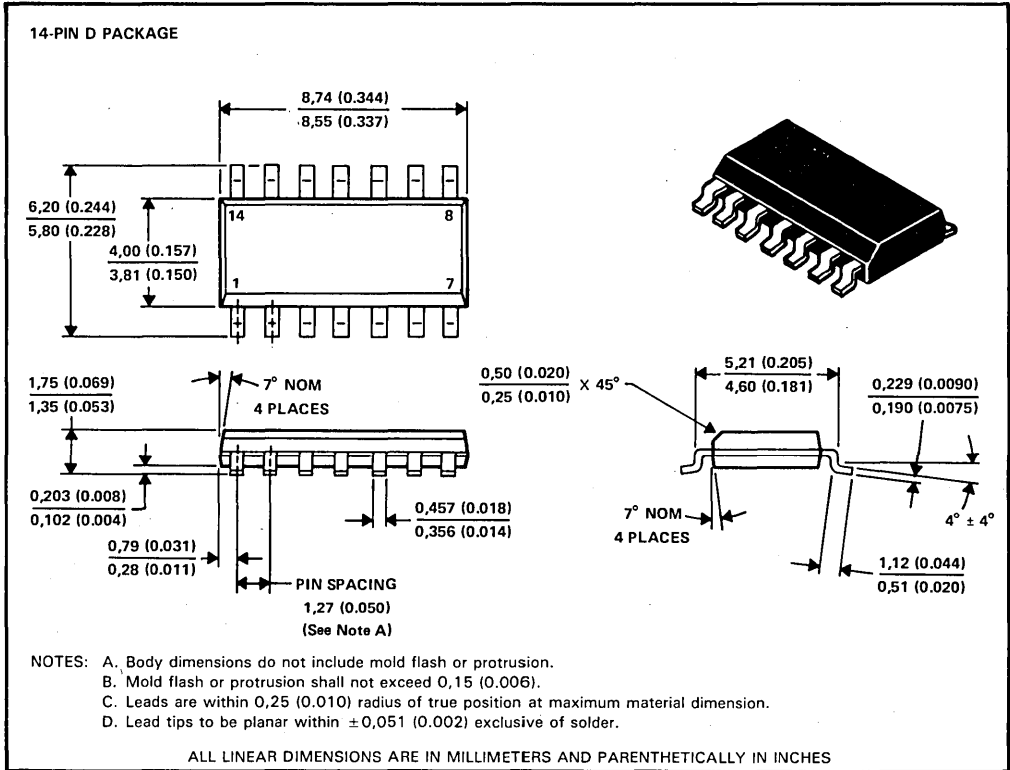
"Small Outline" (D, DW)  
 Dual-in-Line (J, JD, JG, JT, N, NT, NW, P, W)

- A-Channel Plastic Tubing
- Tape and Reel
- Barnes Carrier (W only)

# MECHANICAL DATA

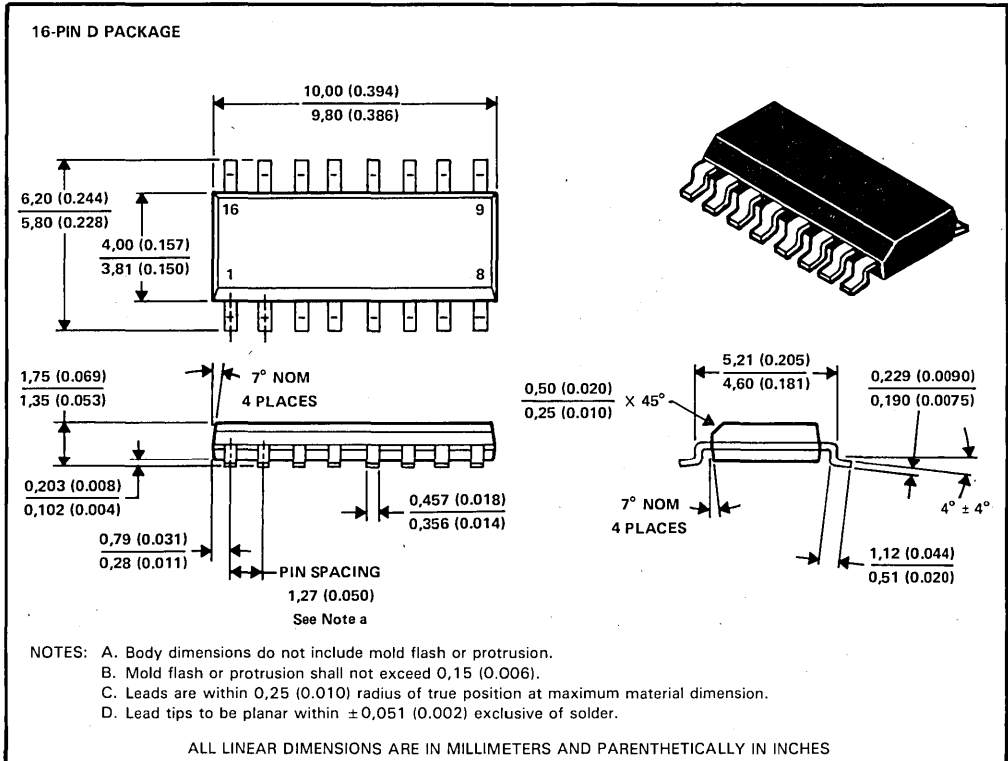
## D plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



D plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



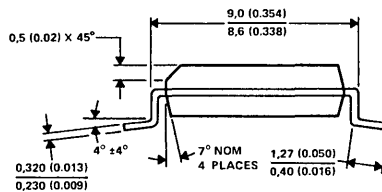
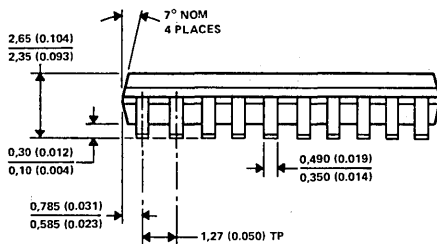
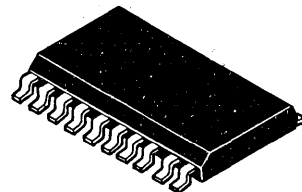
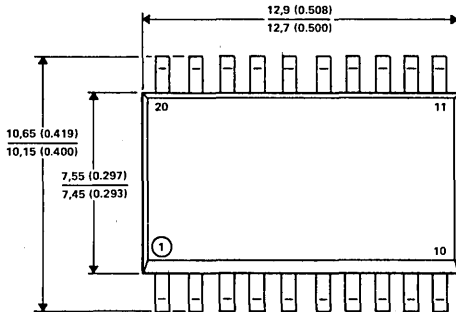


# MECHANICAL DATA

## DW plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

### 20-PIN DW PACKAGE



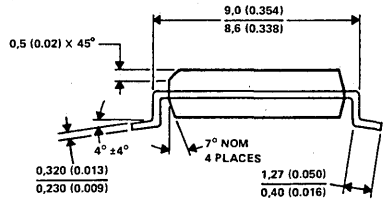
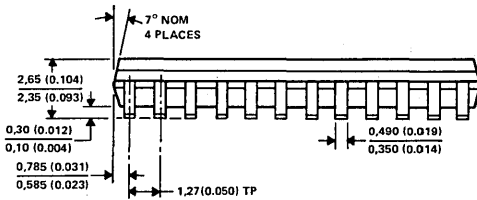
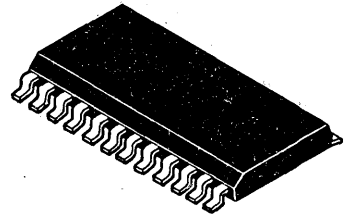
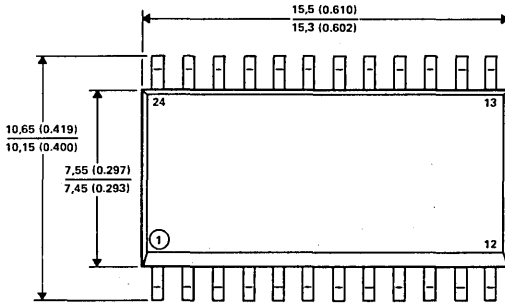
- NOTES: A. Body dimensions do not include mold flash or protrusion.  
 B. Mold flash or protrusion shall not exceed 0,15 (0.006).  
 C. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.  
 D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

DW plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

24-PIN DW PACKAGE



- NOTES: A. Body dimensions do not include mold flash or protrusion.  
 B. Mold flash or protrusion shall not exceed 0,15 (0.006).  
 C. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.  
 D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

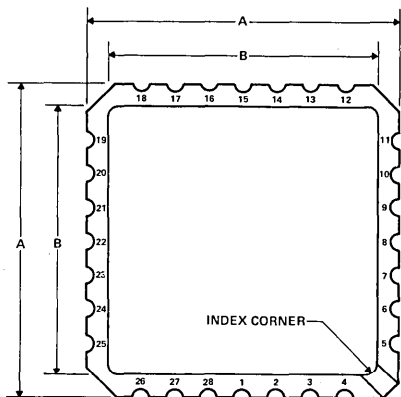
# MECHANICAL DATA

## FK ceramic chip carrier packages

Each of these hermetically sealed chip carrier packages has a three-layer ceramic base with a metal lid and braze seal. The packages are intended for surface mounting on solder lands on 1,27 (0.050-inch) centers. terminals require no additional cleaning or processing when used in soldered assembly.

FK package terminal assignments conform to JEDEC Standards 1 and 2.

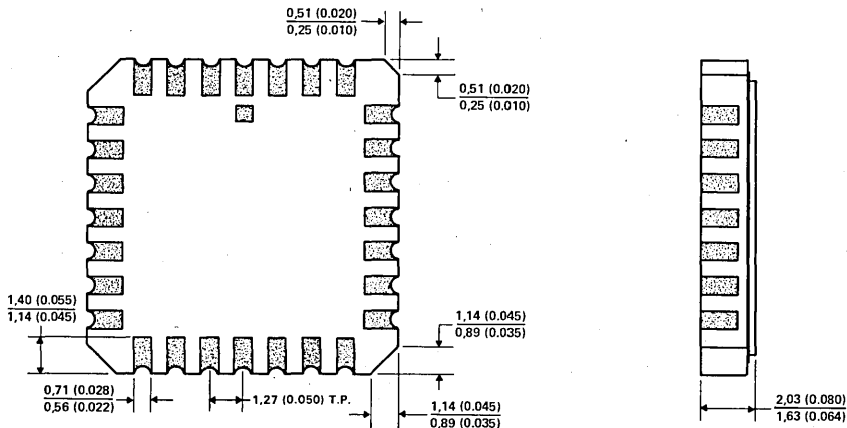
FK CERAMIC CHIP CARRIER PACKAGES  
(28-terminal package shown)



CERAMIC CHIP CARRIERS

| JEDEC OUTLINE DESIGNATION* | NO. OF TERMINALS | A                |                  | B                |                  |
|----------------------------|------------------|------------------|------------------|------------------|------------------|
|                            |                  | MIN              | MAX              | MIN              | MAX              |
| MS004CB                    | 20               | 8,69<br>(0.342)  | 9,09<br>(0.358)  | 7,80<br>(0.307)  | 9,09<br>(0.358)  |
| MS004CC                    | 28               | 11,23<br>(0.442) | 11,63<br>(0.458) | 10,31<br>(0.406) | 11,63<br>(0.458) |

\*All dimensions and notes for the specified JEDEC outline apply.

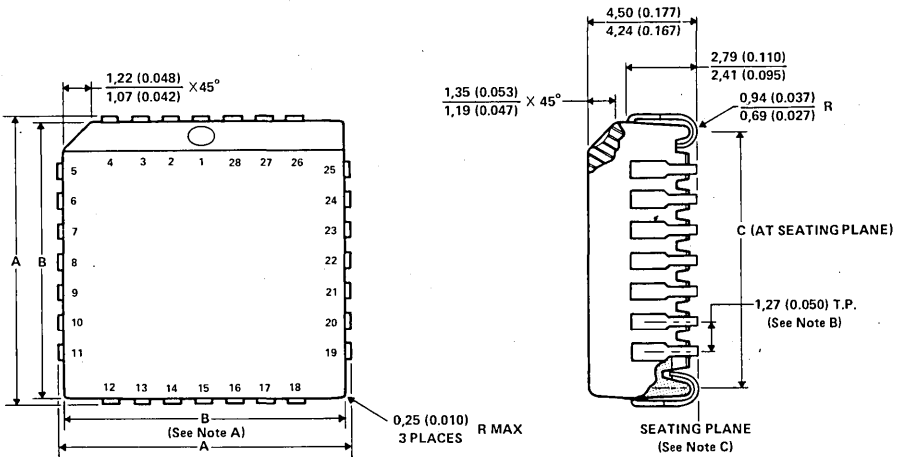


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

**FN plastic chip carrier package**

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.

**FN PLASTIC CHIP CARRIER PACKAGE**  
(28-terminal package used for illustration)



| JEDEC OUTLINE | NO. OF TERMINALS | A                |                  | B                |                  | C                |                  |
|---------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
|               |                  | MIN              | MAX              | MIN              | MAX              | MIN              | MAX              |
| MO 047AA      | 20               | 9.78<br>(0.385)  | 10.03<br>(0.395) | 8.89<br>(0.350)  | 9.04<br>(0.356)  | 7.87<br>(0.310)  | 8.38<br>(0.330)  |
| MO 047AB      | 28               | 12.32<br>(0.485) | 12.57<br>(0.495) | 11.43<br>(0.450) | 11.58<br>(0.456) | 10.41<br>(0.410) | 10.92<br>(0.430) |
| MO 047AC      | 44               | 17.40<br>(0.685) | 17.65<br>(0.695) | 16.51<br>(0.650) | 16.66<br>(0.656) | 15.49<br>(0.610) | 16.00<br>(0.630) |
| MO 047AE      | 68               | 25.02<br>(0.985) | 25.27<br>(0.995) | 24.13<br>(0.950) | 24.33<br>(0.956) | 23.11<br>(0.910) | 23.62<br>(0.930) |

All dimensions and notes for the specified JEDEC outline apply.

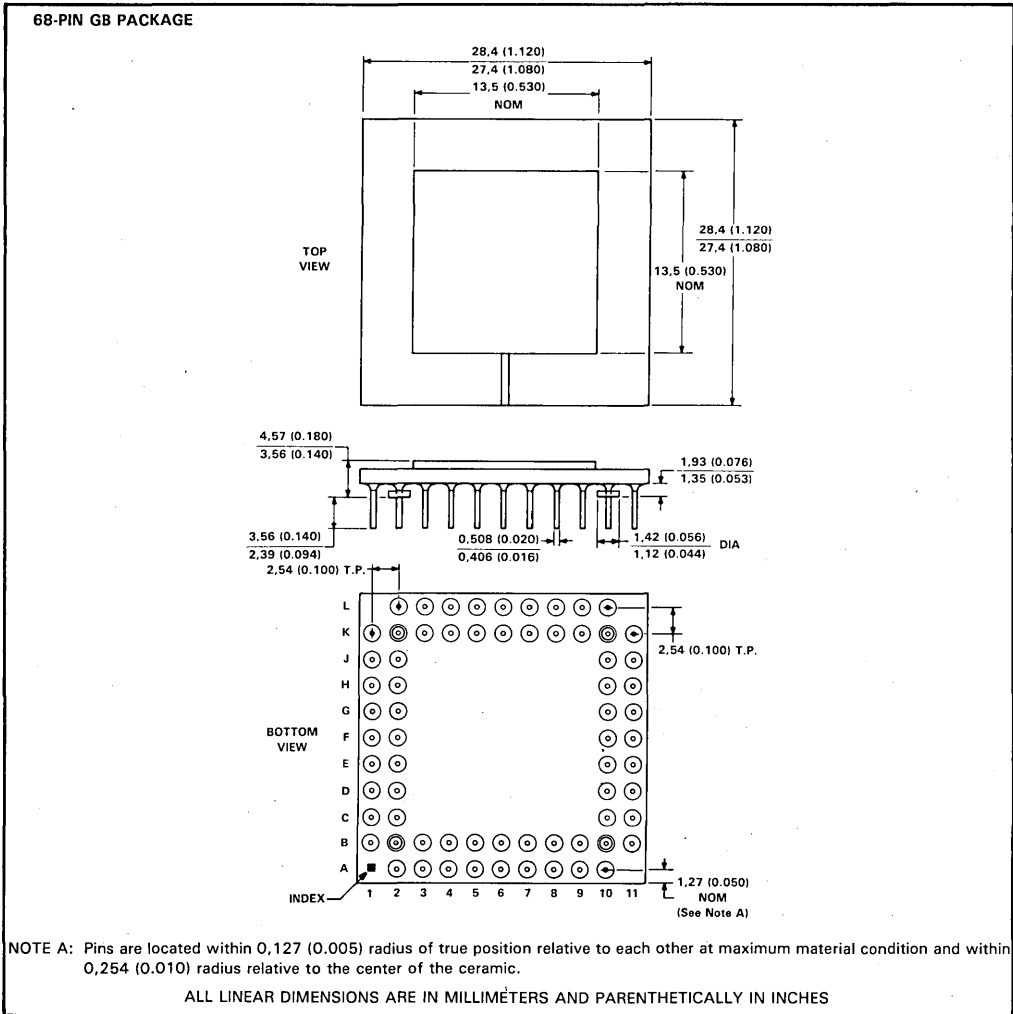
- NOTES: A. Centerline of center pin each side is within 0,10 (0.004) of package centerline as determined by dimension B.  
 B. Location of each pin is within 0,127 (0.005) of true position with respect to center pin on each side.  
 C. The lead contact points are planar within 0,10 (0.004).

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

# MECHANICAL DATA

## 68-pin GB pin grid array ceramic package

This is a hermetically sealed ceramic package with metal cap and gold-plated pins.



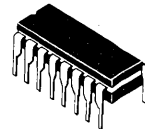
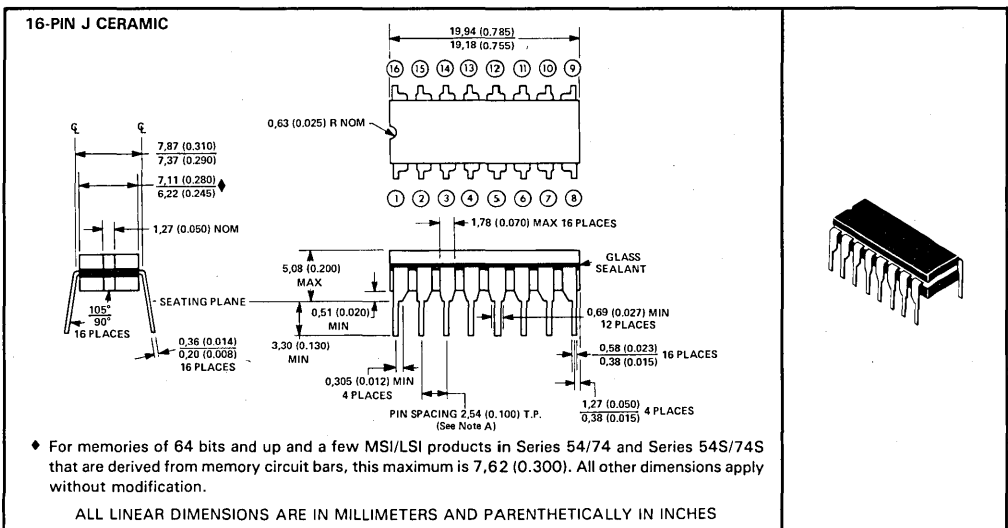
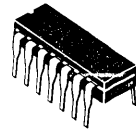
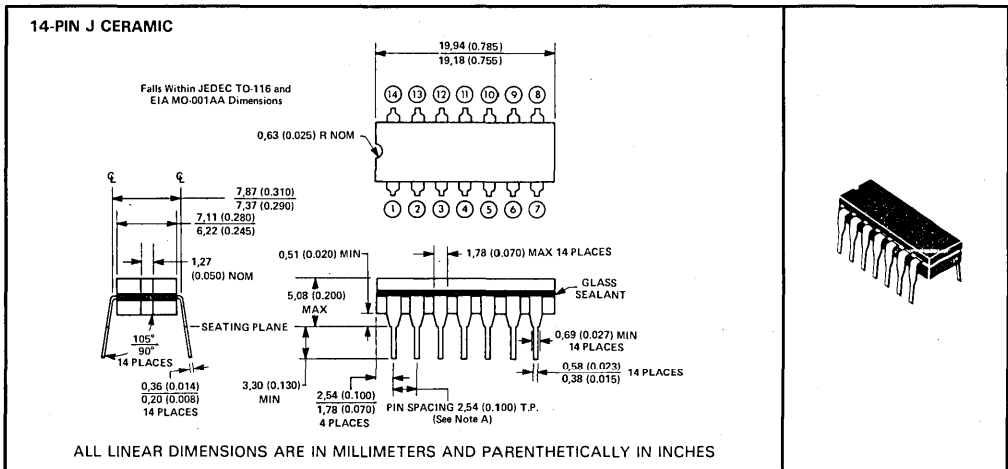
Mechanical Data

4

**J ceramic packages (including JD, JT, and JW dual-in-line packages)**

Each of these hermetically sealed dual-in-line packages consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300) or 15,24 (0.600) centers. Once the leads are compressed and inserted sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

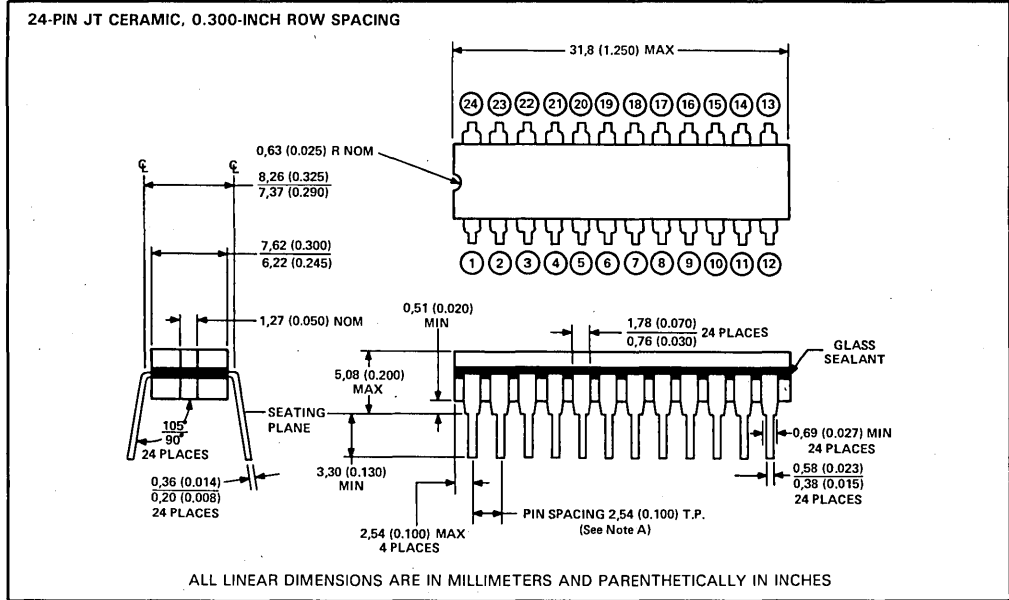
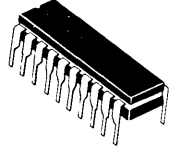
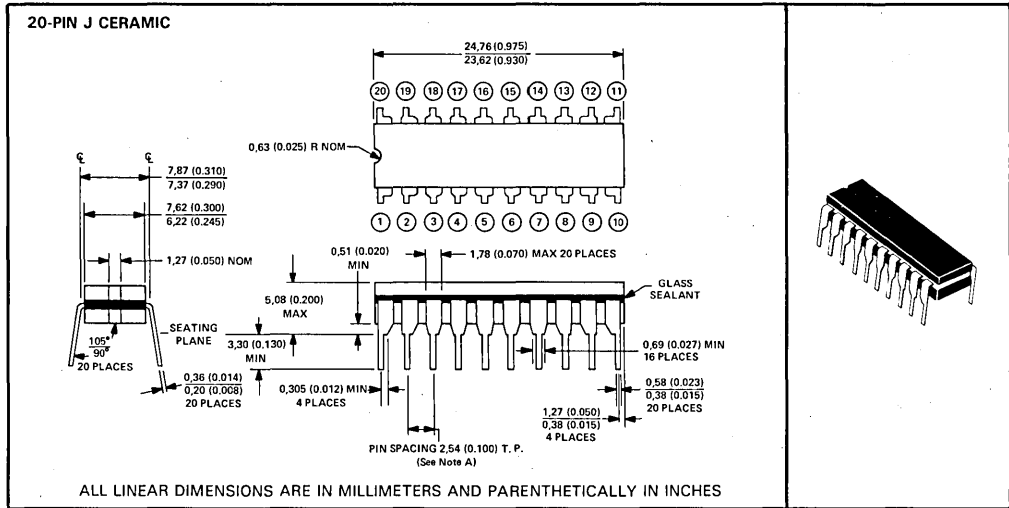
NOTE: For the 14-, 16-, and 20-pin packages, the letter J is used by itself since these packages are available only in the 7,62 (0.300) row spacing. For the 24-pin packages, if no second letter or row spacing is specified, the package is assumed to have 15,24 (0.600) row spacing.



NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

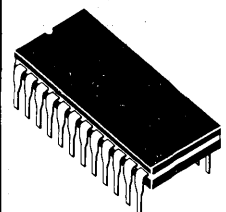
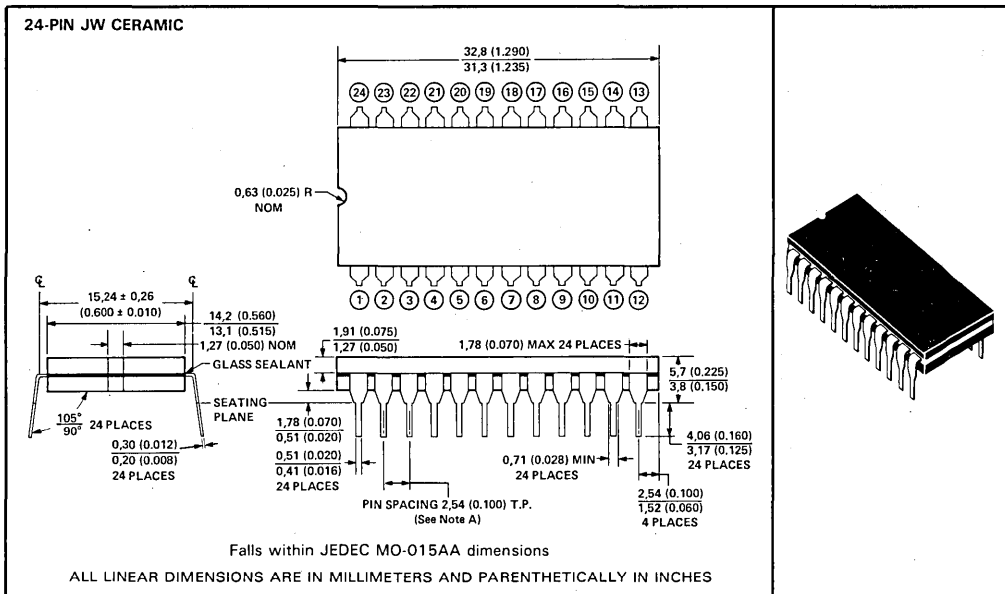
# MECHANICAL DATA

## J ceramic dual-in-line packages (continued)



NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

J ceramic dual-in-line packages (continued)



NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

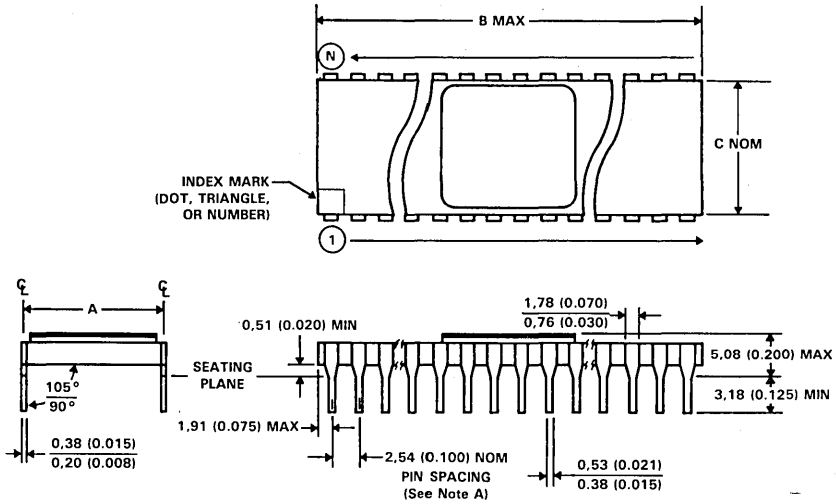


# MECHANICAL DATA

## J ceramic dual-in-line packages (continued)

This is a hermetically sealed ceramic package with a metal cap and side-brazed tin-plated leads.

### JD CERAMIC--SIDE BRAZE



| DIM \ PINS (N)                     | 16               | 18               | 20               | 22               | 24               |
|------------------------------------|------------------|------------------|------------------|------------------|------------------|
| A +0,51 (+0.020)<br>-0,25 (-0.010) | 7,62<br>(0.300)  | 7,62<br>(0.300)  | 7,62<br>(0.300)  | 7,62<br>(0.300)  | 7,62<br>(0.300)  |
| B (MAX)                            | 20,57<br>(0.810) | 23,11<br>(0.910) | 25,65<br>(1.010) | 27,94<br>(1.100) | 30,86<br>(1.215) |
| C (NOM)                            | 7,37<br>(0.290)  | 7,37<br>(0.290)  | 7,37<br>(0.290)  | 9,91<br>(0.390)  | 7,37<br>(0.290)  |

| DIM \ PINS (N)                     | 24               | 28               | 40               | 48               | 52               | 64               |
|------------------------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| A +0,51 (+0.020)<br>-0,25 (-0.010) | 15,24<br>(0.600) | 15,24<br>(0.600) | 15,24<br>(0.600) | 15,24<br>(0.600) | 15,24<br>(0.600) | 22,86<br>(0.900) |
| B (MAX)                            | 31,8<br>(1.250)  | 36,8<br>(1.450)  | 52,1<br>(2.050)  | 62,2<br>(2.450)  | 67,3<br>(2.650)  | 82,6<br>(3.250)  |
| C (NOM)                            | 15,0<br>(0.590)  | 15,0<br>(0.590)  | 15,0<br>(0.590)  | 15,0<br>(0.590)  | 15,0<br>(0.590)  | 22,6<br>(0.890)  |

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

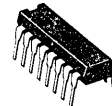
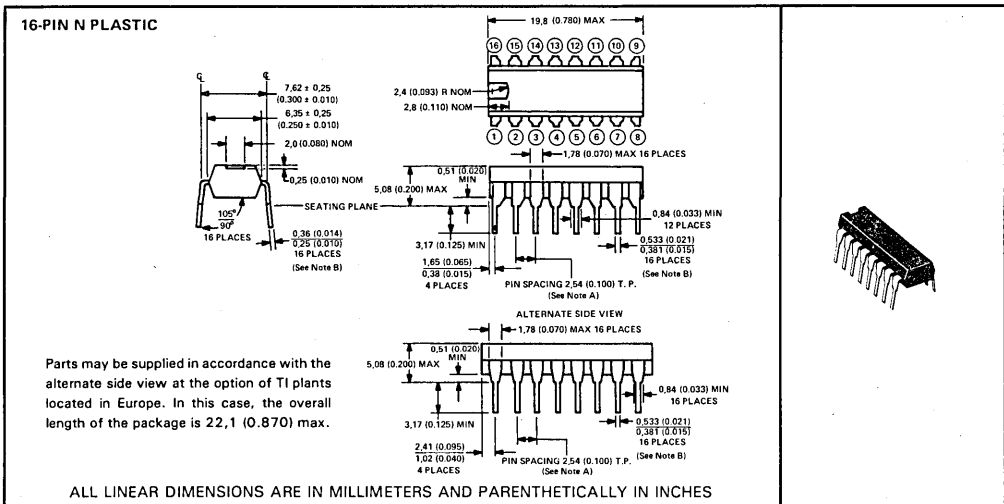
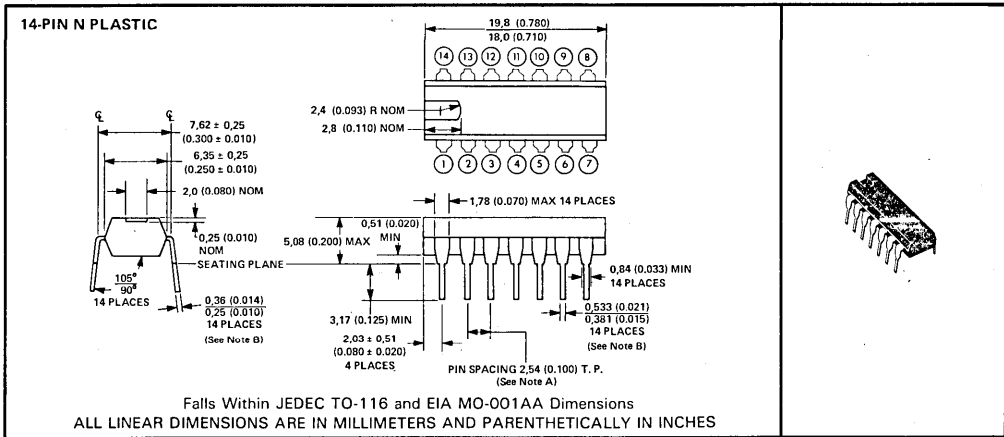
Mechanical Data

4

**N plastic packages (including NT and NW dual-in-line packages)**

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300), 15,24 (0.600), or 22,86 (0.900) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin packages, the letter N is used by itself since only the 24-pin package is available in more than one row-spacing. For the 24-pin package, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.

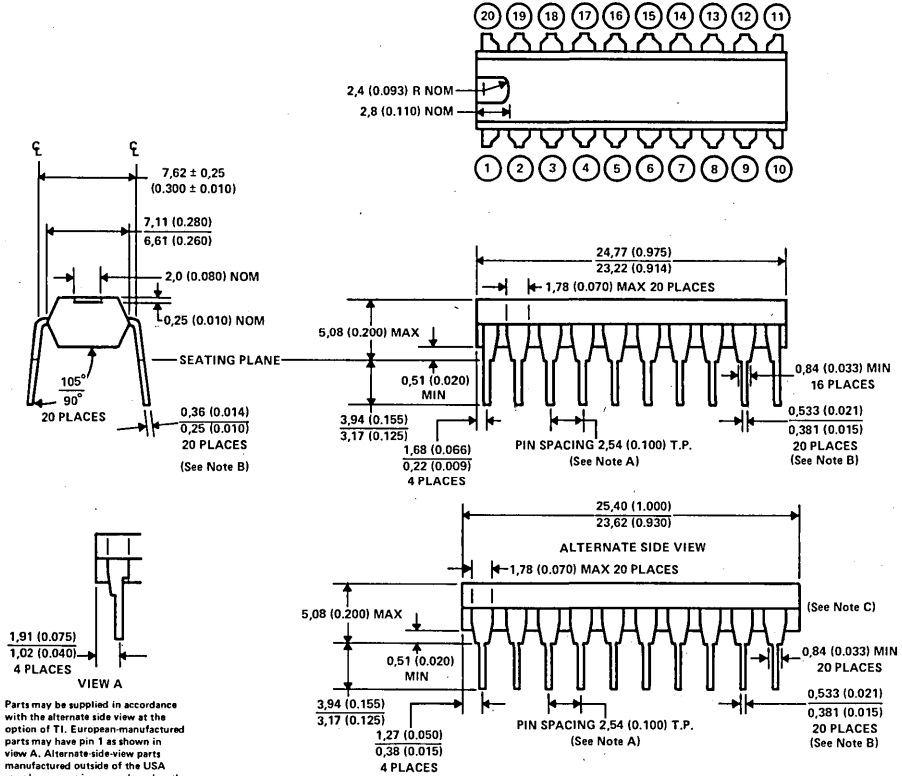


NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.  
B. For solder-dipped leads, this dimension applies from the lead tip to the standoff.

# MECHANICAL DATA

## N plastic dual-in-line packages (continued)

### 20-PIN N PACKAGE



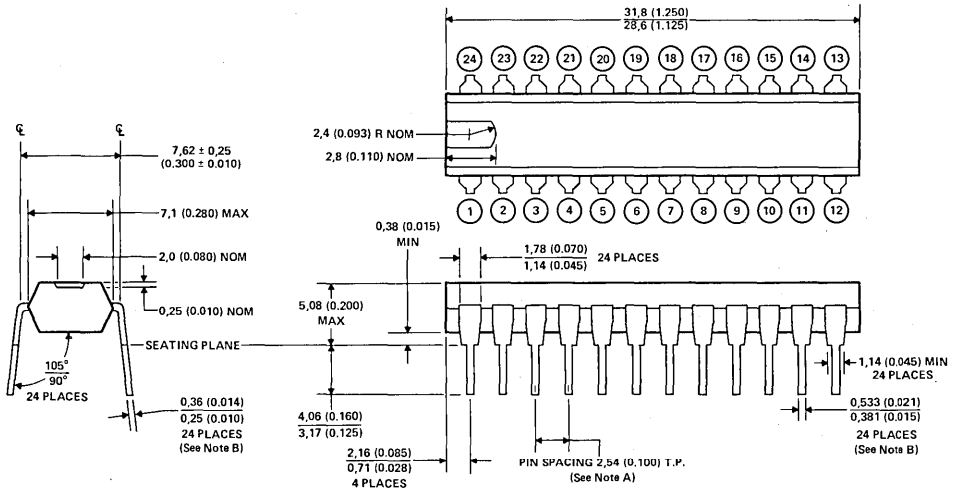
Parts may be supplied in accordance with the alternate side view at the option of TI. European-manufactured parts may have pin 1 as shown in view A. Alternate-side-view parts manufactured outside of the USA may have a maximum package length of 26.7 (1.050).

- NOTES: A. Each pin centerline is located within 0.25 (0.010) of its true longitudinal position.  
 B. For solder-dipped leads, this dimension applies from the lead tip to the standoff.  
 C. Parts may be supplied with a draft angle of  $7^\circ$  typical at the option of TI.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHESTICALLY IN INCHES

N plastic dual-in-line packages (continued)

24-PIN NT PLASTIC

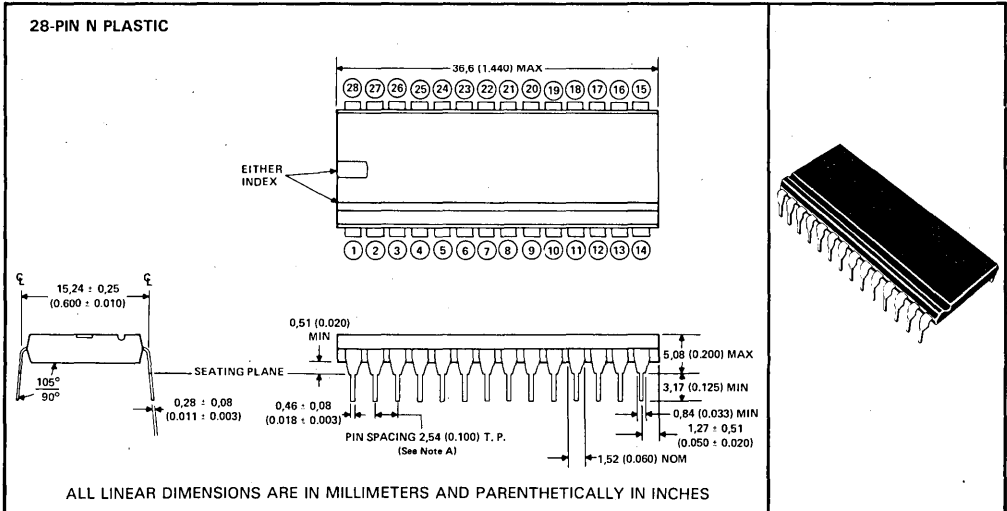
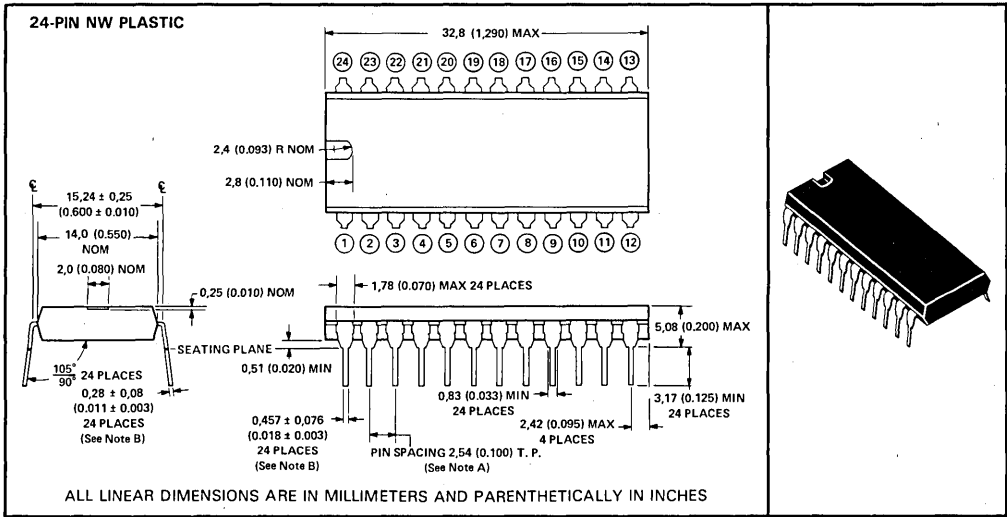


NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.  
 B. For solder-dipped leads, this dimension applies from the lead tip to the standoff.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHEMICALLY IN INCHES

# MECHANICAL DATA

## N plastic dual-in-line packages (continued)

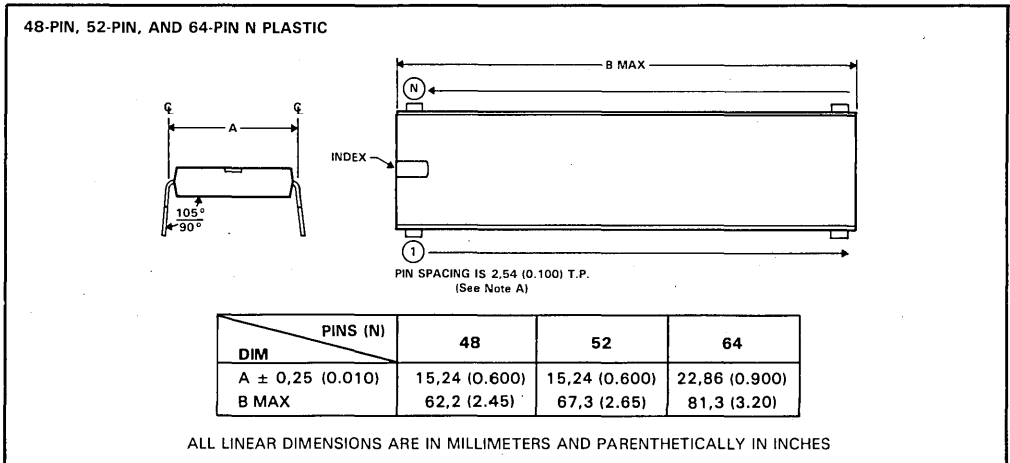
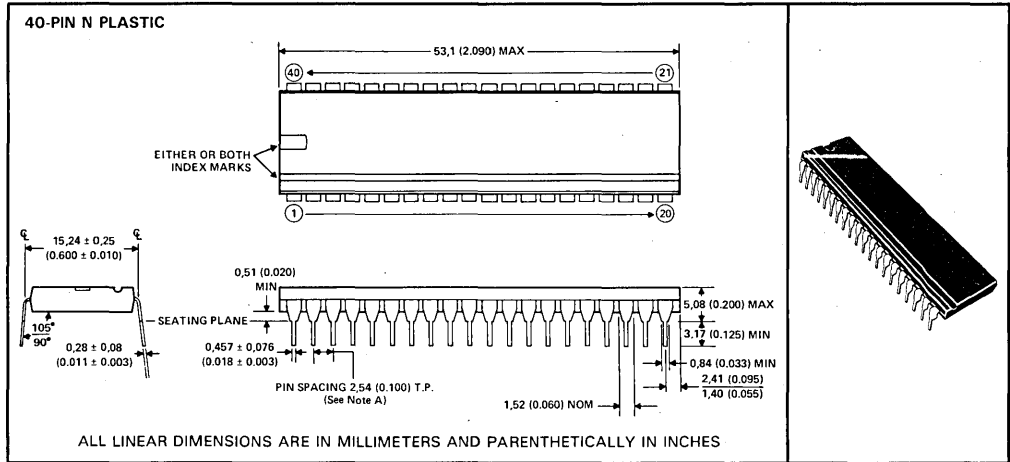


NOTES: A. Each pin centerline is located within 0,25 (0,010) of its true longitudinal position.  
 B. For solder-dipped leads, this dimension applies from the lead tip to the standoff.

Mechanical Data

4

N plastic dual-in-line packages (continued)



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.



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 (8:00 a.m. — 5:00 p.m. CST)

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